IF07 Electronics/ASICS
High Granularity, High Dynamic Range Readout
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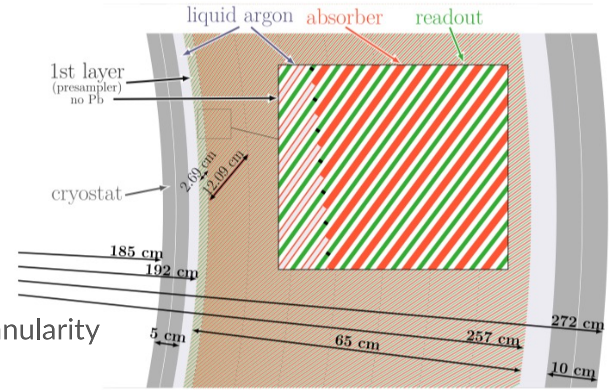
High Granularity, High Dynamic Range Readout

Nearly all detectors designed for the ILC, CliC, CEPC, FCC-ee, FCC-hh, (etc.) includes high granularity detectors, particularly for calorimeters. Driven by :

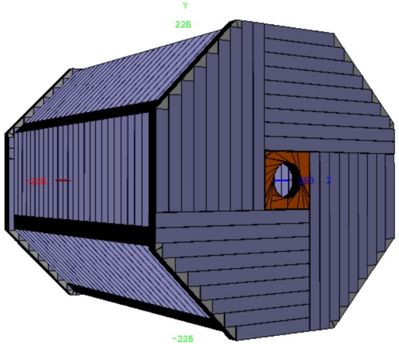
1) The success of particle flow algorithms CMS and ATLAS

2) The need to capture full EM and hadronic showers (of many TeV electrons).

Electronic readout must be developed to accommodate high granularity, high dynamic range detector requirements.



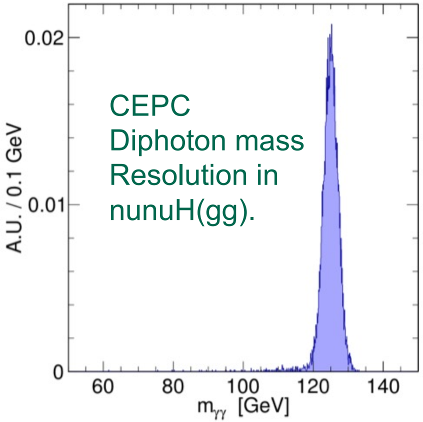
FCC-hh LAr calorimeter

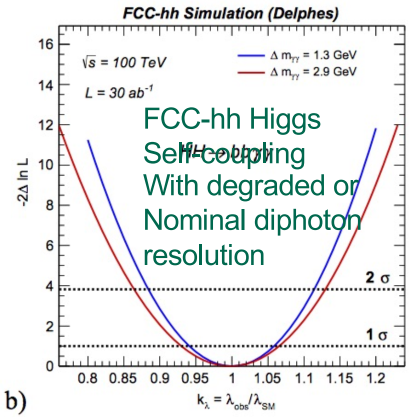

CEPC SiW calorimeter

Specifically addressing BRN:

PRD 1	Enhance calorimetry energy resolution for precision electroweak mass and missing-energy measurements
PRD 2	Advance calorimetry with spatial and timing resolution and radiation hardness to master high-rate environments
PRD 16	Develop process evaluation and modeling for ASICs in extreme environments
PRD 17	Create building blocks for Systems-on-Chip for extreme environments

Science Need





Physics drivers - The physics focuses are different for each detector, but Higgs physics with photons will continue to be driver (above benchmark plots from CEPC and FCC-hh).

Technology opportunity – At the extreme end (FCC-hh) the speed, precision, high density (channel count), high-dynamic range "low-power readout" ASICS needed do not exist in any technology. Creative system architecture is needed. For the ILC and CEPC electronics readout design is already well underway (SKIROC chip, SPIROC chip, respectively).

This work both develops technical expertise in instrumentation and engineering for detector design and maintains detector design in physics community.

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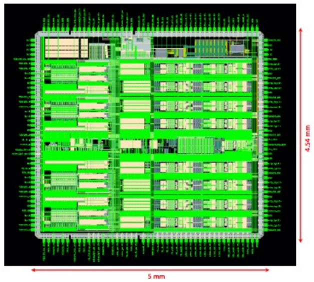
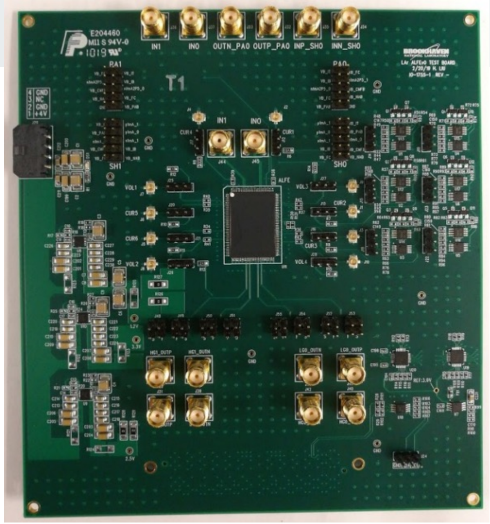
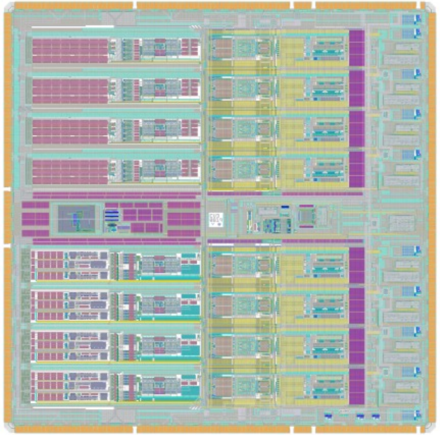




COLUTAv3 Die



Current effort

ASICS design and system architecture – determine specifications need, possible technological implementations, identify areas that require novel design work.

Team : Columbia U, BNL, UT Austin

Existing team involved in ATLAS LAr calorimeter electronics development. Current challenge is “high” dynamic range, “high” granularity (by HL-LHC standards) PA/S and ADC ASICS investigating novel ”dynamic ranging enhancing” architectures. - Can we apply these techniques to meet the coming challenges?

New people and new ideas welcome!

Possible Focus: Open-Source ASICS

- Significant recent progress in Free and Open-Source (FOSS) tools for ASIC design, and open-source PDKs.
    - Skywater SKY130 nm Open Foundry, Efabless OpenLane design tools.
        - Other nodes in progress
- Advantages:
    - Simplifies collaboration, fewer IP/NDA issues. More reusable design blocks.
    - Aligned with open software/hardware movement in the field.
    - Lower costs: ~10 mm^2 useable area <$10k for MPW run (at least for now), and FOSS design flow (vs CADANCE) means more/smaller groups can participate
- Disadvantages:
    - Only 1 fab, 1 technology node (as of today).
    - Focus now on digital design (some progress on analog design in progress).

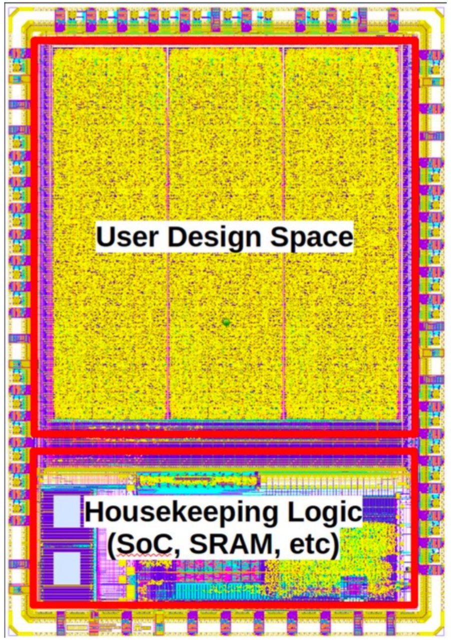


Figure 3: Available chip area for user design (top) and provided housekeeping below for SKY130 MPW.

Open-Source Readout at Future Detectors

- First step – design and fabricate a chip hosting generic R&D components (basic digital structures, “simple” analog building blocks) and testing irradiation hardness of technology.
    - Just the start of evaluation of this design flow/fab. Would likely need substantial work in understanding and removing design constraints in their MPW (specifically analog development and radiation testing), understanding long term costs, verifying open IP, integration with CERN building blocks (I2C)….
    - Would lead to the first useable, shareable blocks for ASISCs
- Opportunities:
    - If initial work is successful, we can imagine a plan of open, reusable development of ASICs for ~FCC-era detectors done by large and small groups at labs and universities.
    - Low cost/fast turnaround also gives additional flexibility. For example, could plan more aggressive ASICs for on-detector process, effectively moving functionality from off-detector FPGAs to on-detector digital very application specific ICs (potentially leading to more sophisticated, low-level triggering)

Plan for Whitepaper

- Explore open-source design/fab as response to calorimeter and readout electronics BRN PRDs.
- Use specific case of FCC-hh calorimeter to focus discussion.

Synergies

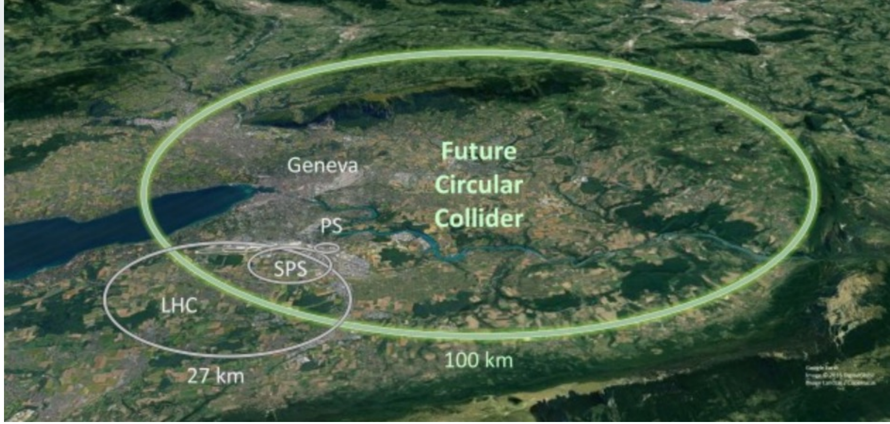
There is significant overlap with specific detector design groups. Important to connect with existing efforts in detector design, simulation, reconstruction.

Connects **IF6 Calorimetry**, and to some degree the rest of the IF groups.

Detailed electronics specifications for specific detectors are driven by (sometimes) a specific, single physics case (eg. Mass resolution in nunu(H->diphotons) process). Important to know what we are designing for, and possible areas for students to participate in reconstruction and analysis details.

Need input for calorimetry and physics groups.

Conclusion



Future detectors and future calorimeters will need high-granularity. The extreme: A 100 TeV collider requires extraordinarily high-dynamic range readout, along with high-granularity to reconstruct photon showers at the EW-scale up to O(10 TeV). **Absolute need for new** ideas for electronic readout of these detectors.

In any new detector electronics and ASIC development are natural areas for US to contribute. We need to be involved now.