University of Hawaii
Instrumentation Development Laboratory

HEP-IC 2022
Fermilab
18-MAY-2022

IDL
Instrumentation
Development
Lab

A brief History of ASIC design @ UH

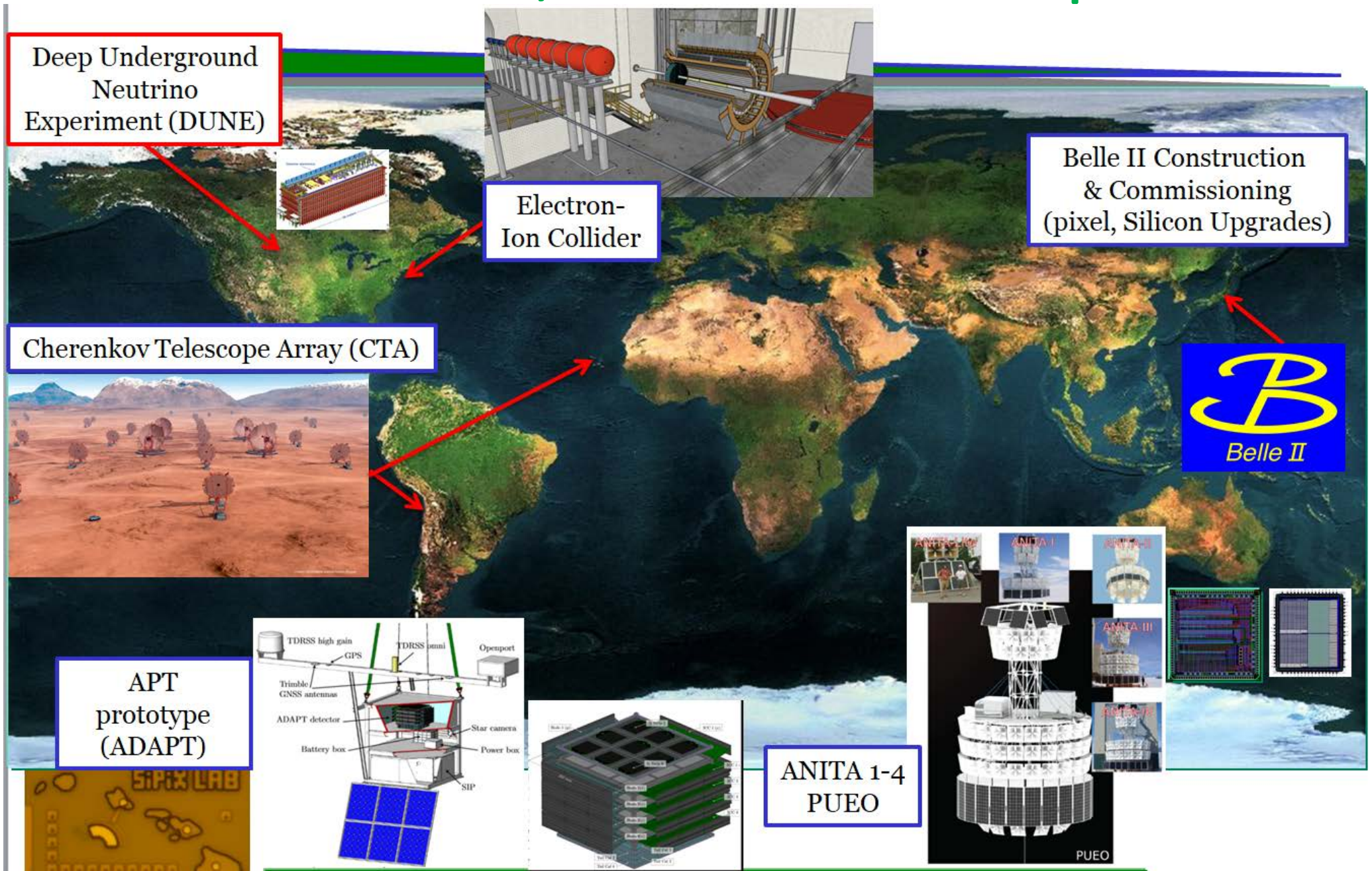
1. **Didn't exist until founding of the ID Lab (circa 2000)**

2. **Had done much board and system-level design, starting with CP-LEAR and GEM @SSC (worked with many ASIC designers)**

3. **After stint in silicon valley, where did ASIC design for start-up company, was contacted with an interesting problem**

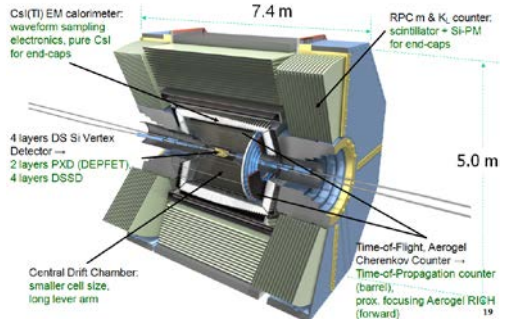
4. **Peter Gorham was at JPL (knew each other from DUMAND days) and wondered if could build a low-power transient digitizer for VHF/UHF signals, which would be enabling for radio neutrino detection**

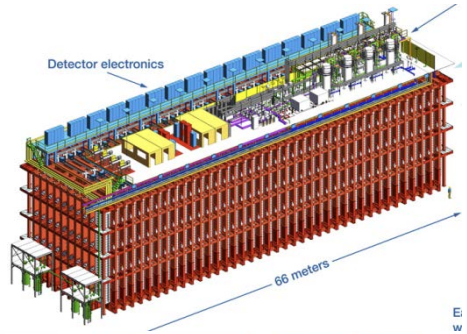
Since then, a world-wide impact

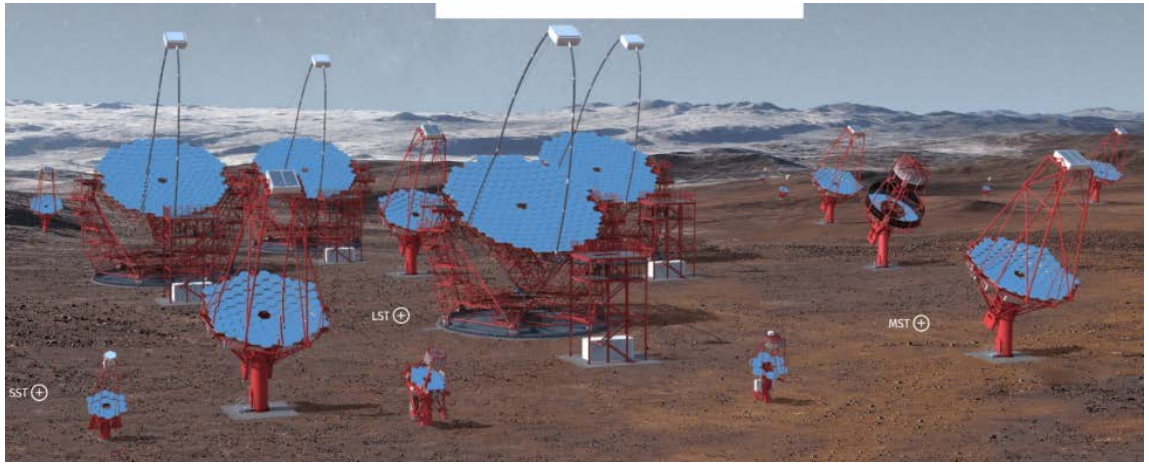


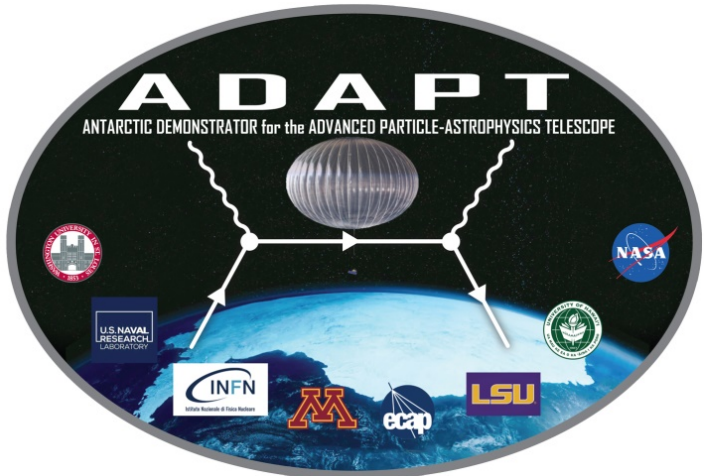
ASICs as enabling tools to the Big Questions

1. CP violation (how get more matter than anti-matter, but not too much)
2. Does CP violation also occur in leptons (and 3-generation problem) ?
3. Origin of highest energy cosmic rays and their neutrino fingerprint?
4. What is the nature and origin of Dark Matter ?







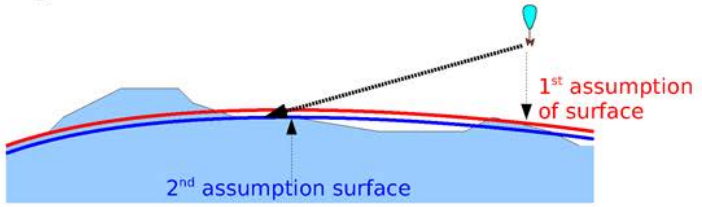


ANITA: LABRADOR3

- **Flown all 4 ANITA flights. LAB4D developed for ANITA5**

<30ps timing

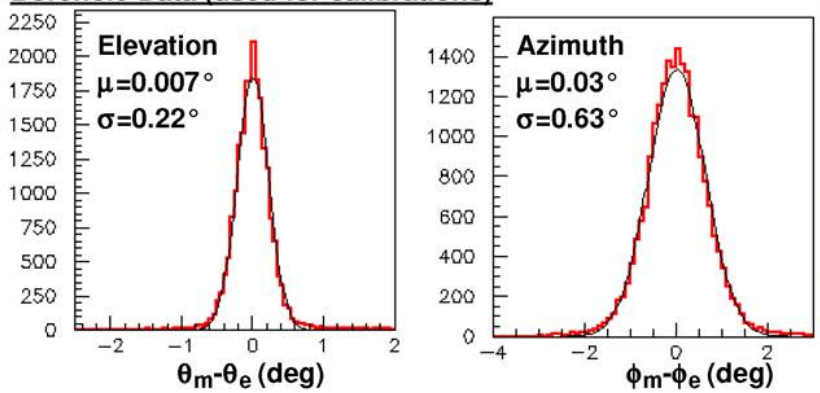
RF Projection onto the surface



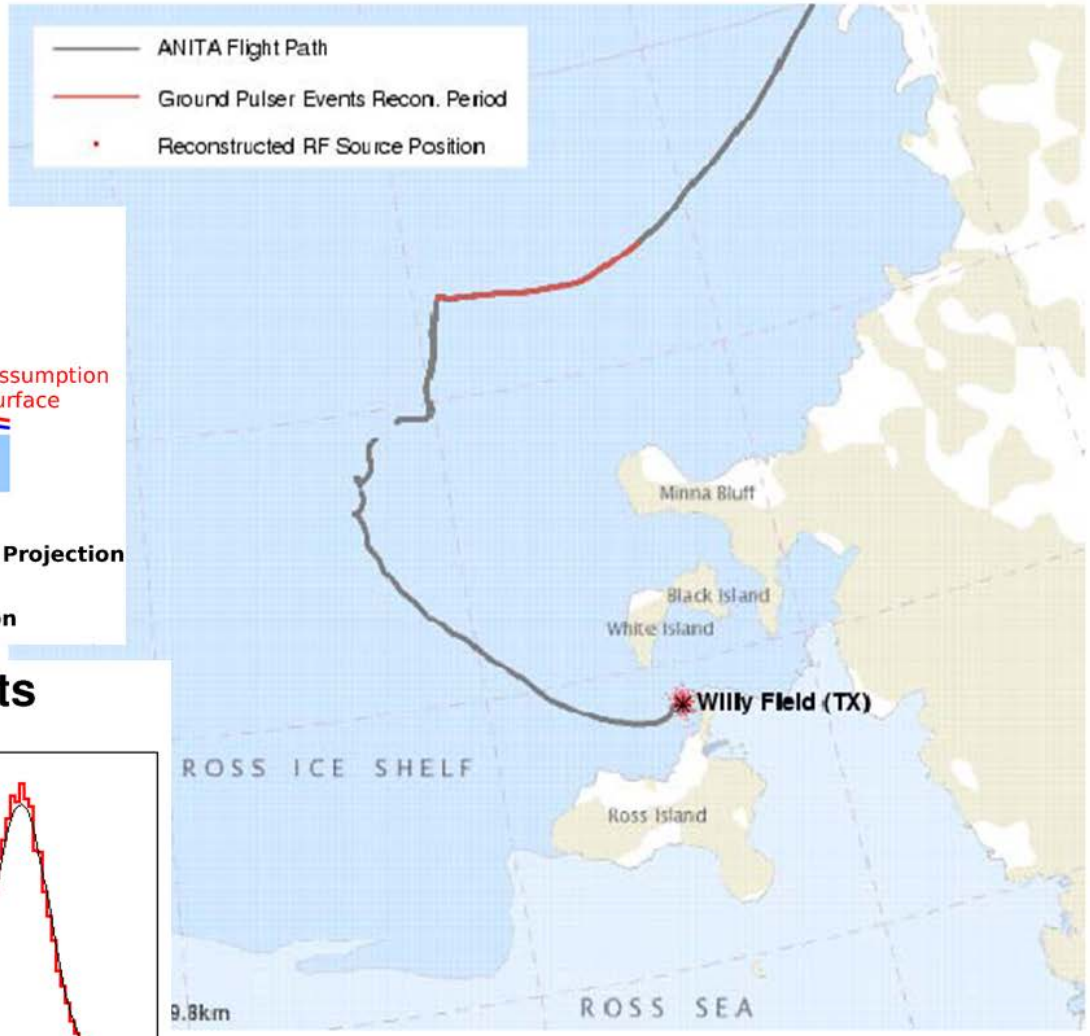
Fast Algorithm: Line Sphere intersection
1st R_{earth}=Geoid + Surface @ Ballon position -> Rough Projection
2nd R_{earth} = Geoid + Surface @ (position from 1st)
3rd: one more iteration -> converged after 2nd iteration

V-pol results

Borehole Data (used for calibrations)



3.8 mrad **11.2 mrad**

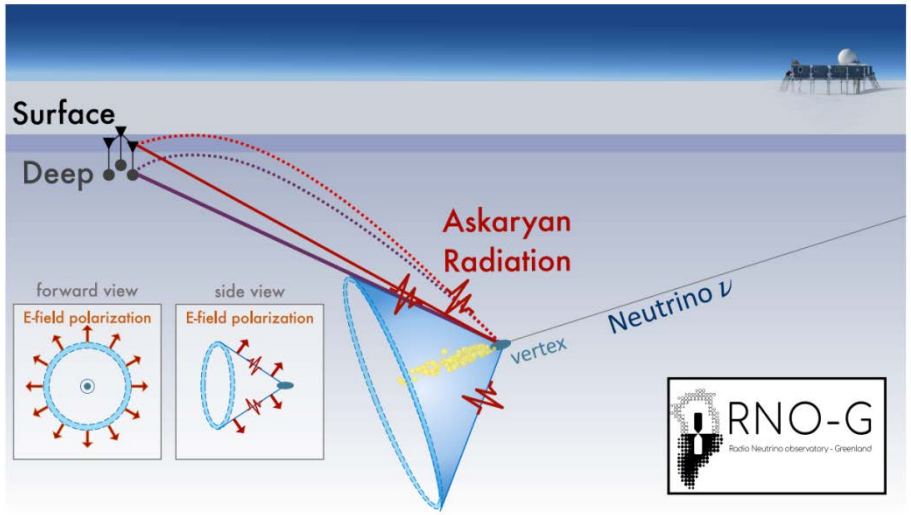


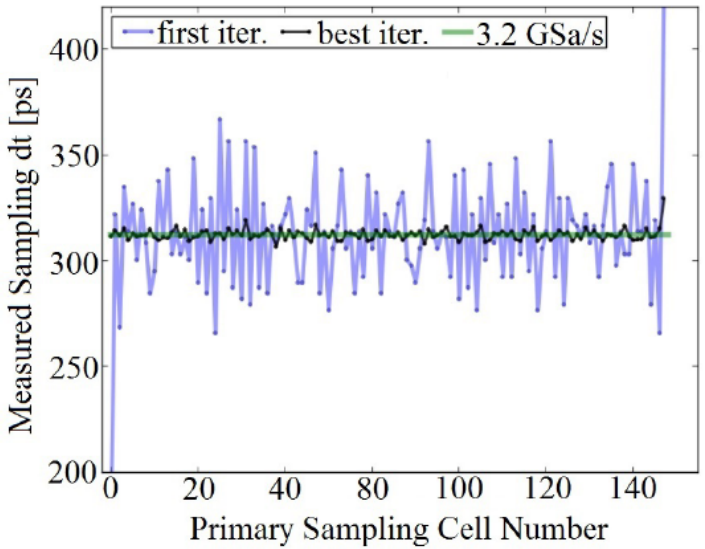
Further exploration directions?

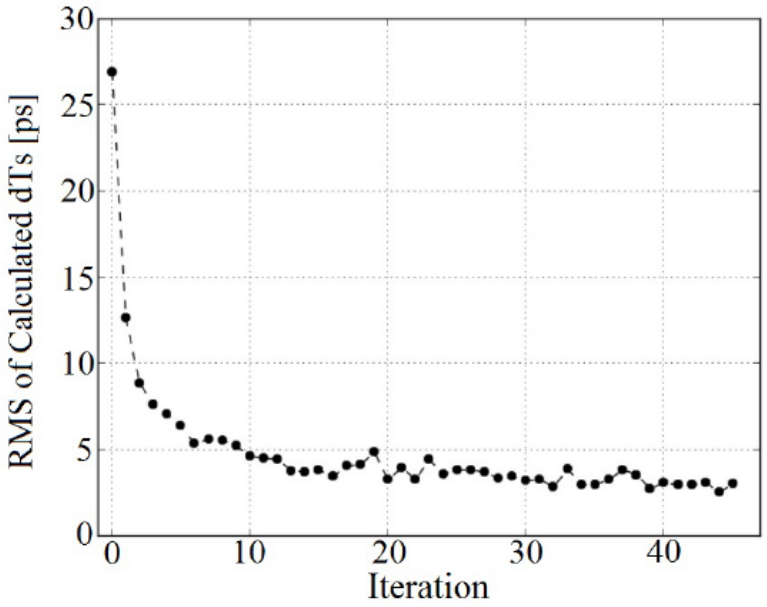
- **Limits of timing resolution (RF-Pix → <1ps time resolution)**
- **Channel density**
- **Processing/feature extraction on chip (digital synthesis)**
- **Timing calibration**

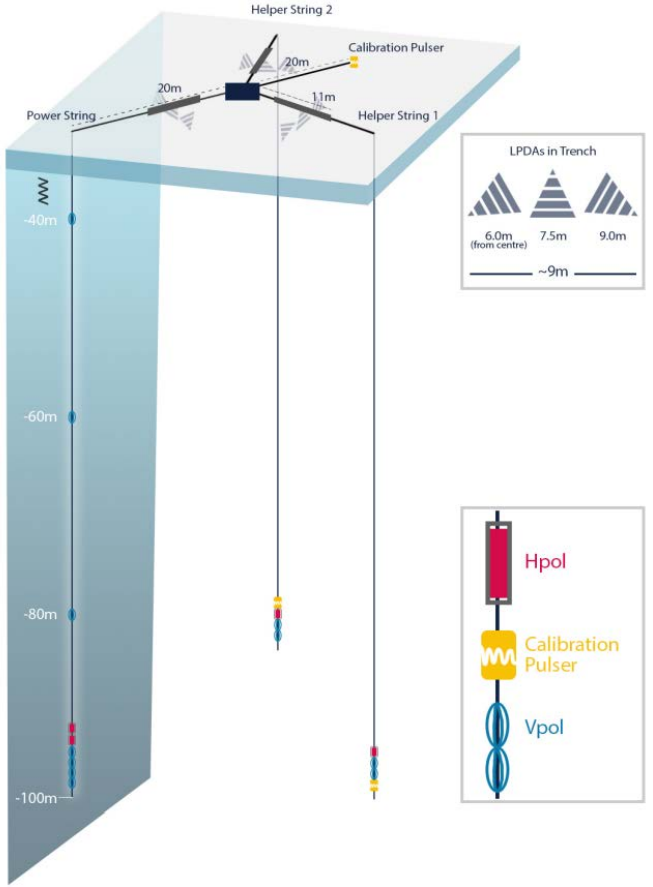
RNO-G: LAB4D

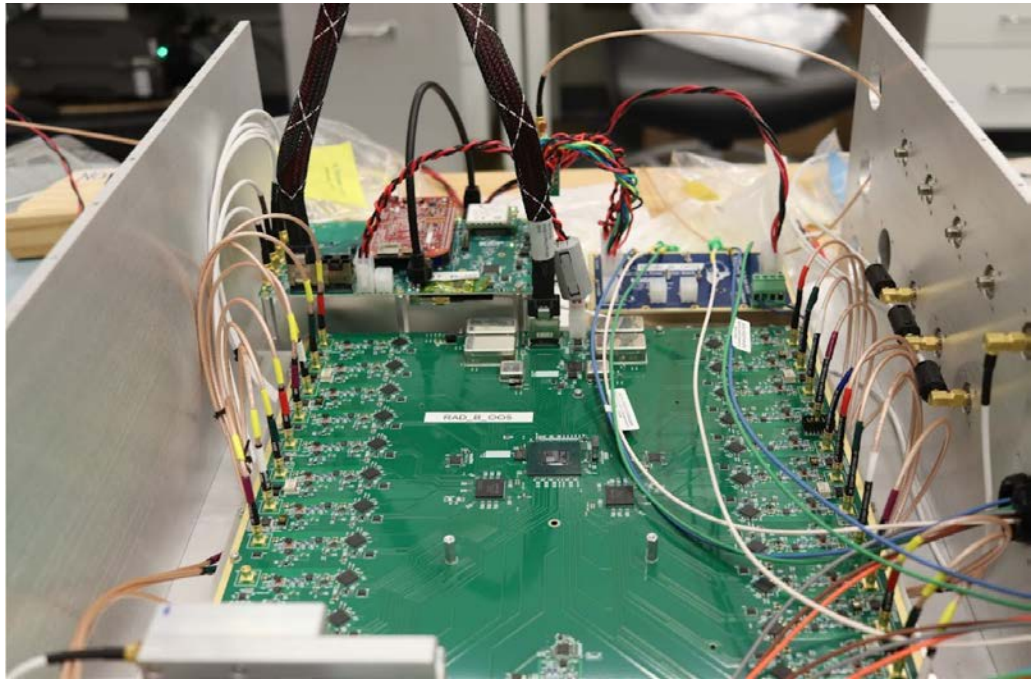
- **LAB4D explored removing "dT" non-uniformity**







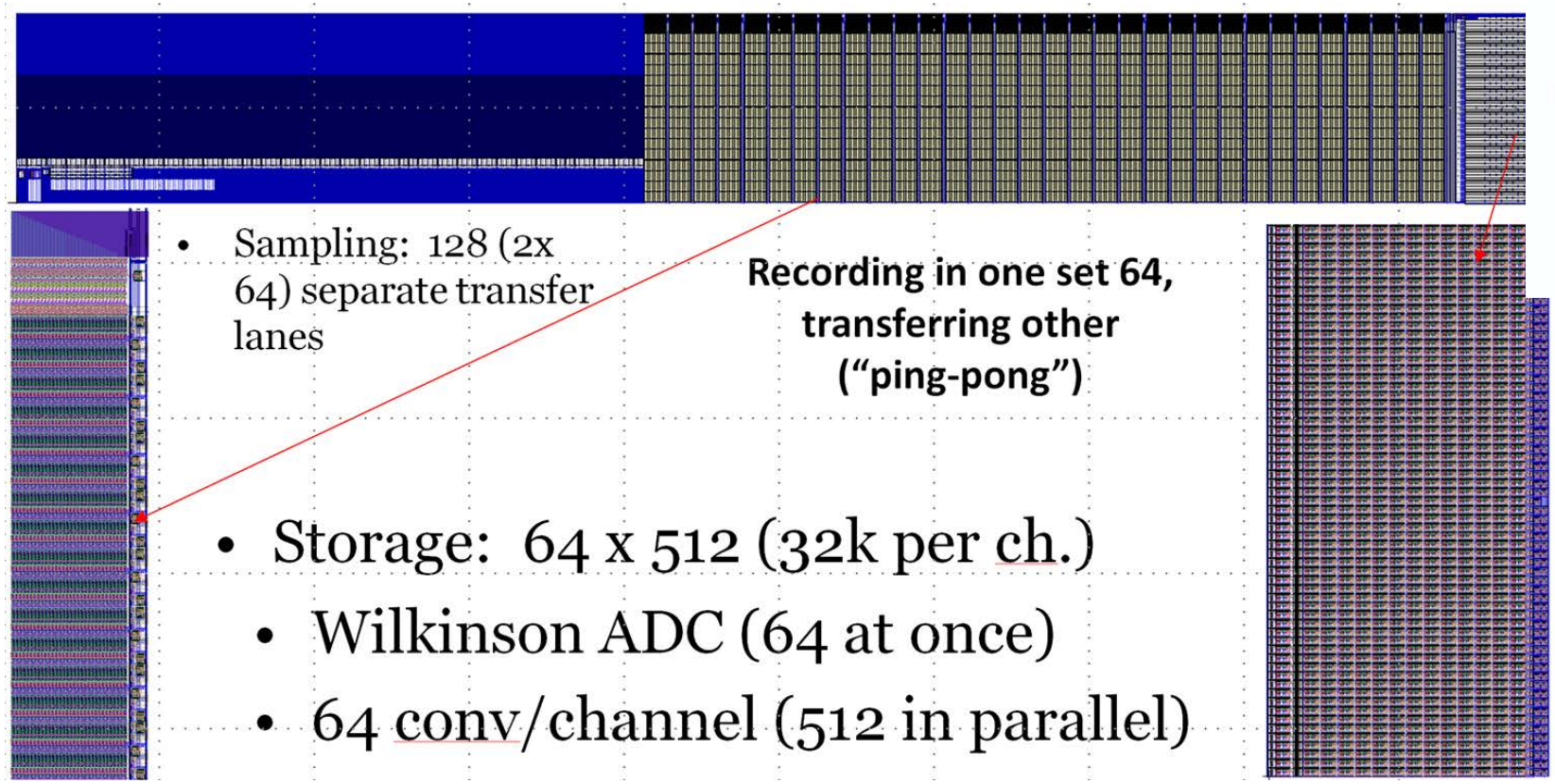


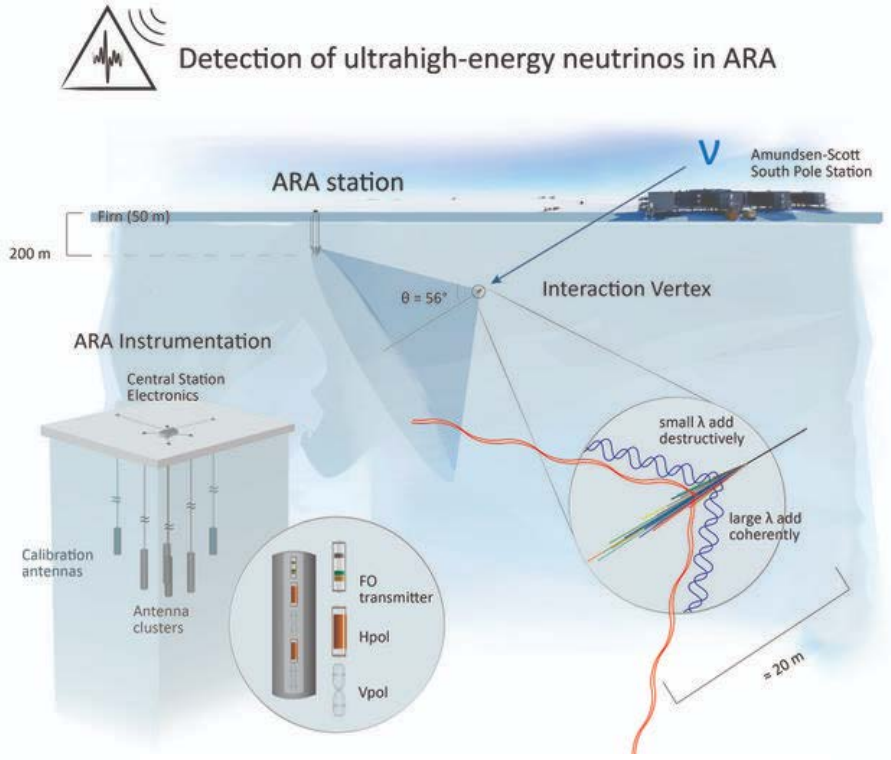


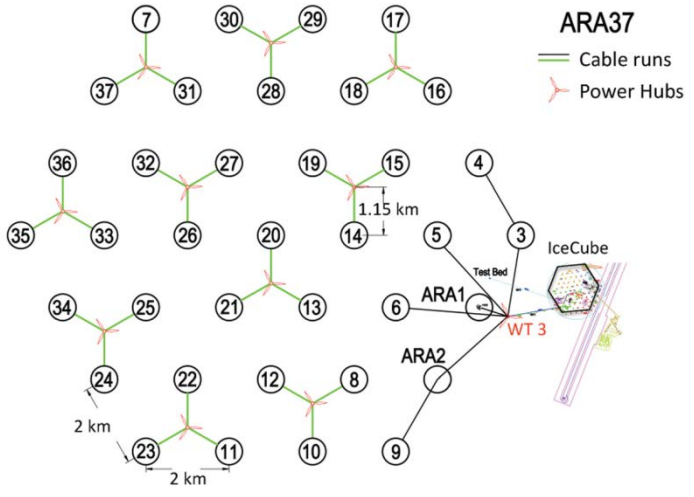
- Removes ~15% diff Timing sample width
- Cal. Converges to ~3ps in 32 iterations
- Avoids re-processing and splining (impossible for real-time triggering)

ARA: IceRadio Sampler

- **Explore how deep (reasonably) can go with SCA architecture**
- **Force single-station trigger and coherently phase stations offline**

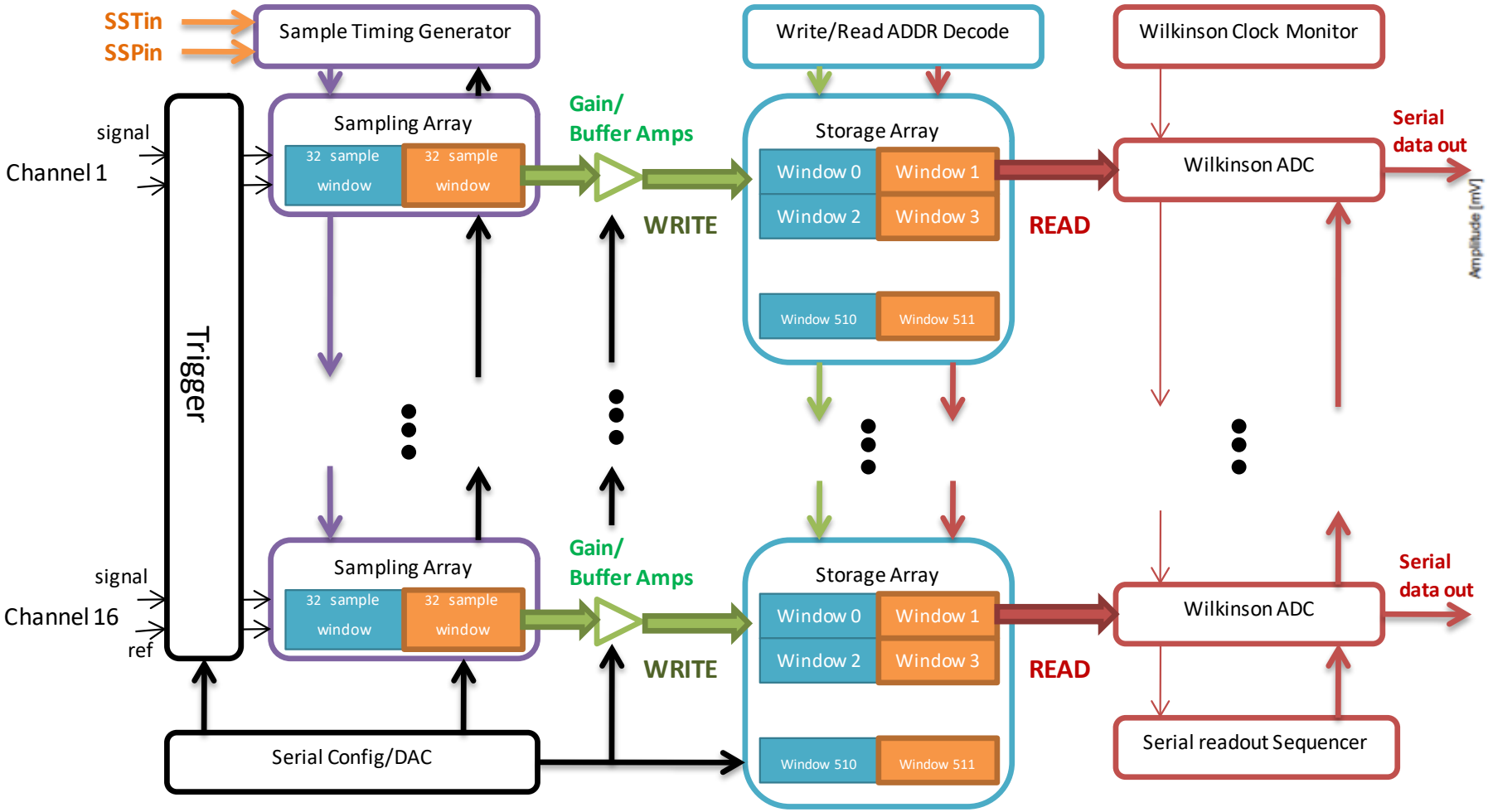


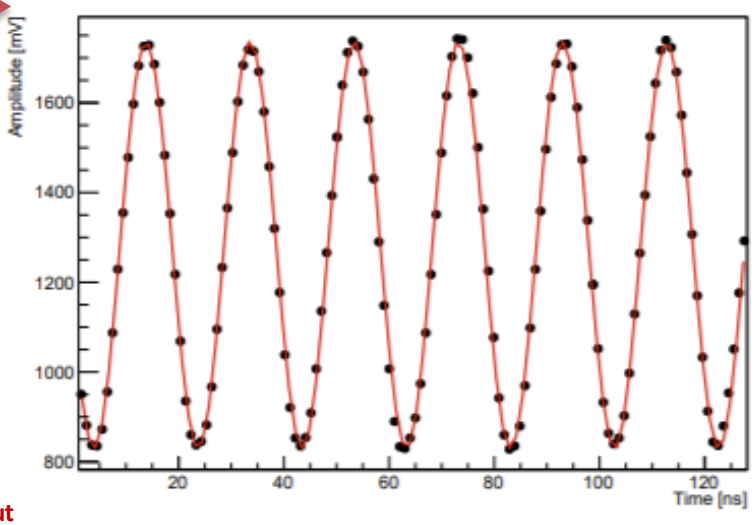




CTA: TARGET

- **Less depth, slower sampling speed, higher channel density**

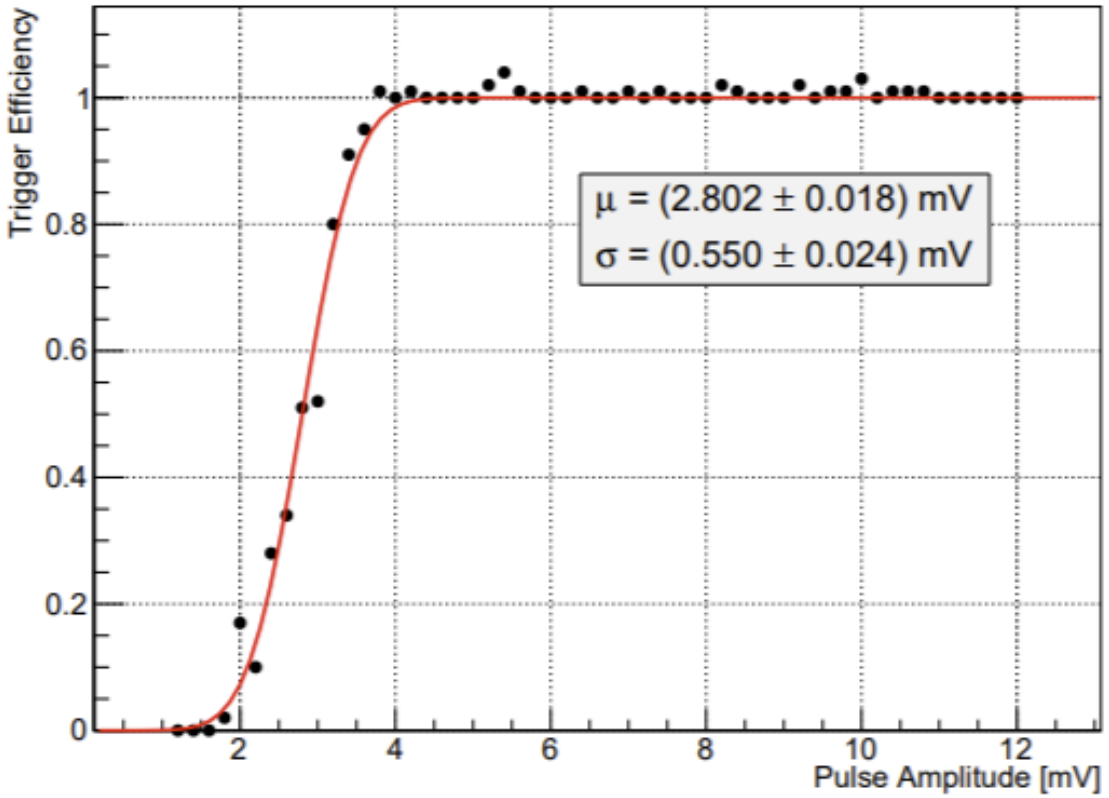




- Sample 50MHz sine wave used for calibration

CTA: CT5TEA

- **Low threshold, analog sum triggering (companion ASIC)**

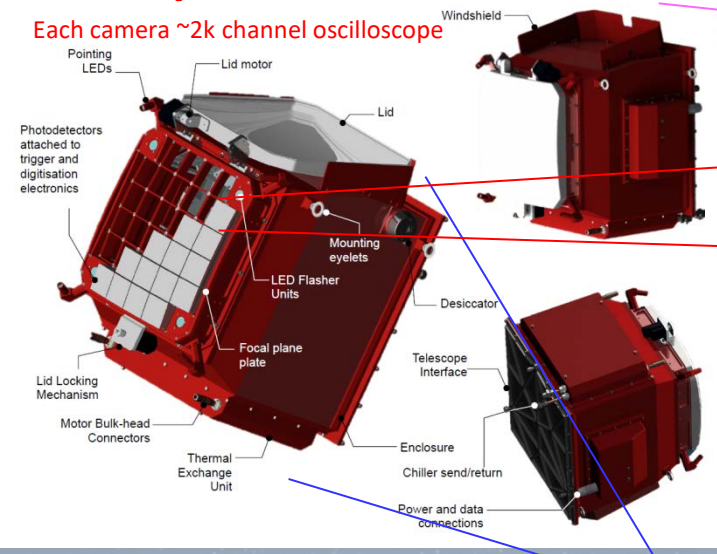


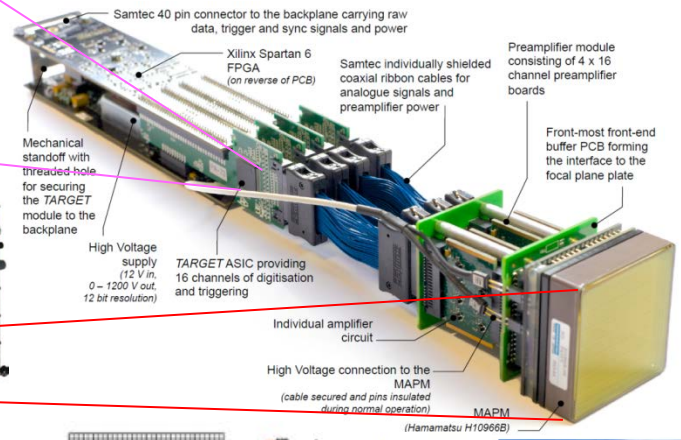
- **Sum of 4 inputs achieves this**
- **Provides DC offset to TARGET sampler**

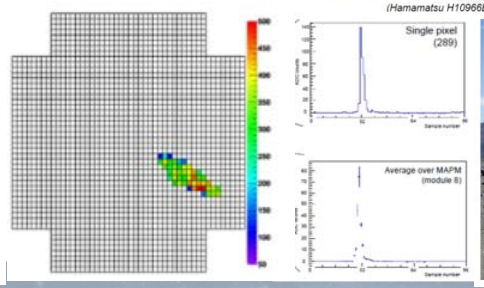
Cherenkov Telescope Array

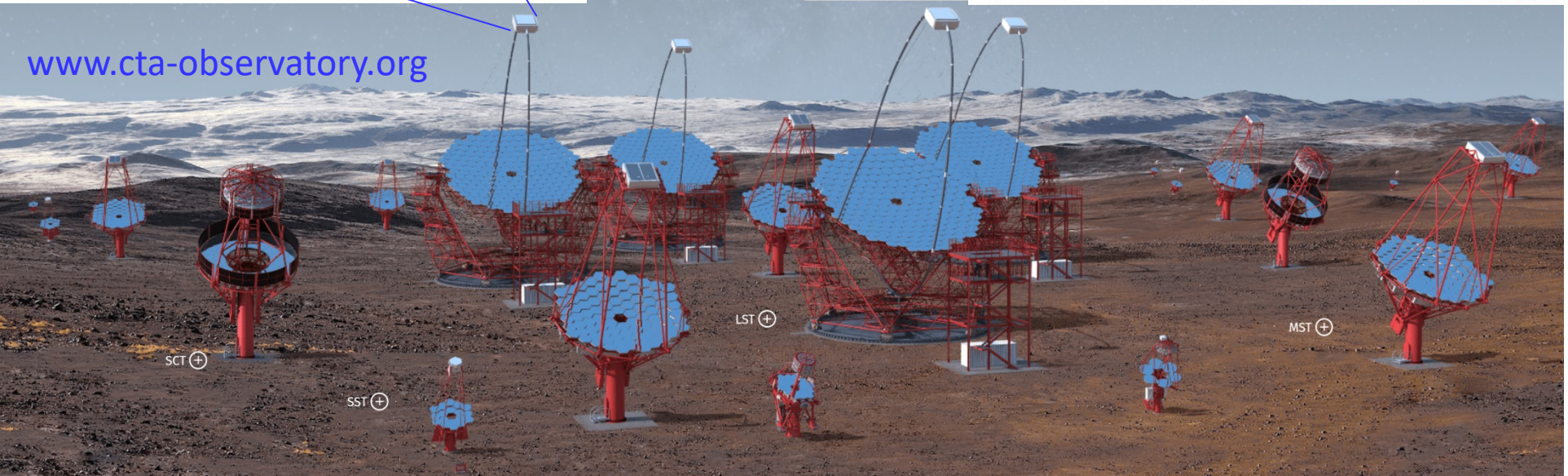
- **Enabling in reducing the SST camera production costs**

Each camera ~2k channel oscilloscope

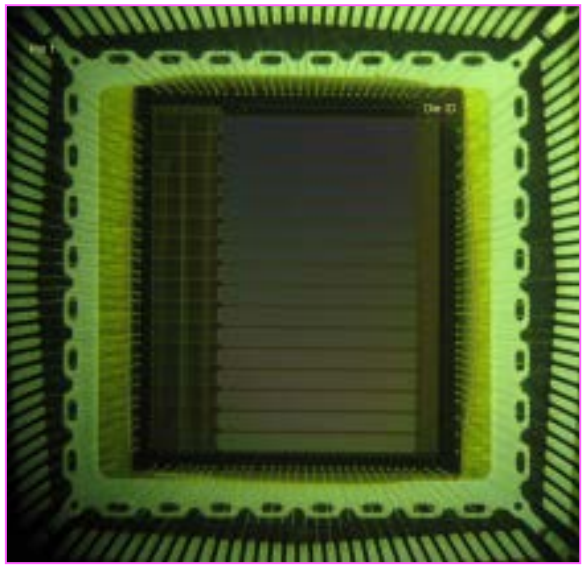








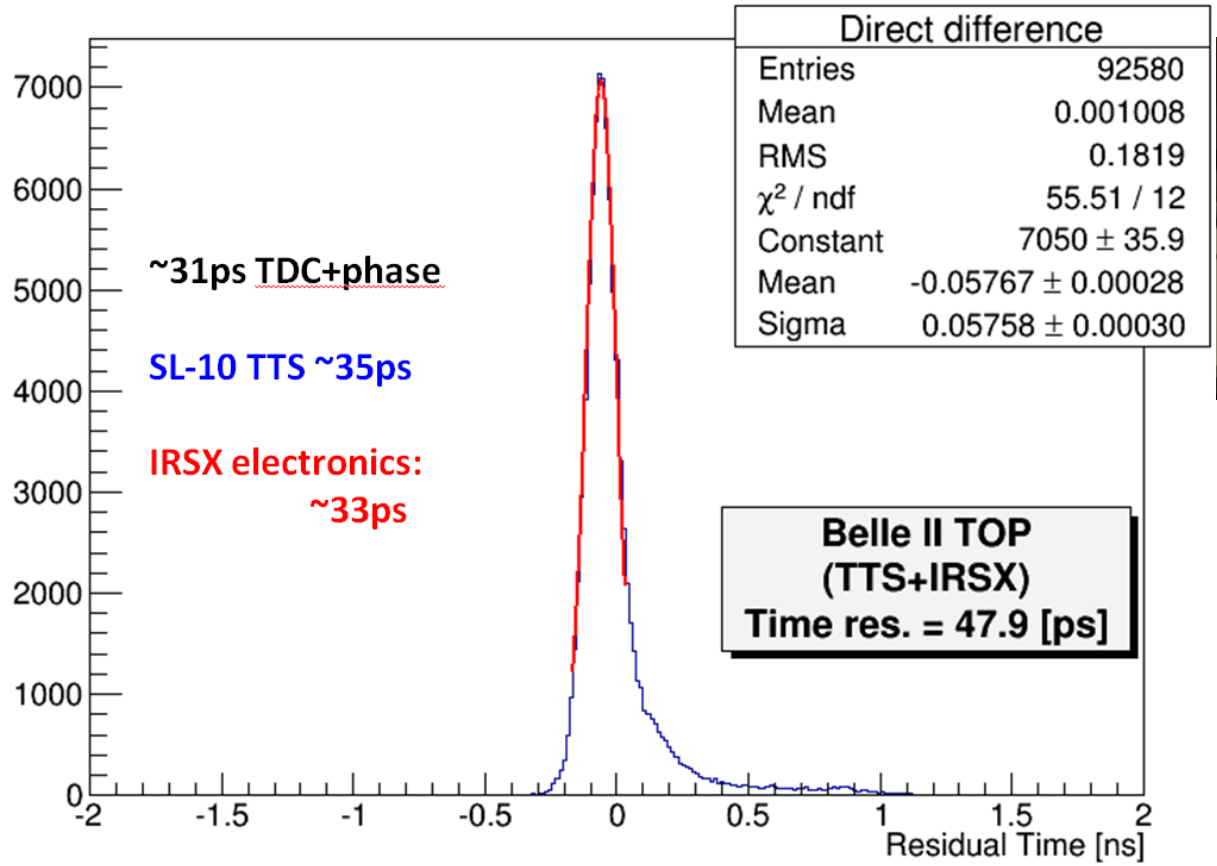
CTC (sampler)
CT5TEA (trigger)
Gang Liu

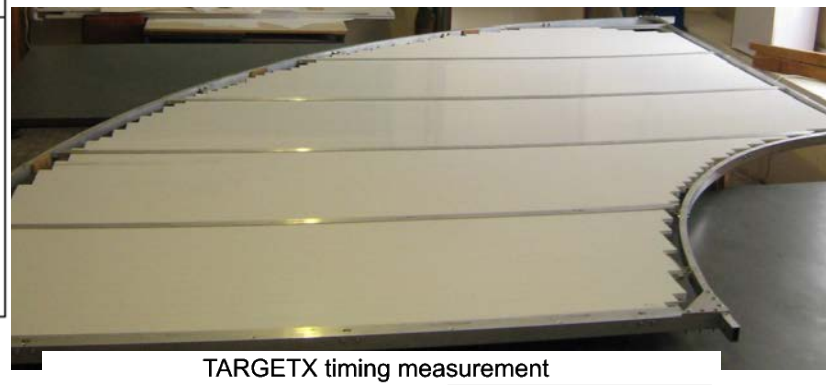


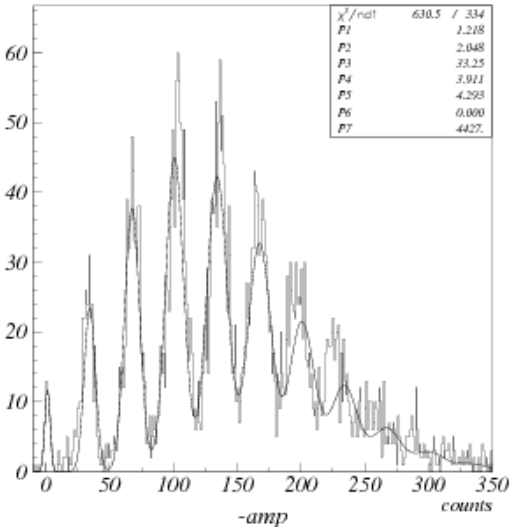
- First production batch of 6k ASICs (~100k chan) started
- ALPHA configuration baseline approved, construction started
- 2023 first light (2026 complete) – though eruption in north

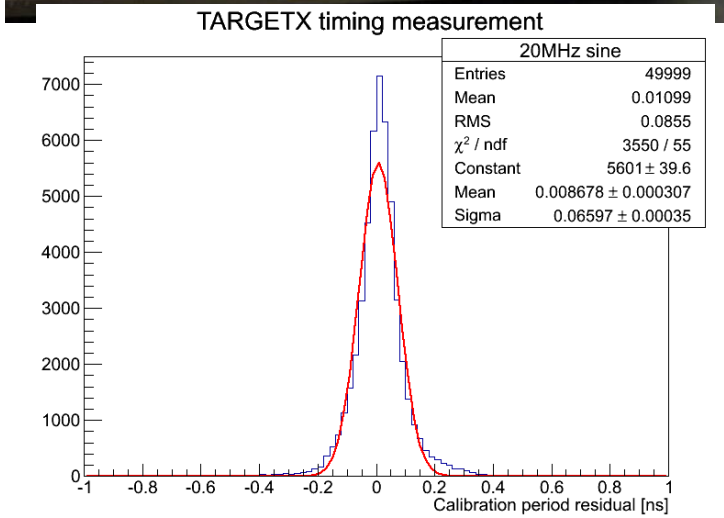
Belle II iTOP and KLM: IRSX, TARGETX

- **Leveraged decade of development for PID and Muon readout**









< 0.1 ns

- **IRSX 8-channels, 32k samples/channel**
- **8k channels of MCP-PMT readout**
- **30kHz L1 trigger rate (5.2us L1 delay)**

- **TARGETX 16-channels, 16k samples/channel**
- **23k channels of Si-PMT readout**
- **$1.40/channel**

APT: ALPHA

- **Lower power, higher density readout (ganging readout/FPGA)**

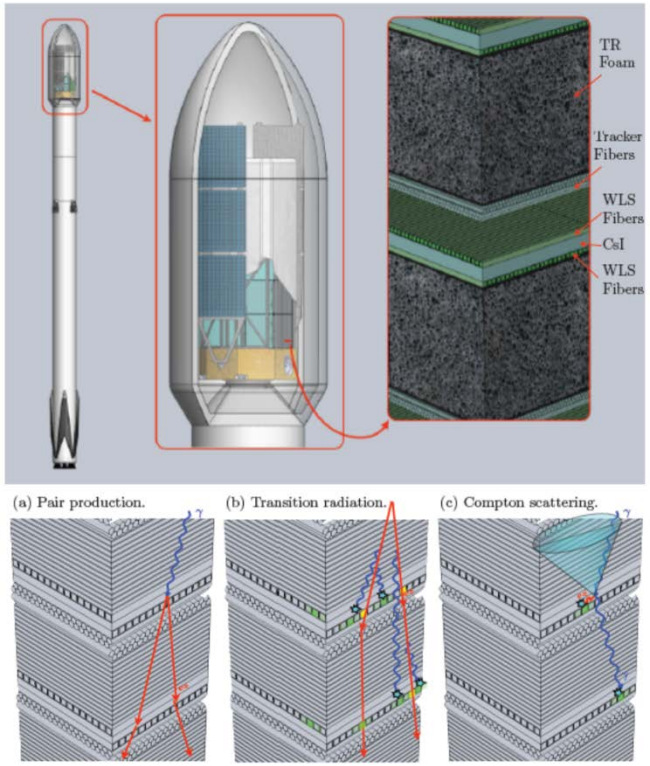
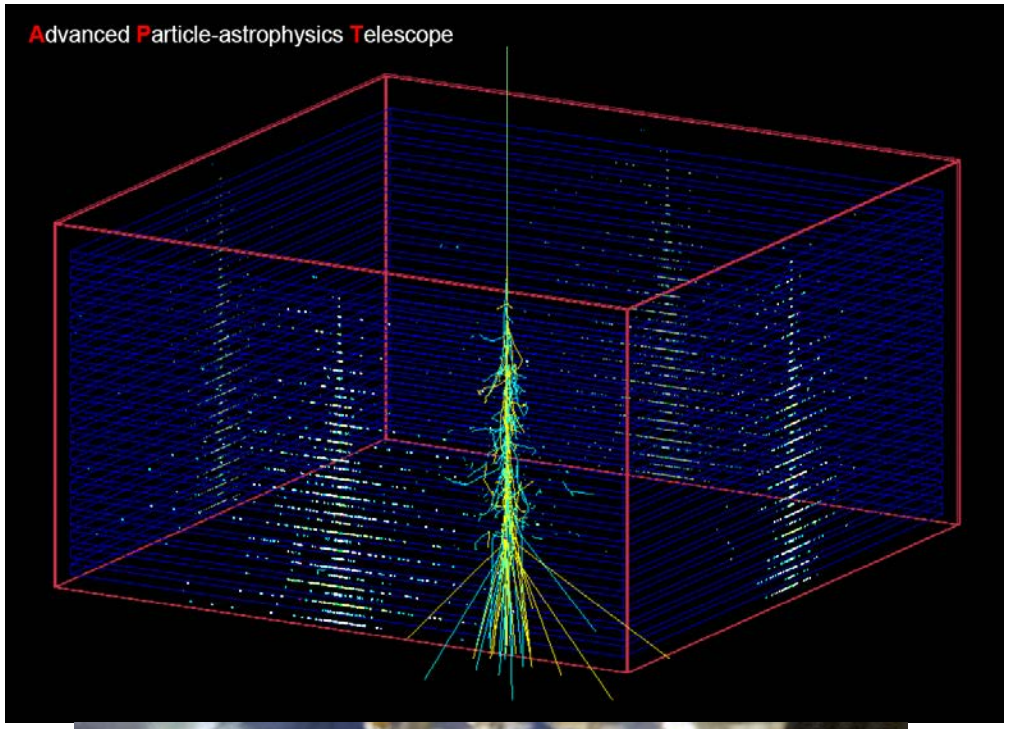
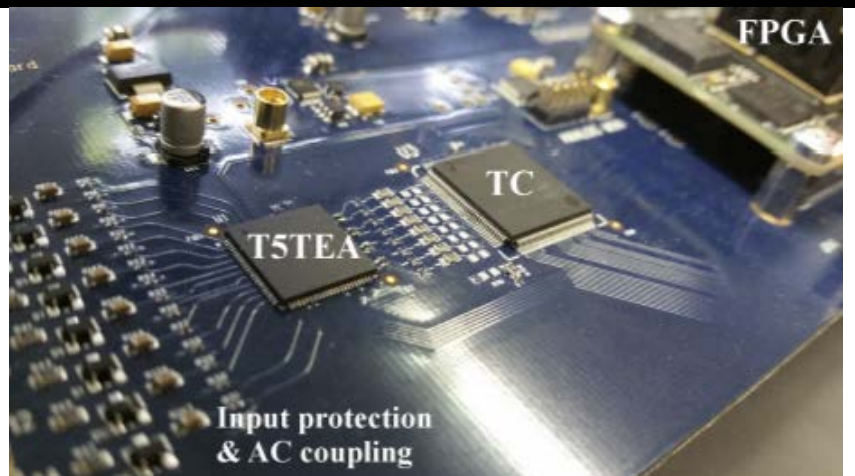


Figure 1: *Top: APT in Falcon-9 faring. Bottom: APT detection modes.*





Baseline design: 380,000 channels (needs to be low power – happy with TARGETC + T5TEA functionality)

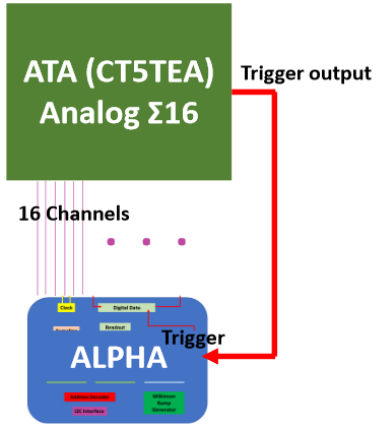
- **Triggering seems fine**
- **"hang" more digitizers from a single FPGA (data is sparse)**
- **No central front-end trigger**

ALPHA Readout Concept

Use existing Cherenkov Telescope Array trigger ASIC (tweaked to have an analog sum-of-16 trigger) and operate digitization of each ALPHA independently.

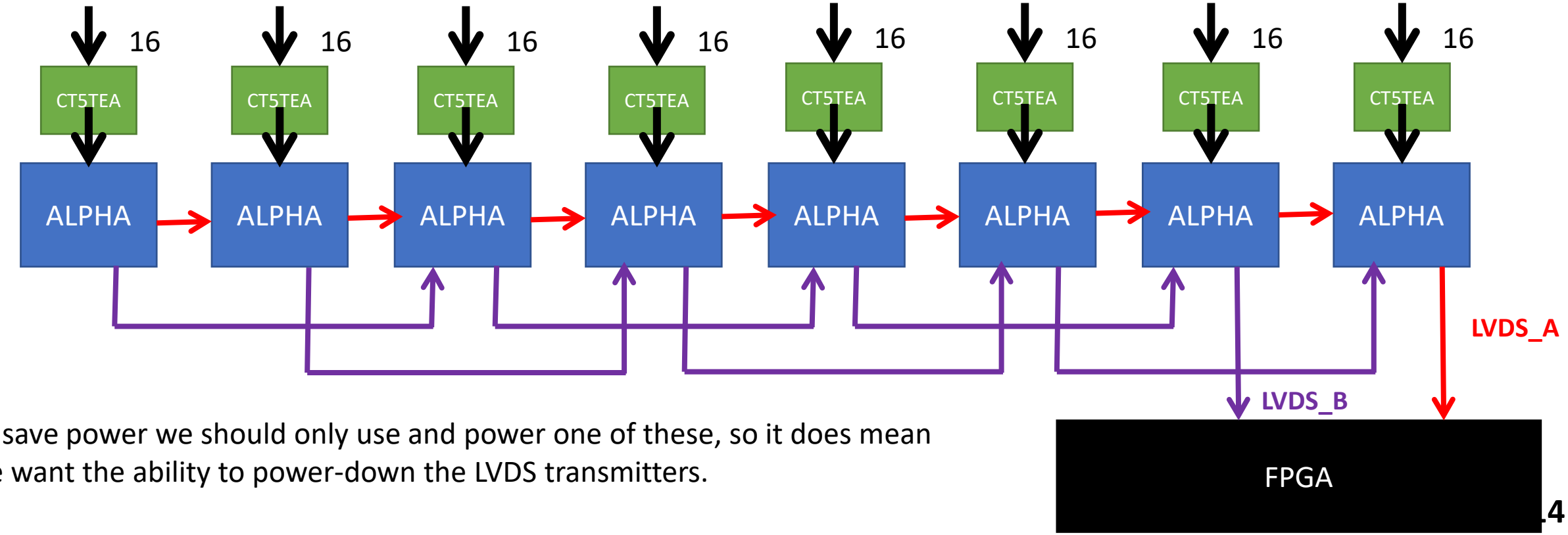
Maximize the number of ALPHA served by a single FPGA (power, I/O limits)

In theory, 64 chains * 32 ALPHA * 16 channels ~ 2^15 channels/FPGA



ATA
1. Triggering
2. Vped offset

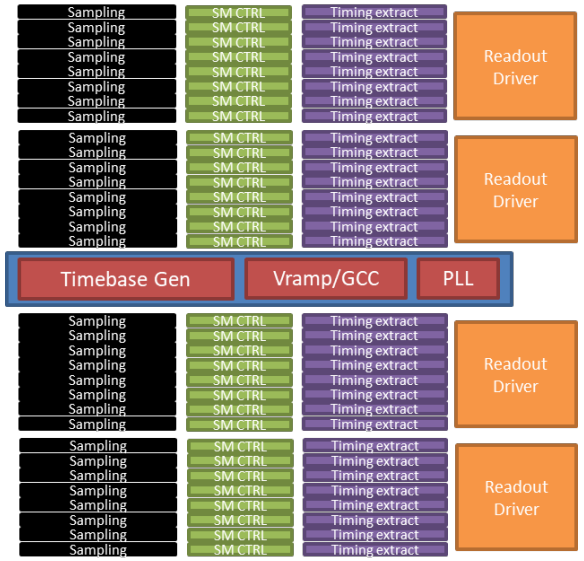
One ATA for one ALPHA



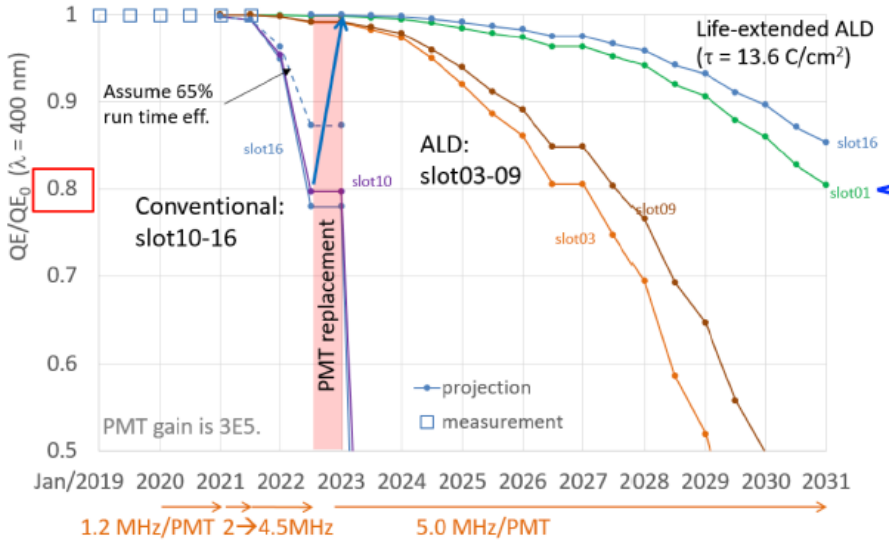
To save power we should only use and power one of these, so it does mean we want the ability to power-down the LVDS transmitters.

GULFstream Overview (iTOP motivation)

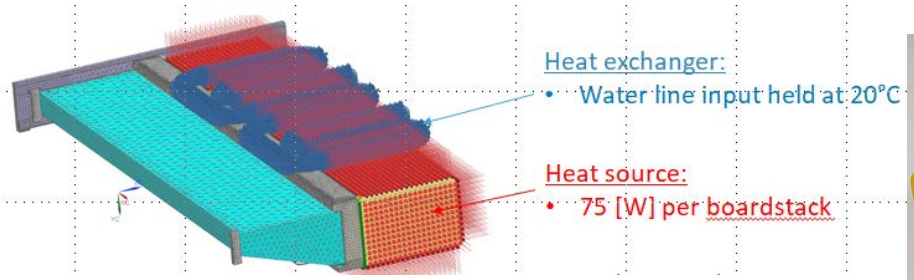
- **Much more compact, lower power**
- **No long storage depth – digitize and ship all hits**
- **GULFstream Features**
  - 32 channels
  - 4x deep, 64 sample SCA
  - 4x Gbps data links (8ch/link)
  - 32 bit words (3 chan, coarse/fine time)
  - Hit streaming: 3.2 Mhits/s/chan
  - Each channel operates independently
  - ~100ns/6-bit conversion
  - Direct feature extraction
  - No pedestal acquisition
  - To user, looks like a TDC
  - Low power/channel (exact savings to be confirmed)



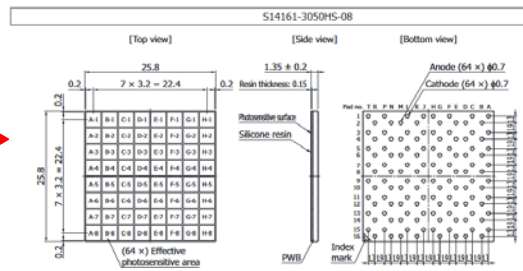
Projection of QE degradation



2.6M$ to replace MCP-PMTs (and 4-5 years!)



Operating @ thermal redline

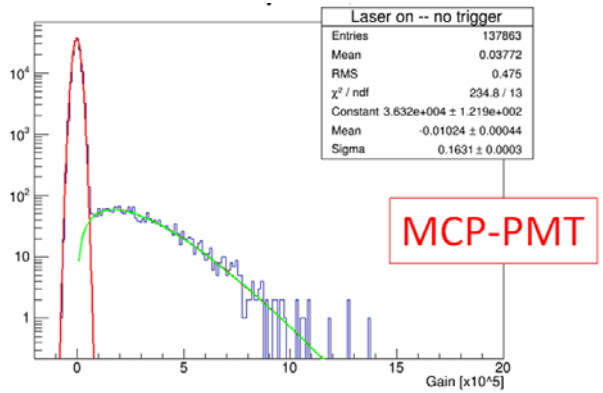


4x more readout channels!

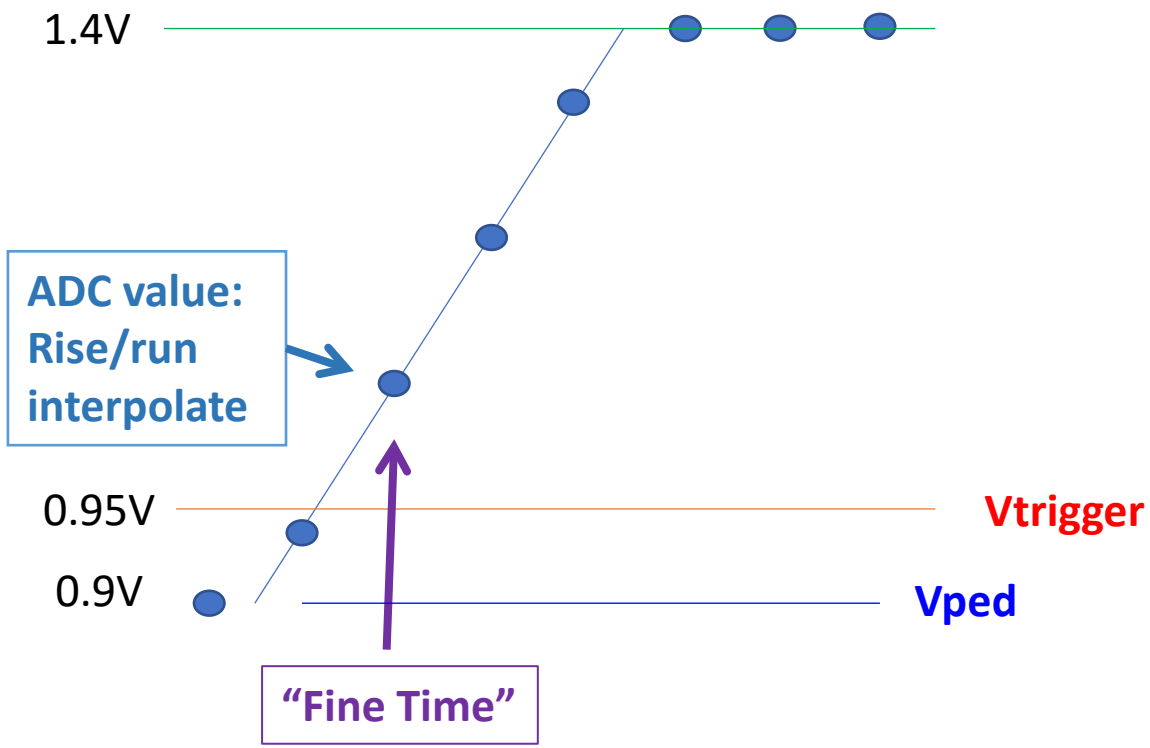
-30C SiPM operation

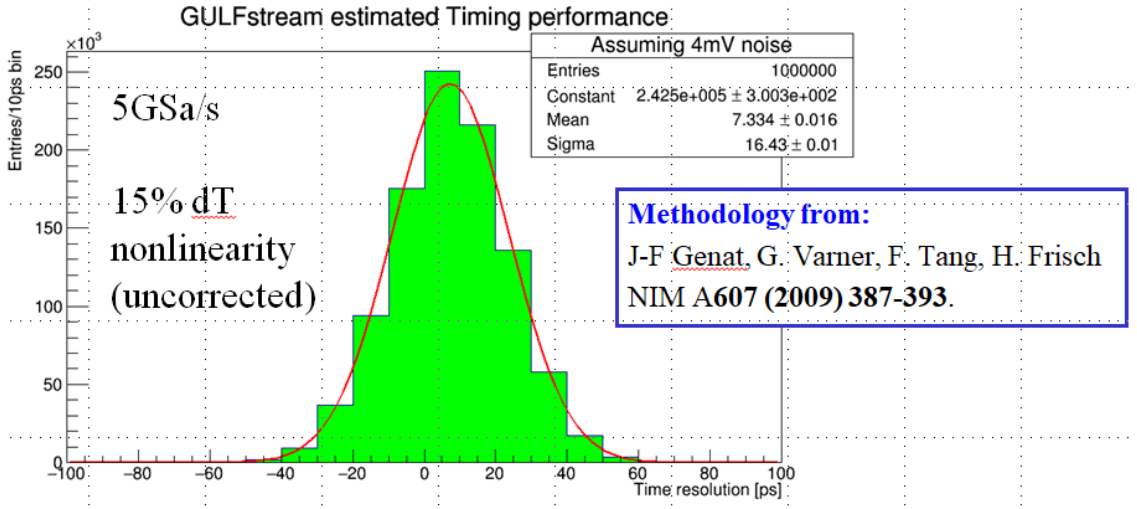
GULFstream Operating Principle

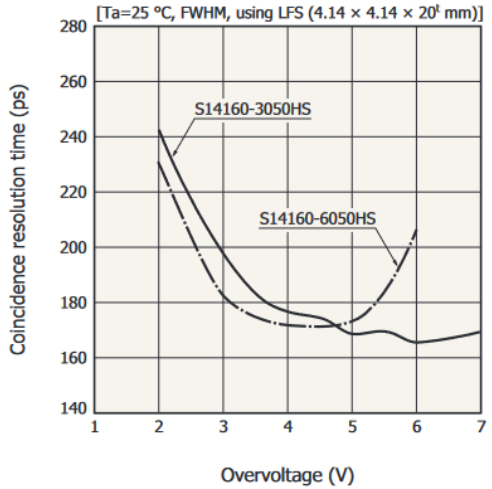
- For MCPs, charge distribution goes all the way to zero
- For SiPMs, quantized; Time to Digital Converter methodology makes sense
- SCA sampling at ~ 4GSa/s; trigger on stored samples; priority encoder time bin
- Target interpolation: 1ns risetime, 0.5V, 64 bit sampling



1.8V process







180ps FWHM ~ 76ps

If 20ps due to ASIC (FTSW limited?)

76ps ➔ 79ps

A summary of ASIC design @ UH

- **High impact from a tiny group; physically the most isolated in the world**
- **Didn't mention all of the endeavors (such as Q-Pix, GRAPH, …)**
  - ❖ **(nor any CAP (MAPS) pixel activities)**
- **Students and Postdocs have made a huge impact**

- **The latter also realized the goal of commercializing the technology (Nalu Scientific)**

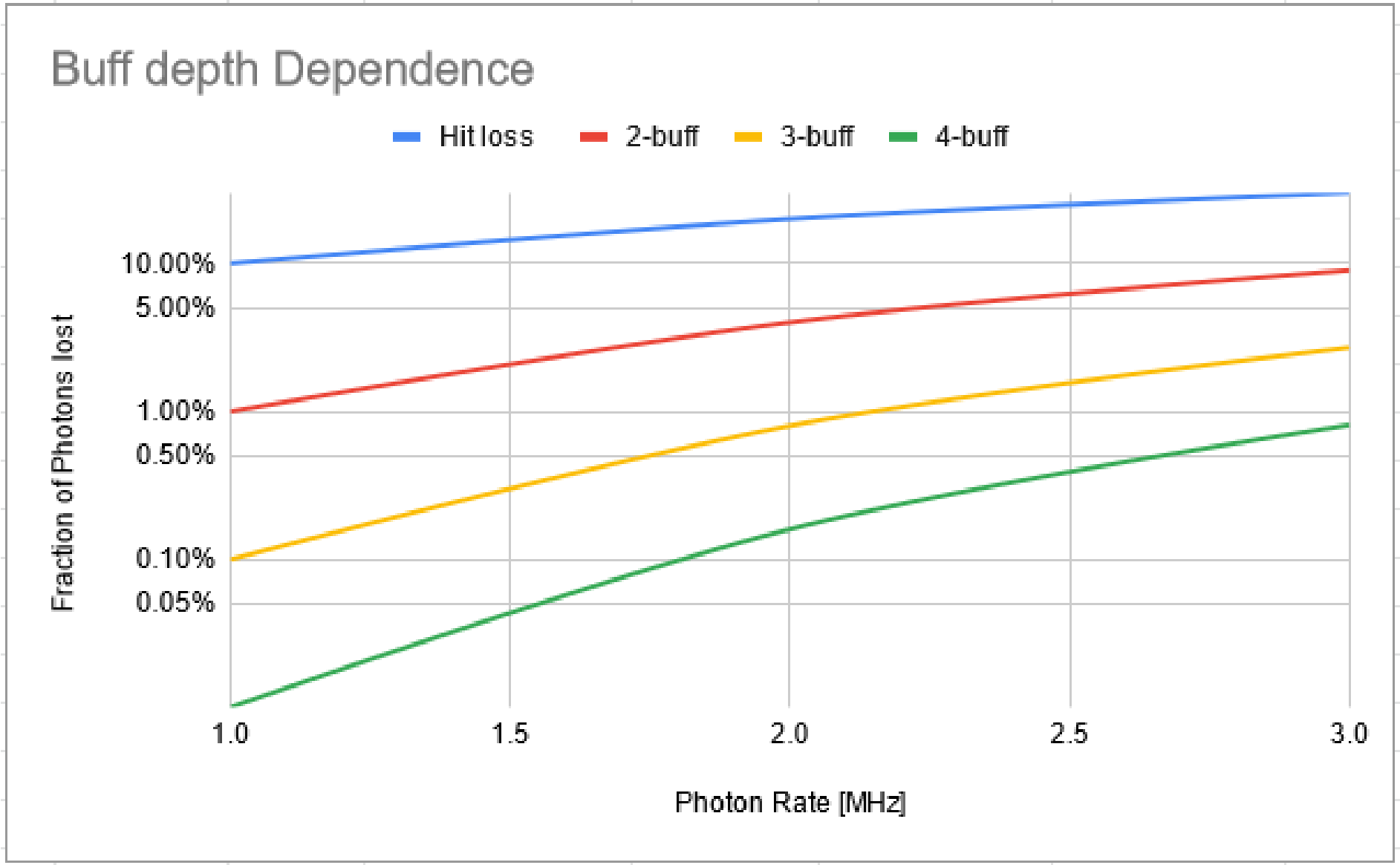
- **Opportunities: we expect to be recruiting for an Instrumentation Frontier faculty position soon**

Backup Slides

4-Deep Bank Buffering

- **Single bank suffers too large hit loss**

<1% @ 3MHz



Layout basically finished… 5x5mm with space