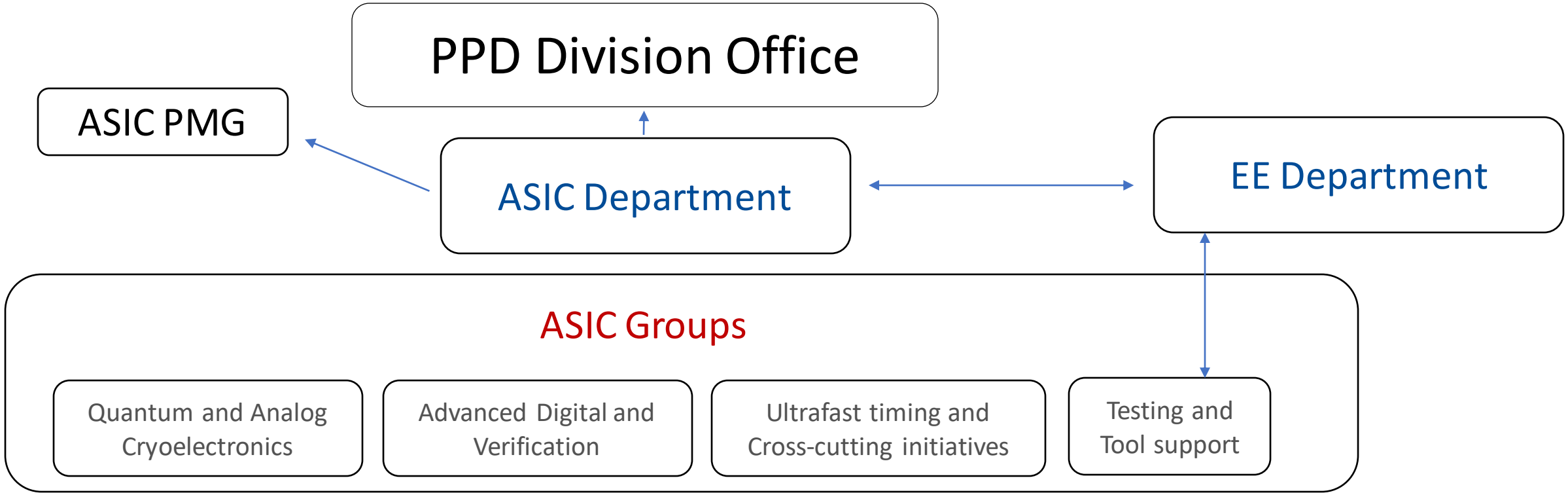
ASIC R&D Department

Farah Fahim & Jim Hirschauer

HEPIC workshop

May 18, 2022

Department Structure



- 19 ASIC designers (2 JA)
- 1 PhD/ 1 MS EECS student (Northwestern University)
- 1 scientist
- 2 Application Physicist
- 1 test engineer, 1 engineering associate

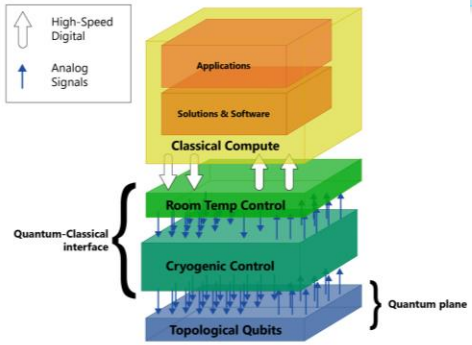
Currently recruiting for 2 more positions
2 ASIC designers – offers extended

5 summer interns - HIRING

ASIC Design at Fermilab

FQI (HEP/ ASCR/DOD/NASA)

SCD (HEP / ASCR)

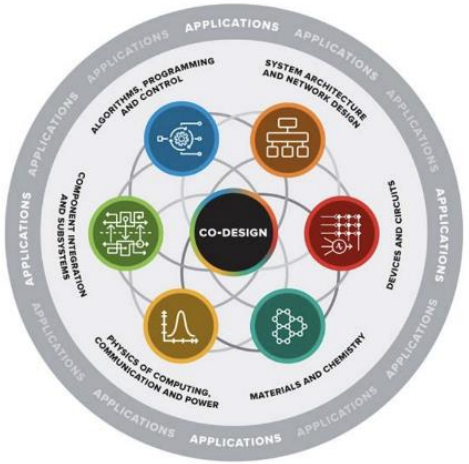


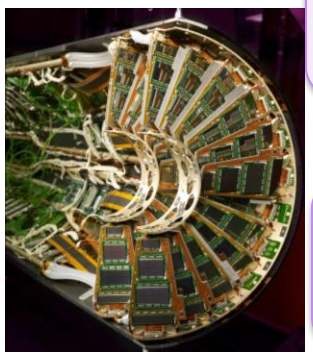
Quantum

Artificial Intelligence

OPTT

Technology Transfer





ND

HEP

PPD

Microelectronics Codesign

PPD, FQI, SCD, AD, etc. (HEP/BES/ASCR/NP/FES)

Fermilab

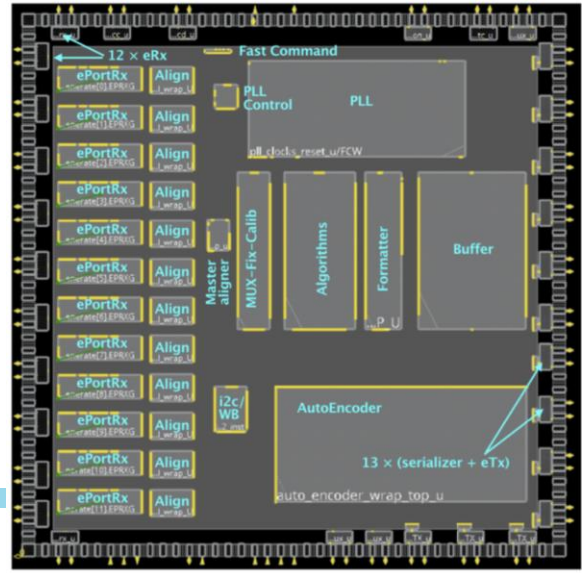
CMS & DUNE : Major deliverables for HEP experiments

Operation in extreme conditions – high ionizing radiation, cryogenic operation with long lifetime requirements

- ECON (T&D): CMS High Granularity Calorimeter Data Concentrator chip for 40 MHz trigger and 1 MHz data path. (Radhard, low power, high data throughput with CERN)

Successful beam tests with excellent radiation performance

- ETROC: CMS Timing layer ASIC for CMS LGAD detectors (picosecond timing chip with SMU). Reticule chip submission FY22
- COLDATA/ COLDADC – Cryogenic DUNE data concentrator and ADC chip (successfully completed in FY 21 with BNL and LBL)
- Other projects include collaboration with RD53, R&D for 28nm, CFD timing chips



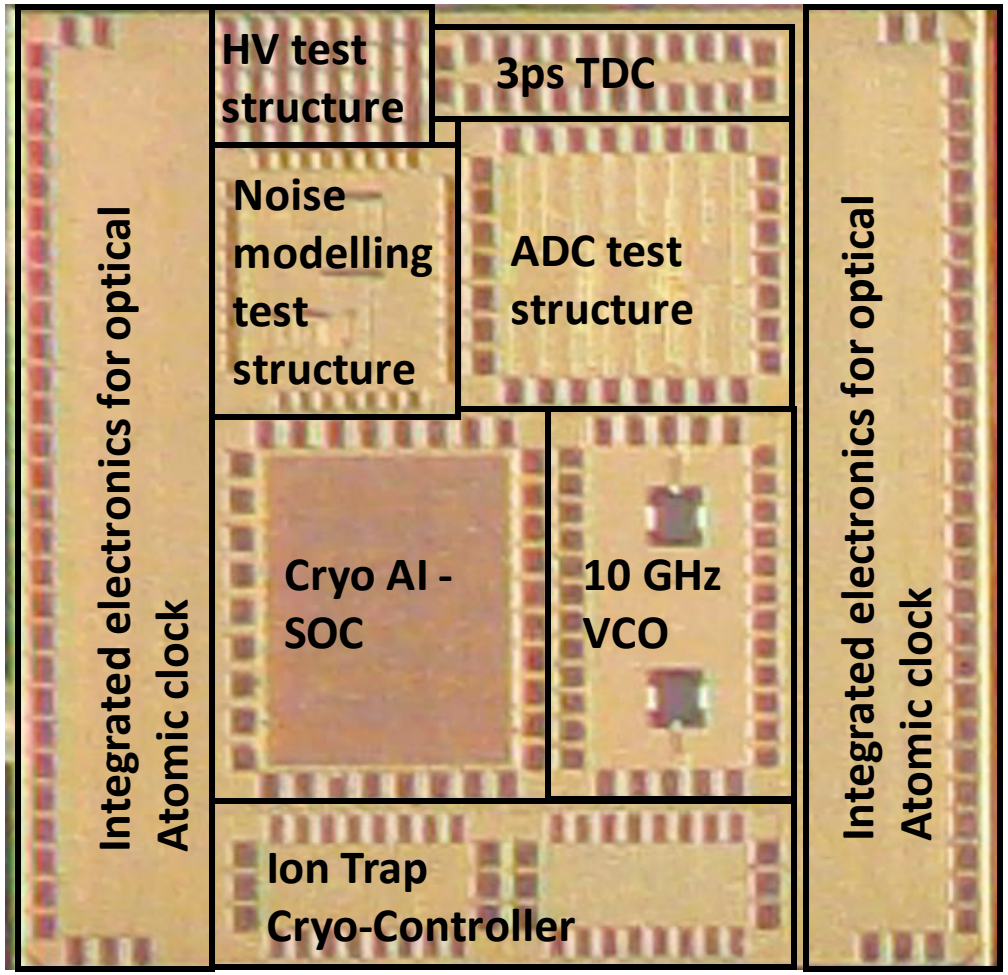
Quantum cryoelectronics projects

Deep cryogenic electronics on advanced technology nodes (GF 22 FDX)

- Cryogenic modelling for development of 4K process design kit for GF 22 FDX with EPFL, Synopsys & GF
- **Quantum Science center** (National Quantum Initiative center led by ORNL)

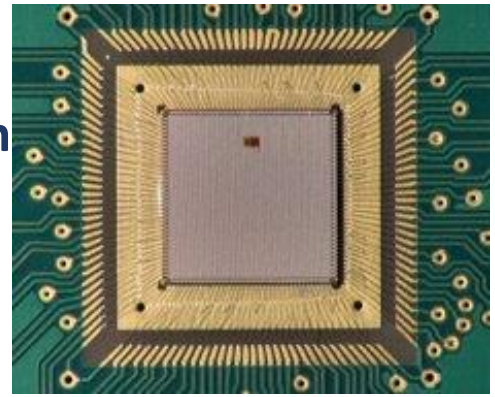
  Ion trap based Quantum Simulator: Cryoelectronics Controller – Low noise, high speed, high voltage DACs
- Compact Optical Atomic Clocks: Room temperature, integrated control **Joint DOE-DOD project** with MIT LL
- High speed cryogenic ADCs at 4K with **Industry**
- Cryo-picosecond TDC for SNSPD readout with JPL and Caltech (Quantum Communication).

Superconducting electronics: TWPAs and JPAs for ADMX-BREAD using a super conducting fab



Fermilab

AI-on-chip – Solve the HEP data challenge



Hardware - software codesign, driven by edge compute: Processing data at source, real-tim feedback and control. Neuromorphic low power architectures with integrated memory

- **1st AI-on-Chip for HEP**: Radhard, Low-power, Low-latency Autoencoder

  ECON-T for HL LHC (with NU & U.Columbia) **(7-20x data compression: 48 pixel)**

  Working with Siemens/ Mentor Graphics (hls4ml) for enhancing tools with radhard capability

  Tested and working well !!!!

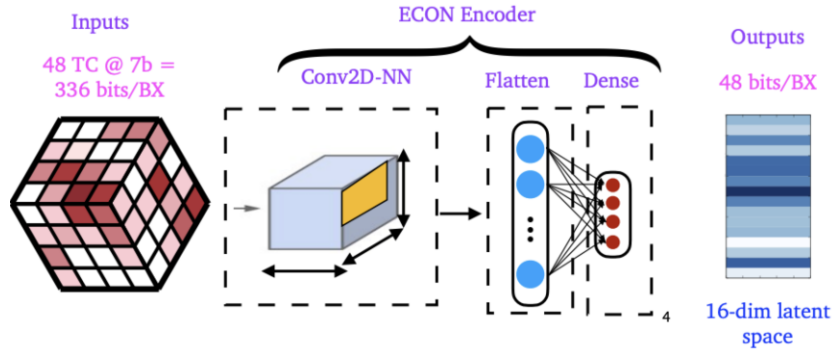
SIEMENS

Mentor Graphics

- AI-in-Pixel: **Data processing at source**

  In-pixel PCA + Autoencoder **(30x - 80x data reduction: 1024 pixel)**

  Both HEP and Photon Science/ BES Applications with Northwestern University



- Cryo AI: Anomaly detector/Quantum ML for controls and readout

  Ultra-low power system cryogenic control for a closed loop system

  RISC V processor and Network on chip (**Integrated and Verfied using ESP)**

- Embedding FPGAs on detector: Radhard/ cryogenic eFPGA on-chip – with Flex Logix (22nm 28nm)

Northwestern University

Columbia University

Pixel Detectors for dark matter, neutrinos, light sources

Gigapixel/ Megapixel camera systems – high resolution, low power, operating in extreme conditions

- Readout of Skipper CCD (Dark matter detection OSCURA)

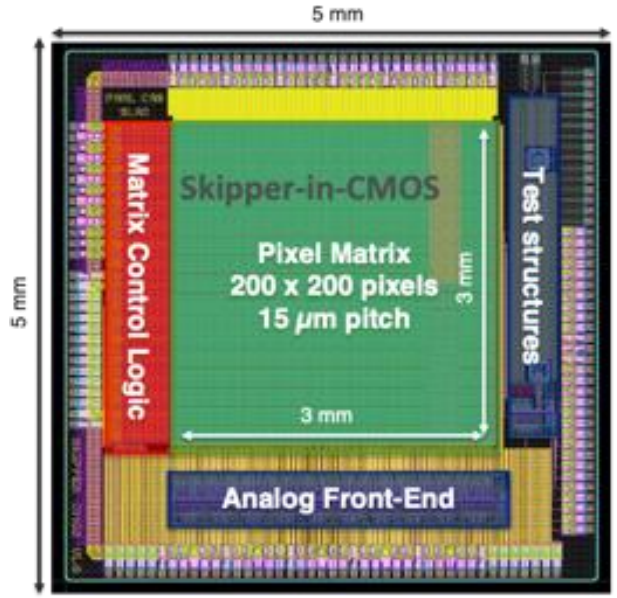
  MIDNA: Low Noise readout of CCDs (Corelated multi sampling amplifier with analog averaging). **Recently demonstrated single photon counting!!**

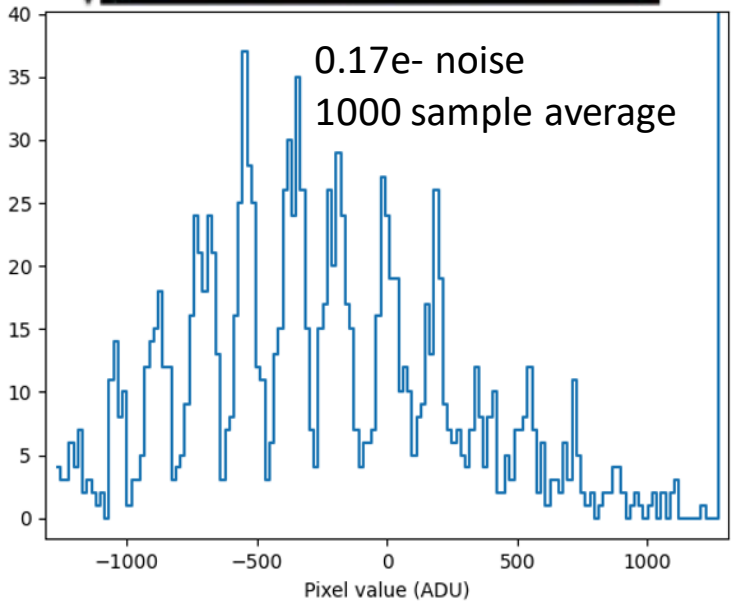
- **Co-design of integrated sensor and readout electronics**

  Skipper CCD in CMOS – collaboration with SLAC and Tower Semiconductor

  Ultrafast skipper CCD (SiSeRo) – collaboration with MIT LL (high gain, high speed, non-destructive readout)

- Qpix: R&D for fully-pixelated readout of DUNE's far detector LArTPC with U.Hawaii, U. Penn & UTA





Fermilab

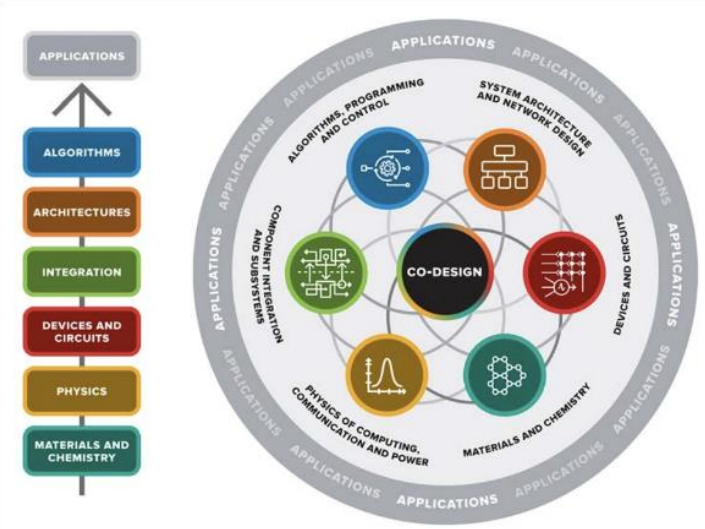
New DOE Microelectronics Initiatives

DOE Microelectronics Codesign Teams:

"Hybrid cryogenic detector architectures for sensing and edge computing enabled by new fabrication processes"

Fermilab led jointly funded by HEP + BES + ASCR + FES

- Massively parallel readout for x1000 speed improvement of Skipper-in-CMOS: SPROKECT
- Development of rad-hard particle detectors based on superconducting nanowires for fast timing (EIC)
- CryoCMOS and beyond-CMOS superconducting electronics for edge computing
- Cryogenic system integration for scaling



CMOS and beyond CMOS for rad-hard neural networks

- Rad-hard Neural Network for front-end data processing
- Beyond-CMOS: Blue Sky R&D
- CMS Phase III Pixel detector R&D (TSMC 28 nm)
- Working in conjunction with **ORNL-led codesign team - ABISKO**

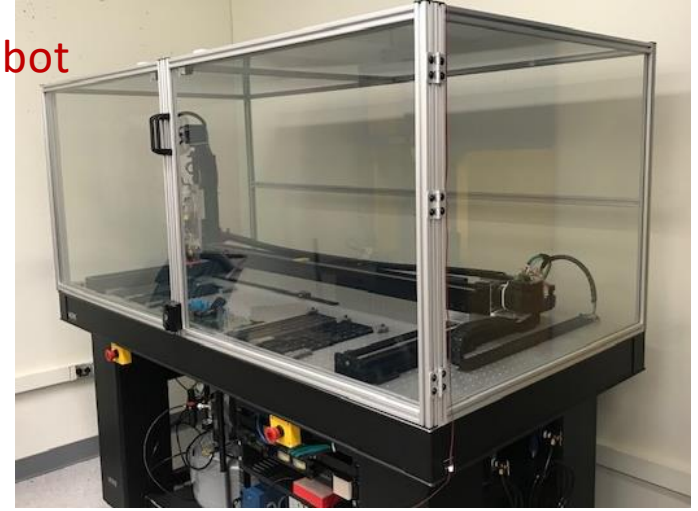
Abisko Codesign

OAK RIDGE National Laboratory, Sandia National Laboratories, Arizona State University, Georgia Tech, HARVARD UNIVERSITY

Collaborator: Fermilab

ASIC Testing and Tools

New ASIC Robot



- **New ASIC Testing Robot**

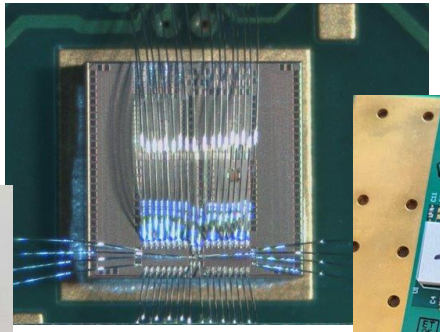
High throughput testing capability: 3000 chips / week

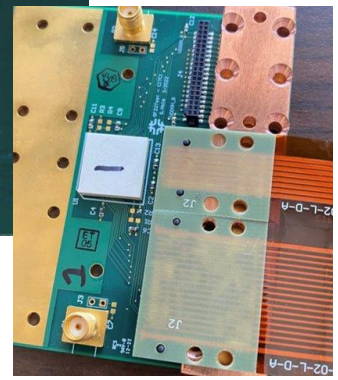
LabVIEW Vision for part alignment

  - Fine adjustment of position based on part or tray image.
  - Completely reproducible after power cycles

Michigan ATLAS TDC ASICs

Test ECONs for CMS Upgrade (75,000 parts)

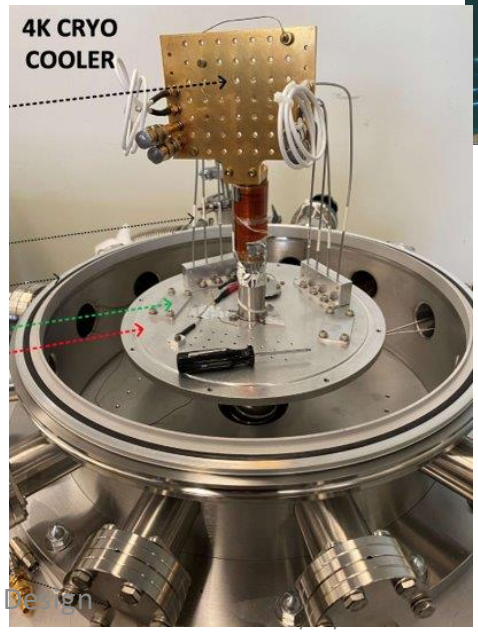




- **DUNE Cold_ADC V2 and COLDATA V3 ASICS (77K)**

  Successfully completed

- **Deep cryogenic testing underway (4K)**



- **ASIC CAD tools support**

  ASIC software tools and design kit support

  New Service Desk for ticket support