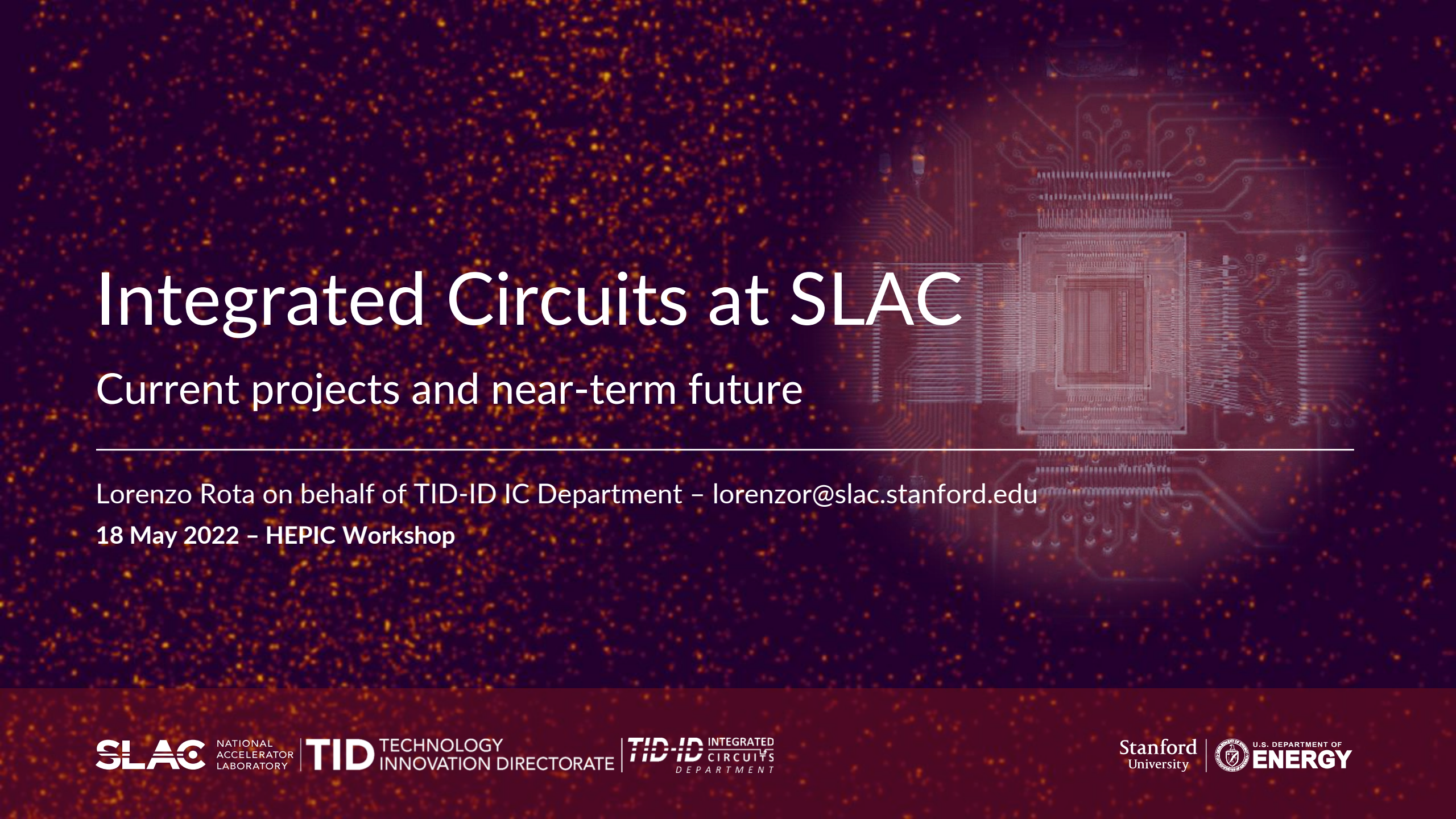


Integrated Circuits at SLAC

Current projects and near-term future

Lorenzo Rota on behalf of TID-ID IC Department – lorenzor@slac.stanford.edu

18 May 2022 – HEPIC Workshop

SLAC NATIONAL ACCELERATOR LABORATORY | TID TECHNOLOGY INNOVATION DIRECTORATE | TID-ID INTEGRATED CIRCUITS DEPARTMENT

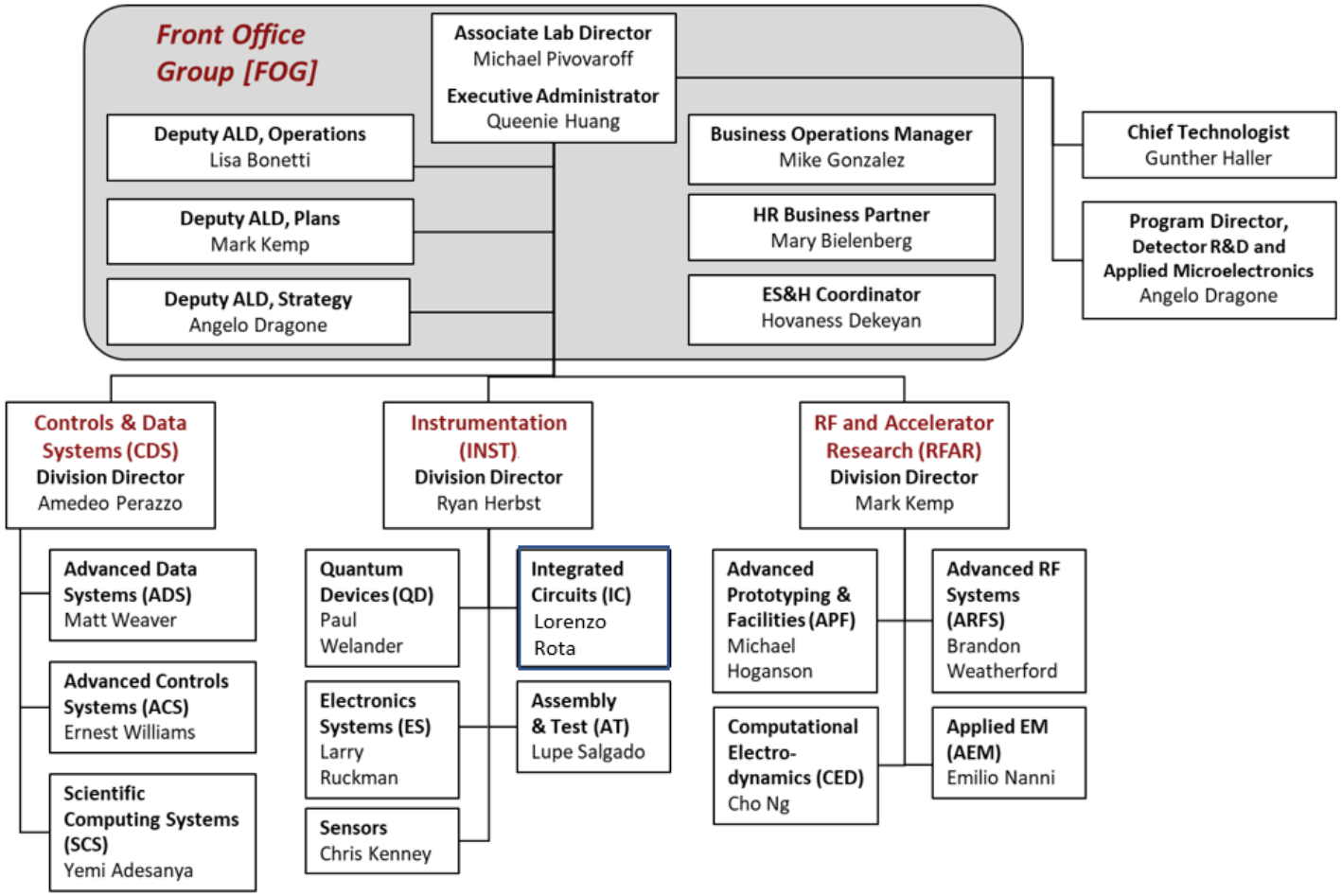
Stanford University | U.S. DEPARTMENT OF ENERGY


San Francisco Bay
Stanford
LCLS beamlines
IC Team
LCLS accelerator

Integrated Circuits @ SLAC

The IC team:

- 7 designers with complementary expertise:
  - Dieter Freytag
  - Bojan Markovic
  - Aldo Pena Perez
  - Aseem Gupta
  - Lorenzo Rota
  - Mohit Sharma
  - Alexandre Habib
- +2 positions being filled (1 analog/mixed, 1 digital)
- +2 visiting/student year

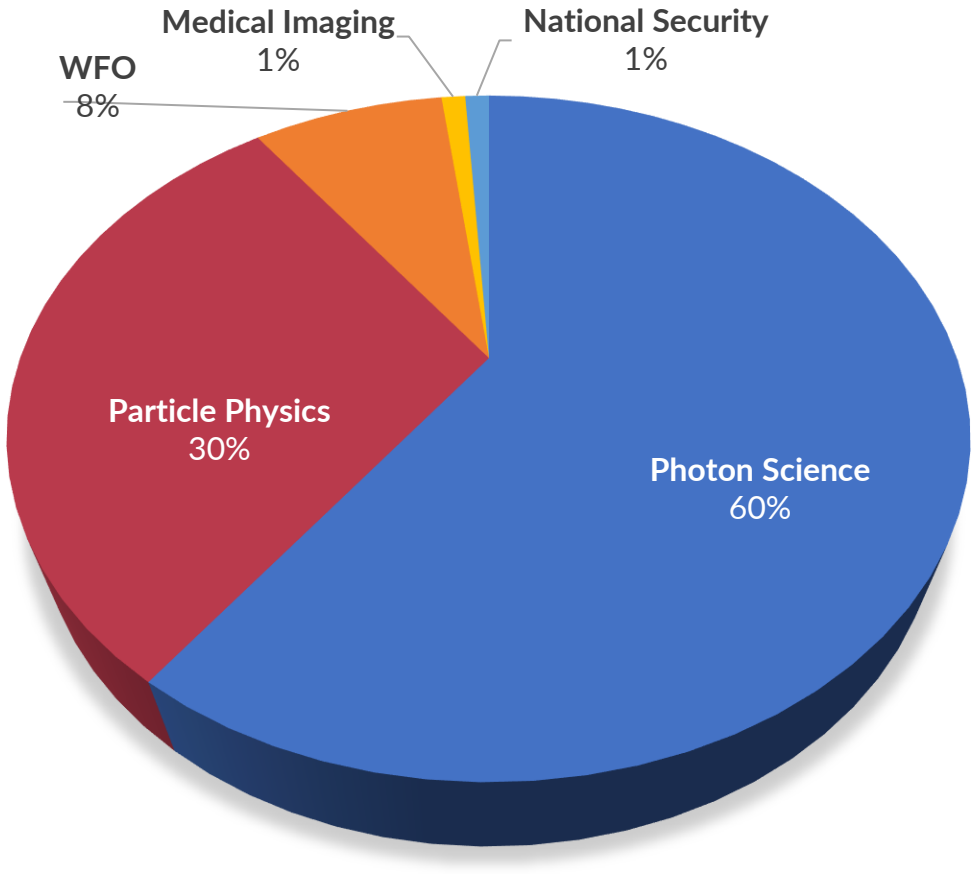


Areas of research

- Particle physics:
  - 5 R&D projects currently funded by KA25 program
  - Development of SoC for nEXO charge readout
  - Collaborations with other institutes (*e.g.*, ALTIROC)

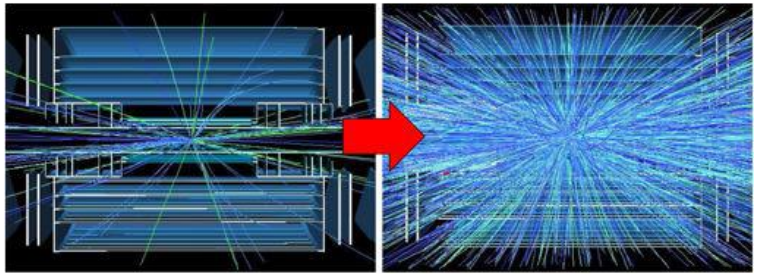
- Strong detector development program to deliver science-ready cameras for LCLS-II:
  - X-ray imaging: ePix, SparkPix families
  - Timing: Tixel (SparkPix-T)

- Collaboration with local start-ups and companies (WFO)
- Medical imaging
- National security



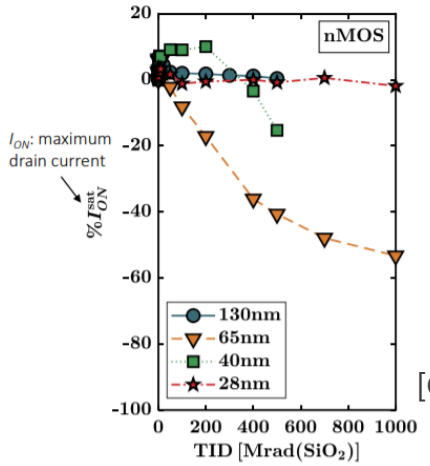
Distribution of projects over past 10 years

4D Tracking on 28 nm



- **Application:** Future High Energy, High Luminosity Colliders
  - High Luminosity → Pileup → Solution: precision timing to distinguish between collisions occurring close in space but separated in time
  - HL-LHC will produce 200 simultaneous pp interaction on average
    → Both ATLAS and CMS will incorporate dedicated fast-timing detector layers (HGTD & ETL) for HL-LHC
  - A future 100 TeV pp collider will produce 1000 nearly simultaneous pp collisions
    → **will require full integration of timing with the 3D spatial information of pixel detectors → 4D Tracking**

- **Technology:** CERN's EP R&D WP5: IC Technologies survey [1] has promoted the selection of 28nm CMOS node as the next step in microelectronics scaling for HEP designs.
  - 4-5X higher density compared to currently used 65nm
  - >2X faster compared to 65nm
  - Better radiation hardness than 65nm (preliminary studies [2])



[G. Borghello, CERN]

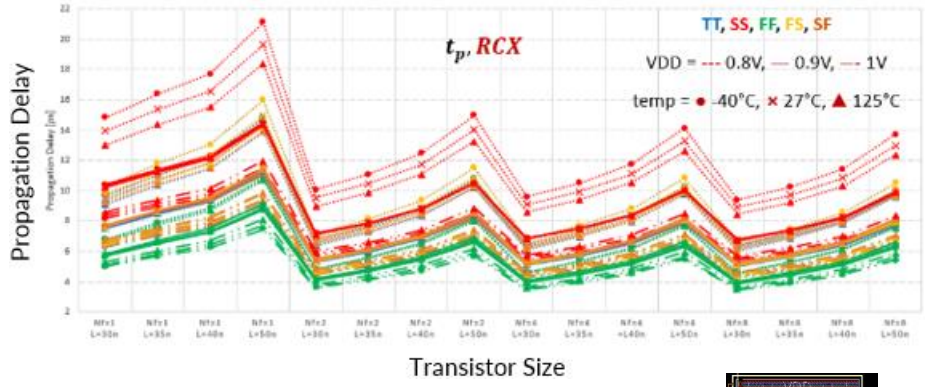
[1] Strategic RD Programme on Technologies for Future Experiments - Annual Report 2020. Technical Report CERN-EP-RDET-2021-001, CERN, Geneva, Apr 2021.

[2] Giulio Borghello, "Ionizing Radiation Effects On 28 nm CMOS Technology". Technical report, CERN, Geneva, May 2020.

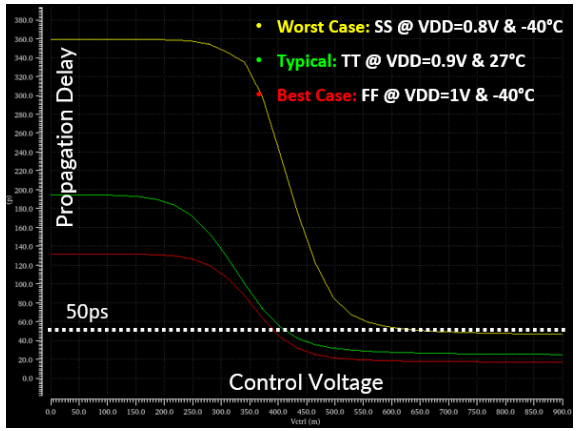
4D Tracking on 28 nm

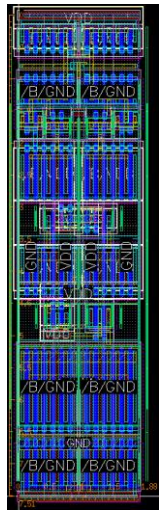
- One of the critical circuit blocks necessary to enable 4D operation in trackers is high-precision **Time-to-Digital Converter** (TDC) → Design in progress:

  - ❑ Evaluation of technology timing properties:

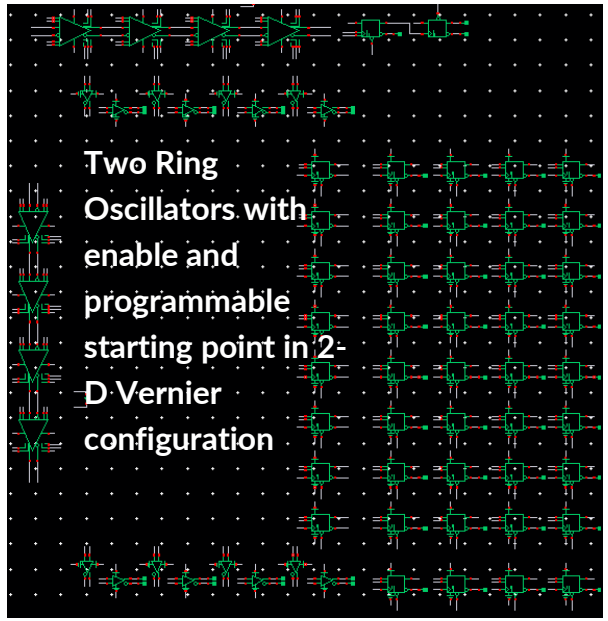


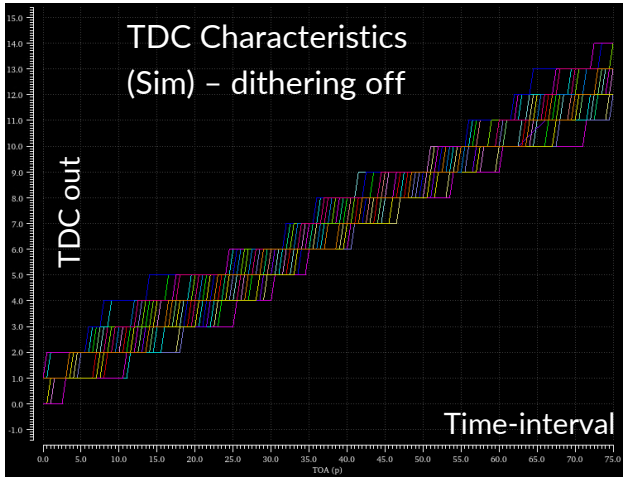
  - ❑ Voltage-Controlled Delay Cell Design:

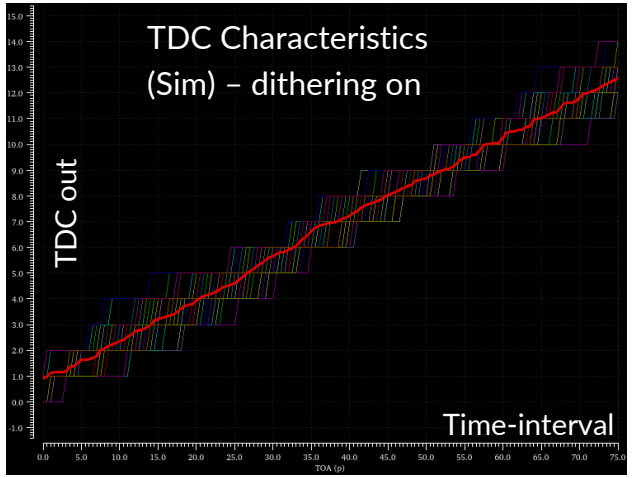




  - ❑ TDC Architecture:
    - Coarse resolution: 50 ps
    - Fine resolution: 6.25 ps
    - Range: 8+ bits
    - Implements dithering for linearity improvement



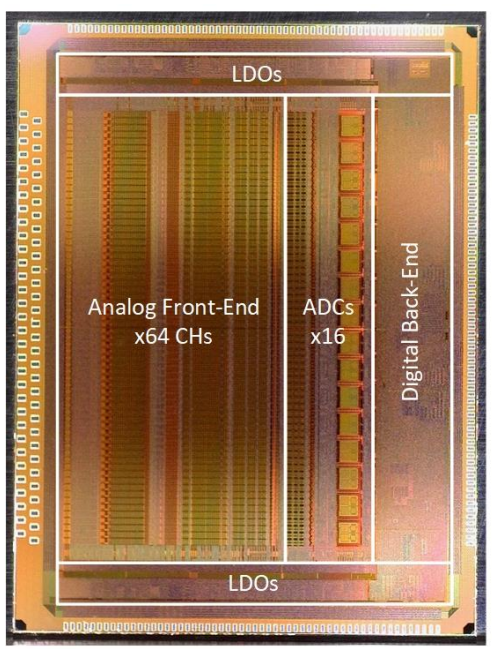


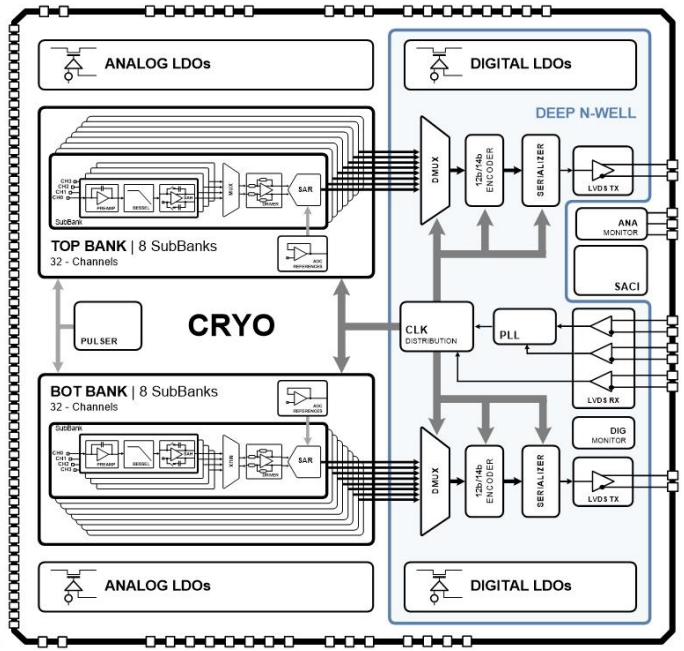


CRYO ASIC

System-on-chip (SoC) charge readout for noble liquid TPC experiments

- **Architecture with combined analog & digital functions**
  - Signal pre-amplification with channel multiplexing, A/D conversion, encoding, and serialization
- **Optimized for cryogenic operation (i.e., LAr - 87 K, LXe - 160 K)**
  - Chip designed using custom models developed at SLAC
  - Characterization of 130 nm CMOS at cryo temperatures
- **On-chip supply regulation**
  - No external active components (low background)
- **Small chip size (7 mm x 9 mm) with a minimal number of I/Os**
- **Power scaling mode to reduce overall power consumption**
- **Designed for reliability and testability**



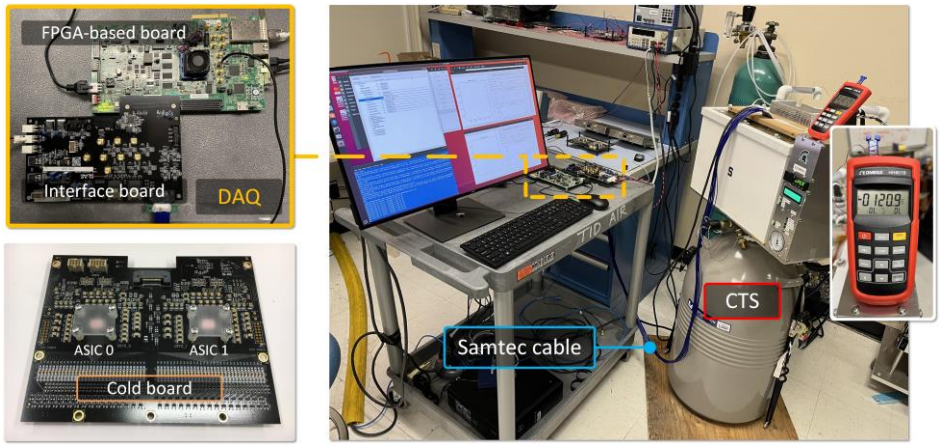


Chip Size: 7mm x 9mm

CRYO ASIC

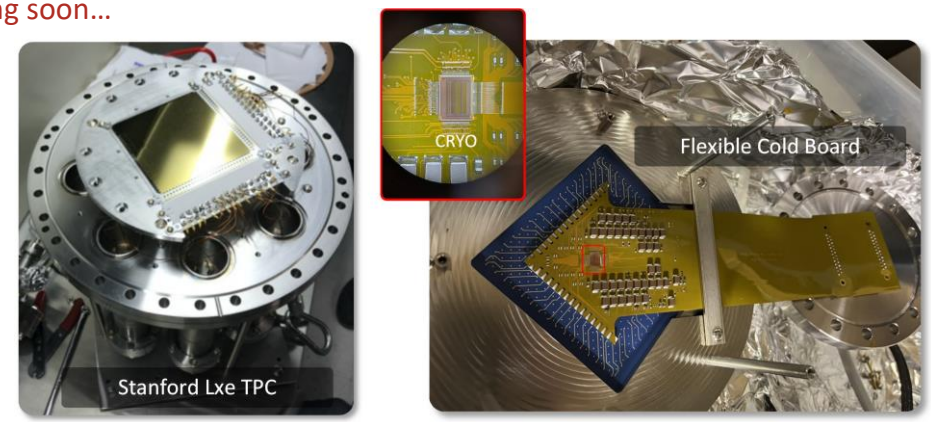
Test bench setups

System at SLAC - Characterization in LN2 (liquid or cold gas)

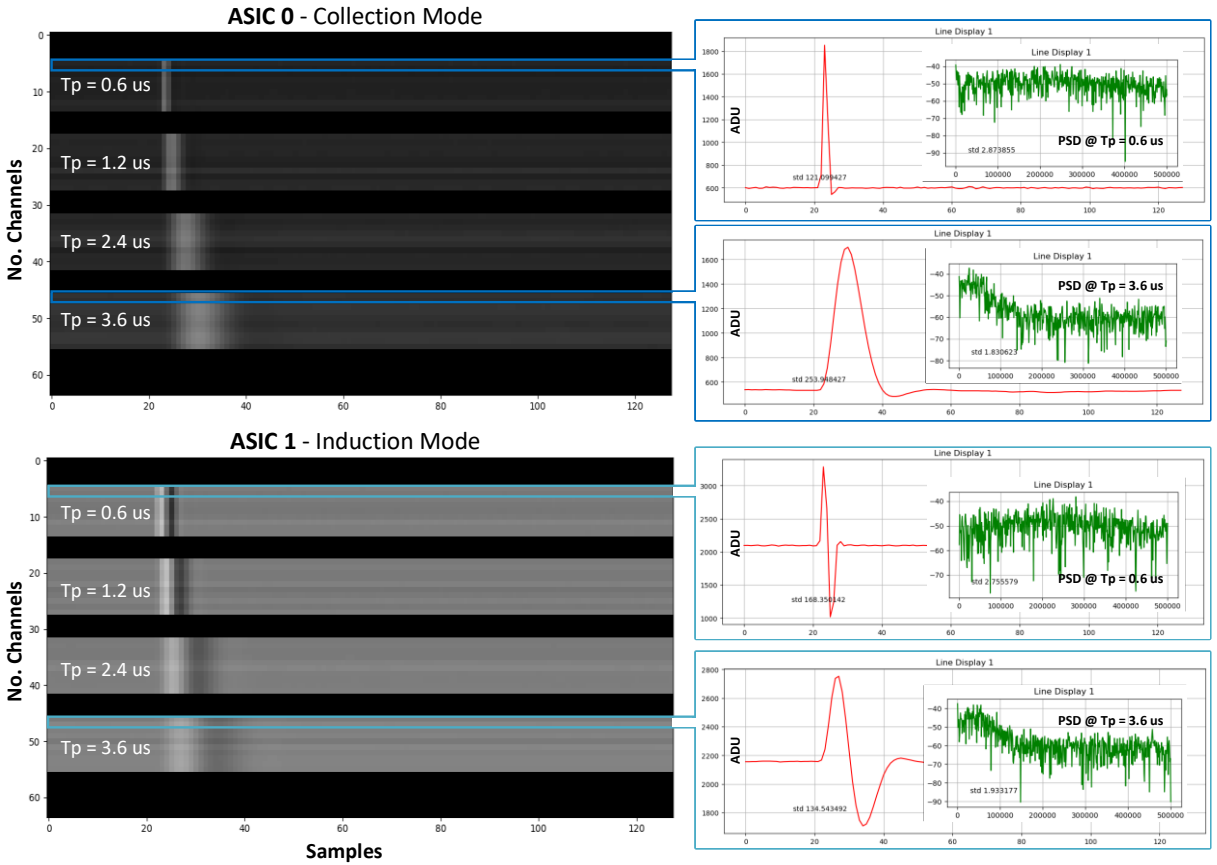


System at Stanford - Characterization in LXe

coming soon...

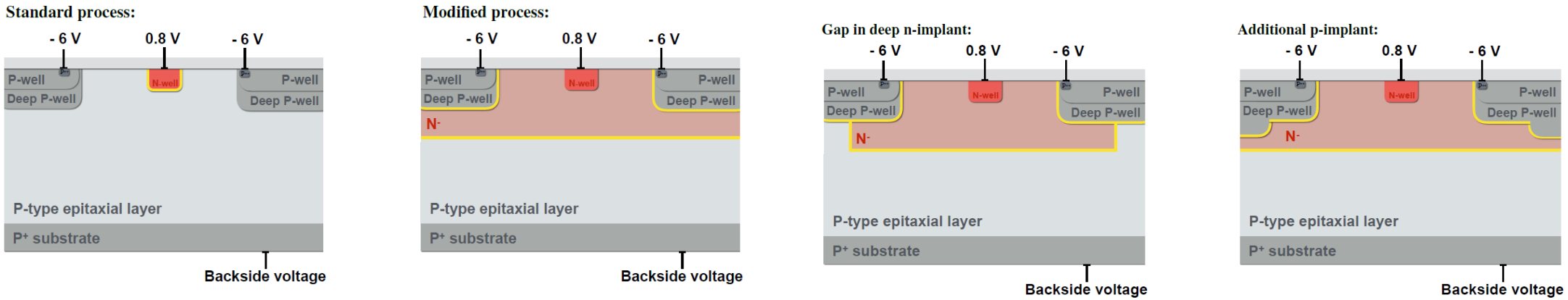


Example results at 160 K (LN2 in cold gas)



MAPS on TowerJazz 65 nm

- New technology for MAPS has recently become available through CERN:
  TowerJazz-Panasonic (TPSCO) 65 nm CMOS imaging process with modified implants
  - Supports stitching: enable wafer-scale MAPS
  - Deep sub-micron CMOS process: enables new architectures with more functionality and unprecedented performance
  - Sensor optimization in the TJ180 process shows radiation hardness up to 10^{15} n_{eq}/cm^2, time resolution < 2ns with uniform charge collection efficiency across the pixel of size 36.4 µm x 36.4 µm with a small sensor capacitance [1][2].
  - The know-how developed for the TJ180nm process is used and adapted to the TJ65 nm process.



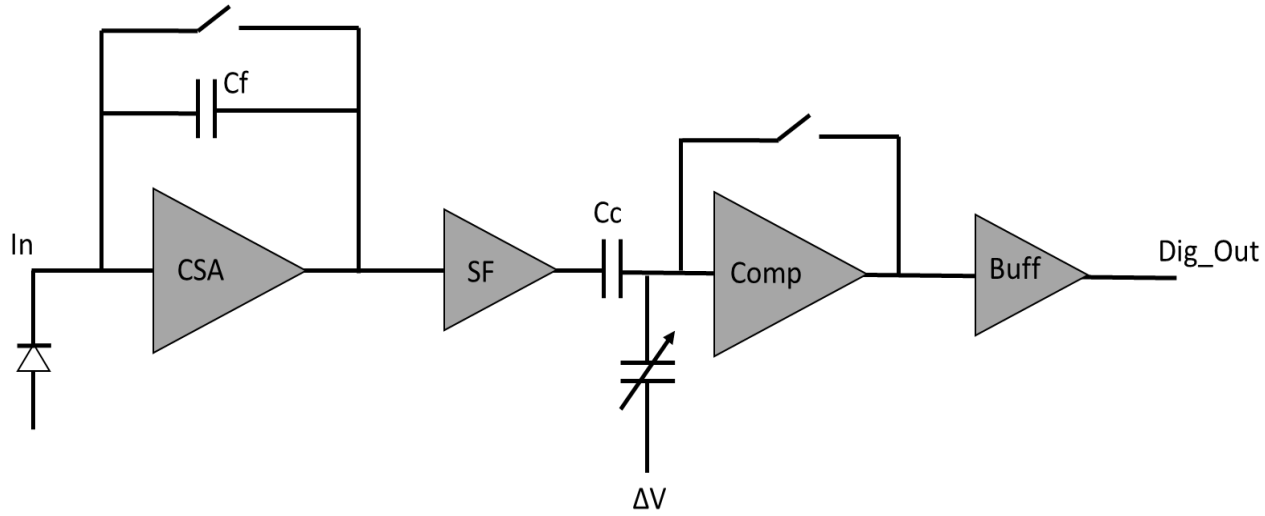
Sensor optimization in TJ180 nm process

[1] M. van Rijnbach et al., *Radiation hardness and timing performance in MALTA monolithic pixel sensors in TowerJazz 180 nm*, 2022 *JINST* C04034

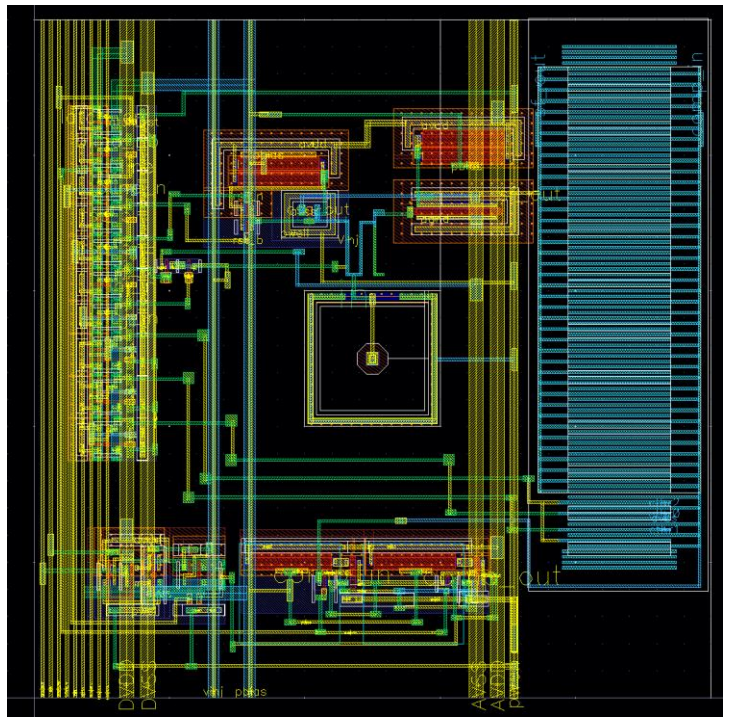
[2] M. Munker et al., *Simulations of CMOS pixel sensors with a small collection electrode, improved for a faster charge collection and increased radiation tolerance,* 2019 *JINST* 14C05013

MAPS on TowerJazz 65 nm

- SLAC joined the WP1.2 from CERN, with ALICE ITS3 upgrade as main driver
- Prototype small pixel matrix designed at SLAC for future linear collider detectors with low duty cycle, in particular tracker and EMcal
- Pixel: CSA with a synchronous reset, Auto-Zero comparator allowing Correlated Double Sampling in the pixel.
- The architecture is optimized for a small detector capacitance of 2-3 fF
- To be submitted on May 2022 MPW organized by CERN



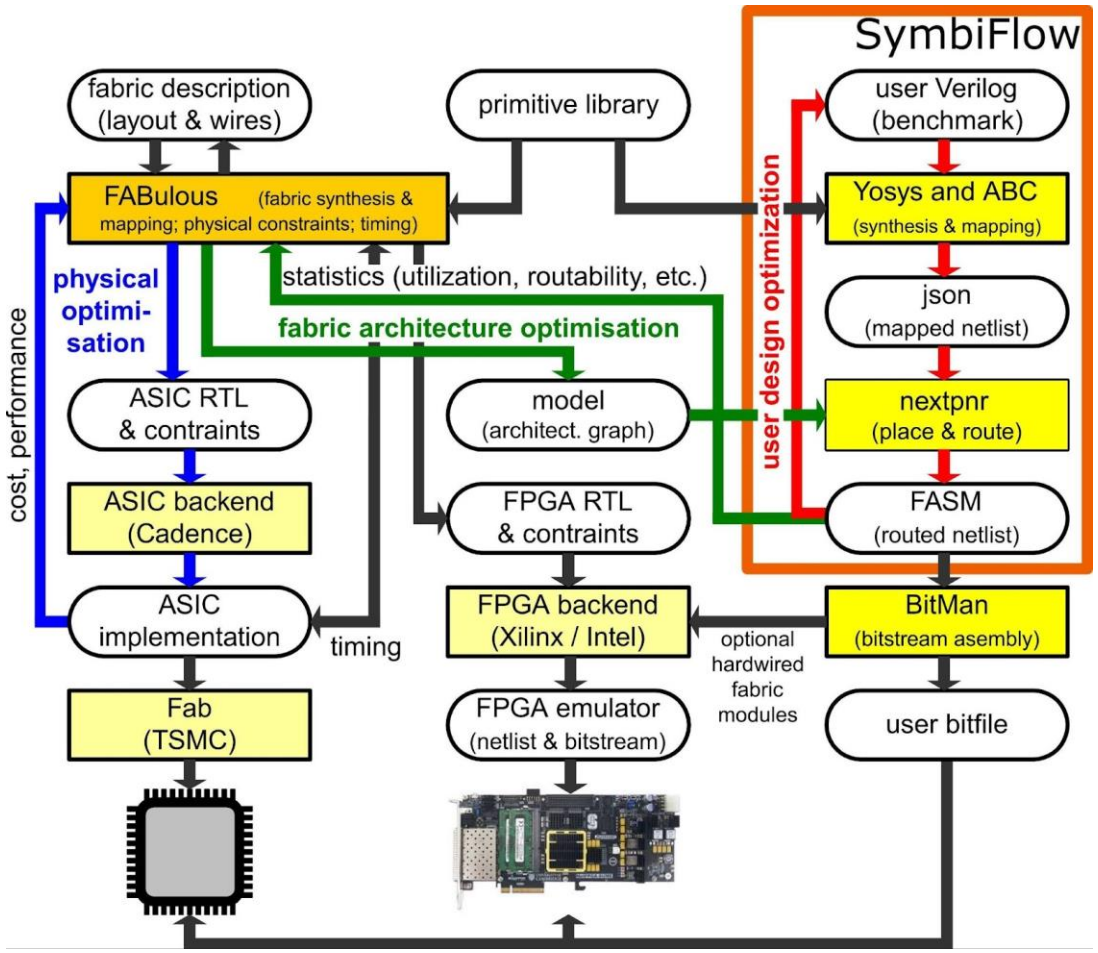
Pixel Architecture


Preliminary Pixel Layout: 25x25 µm^2

Designers: Alexandre Habib, Lorenzo Rota

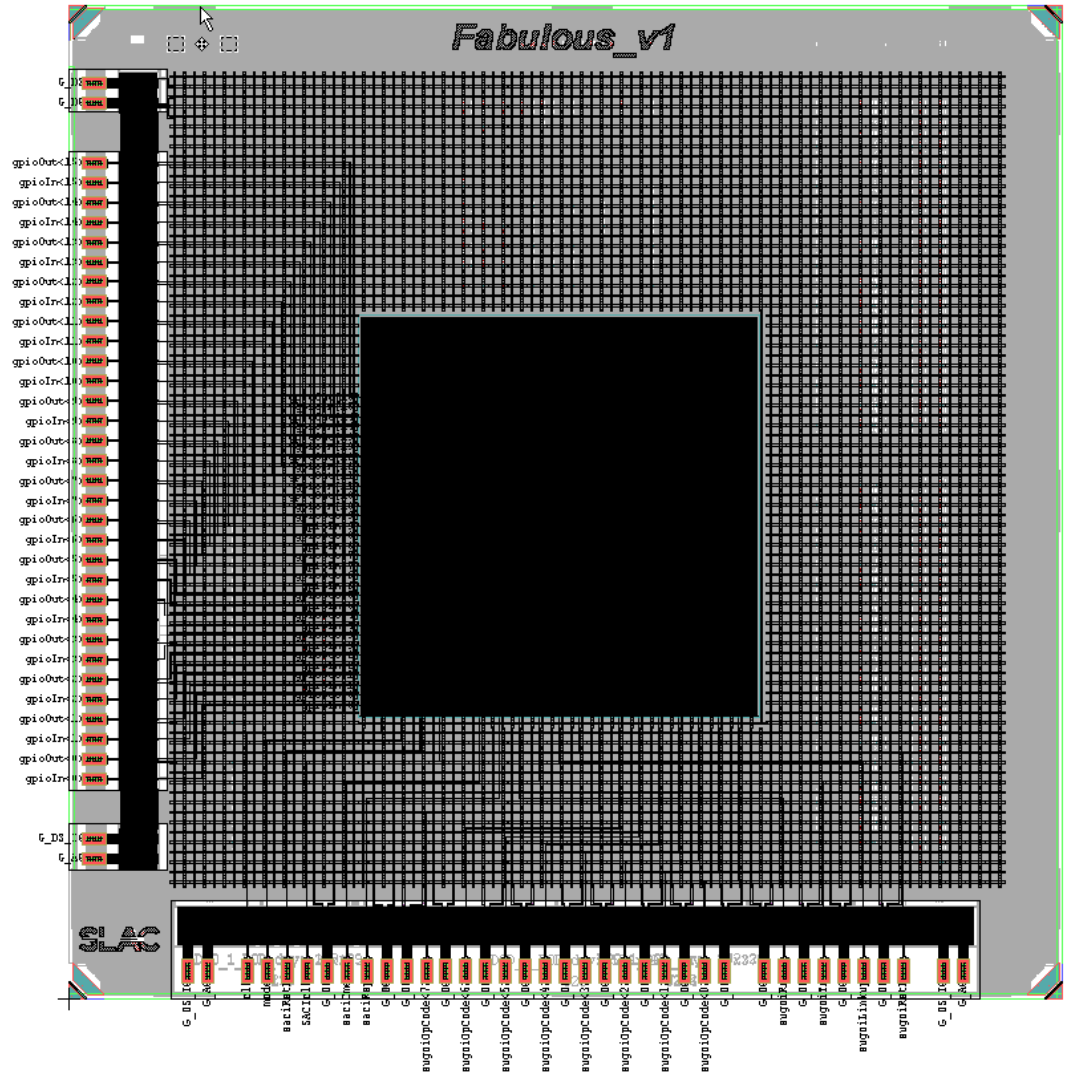
Fabulous

- Several popular FPGA architectures are becoming 20+ years old
  - Which means that original patents have expired
  - Includes Spartan-3 and Virtex-II FPGAs from Xilinx
- In 2021, University of Manchester has started an open-source projects called FABulous
  - an Embedded FPGA (eFPGA) Framework
- Idea is that you put an “reconfigurable logic” in your ASIC design



Fabulous

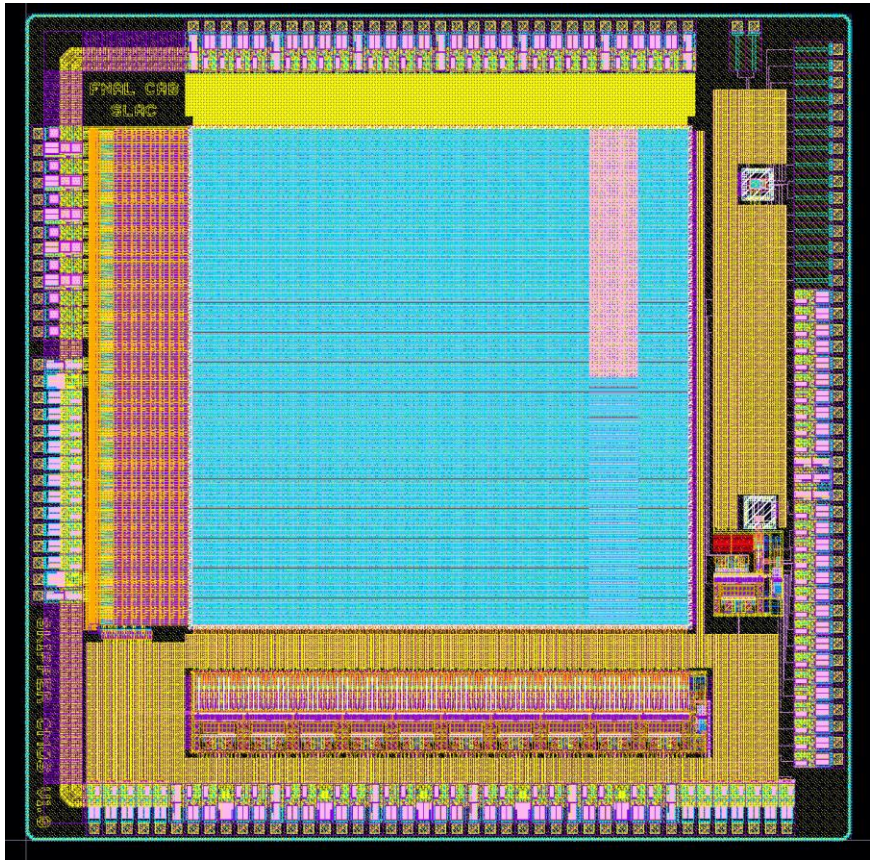
- Submitted on TSMC 130nm MPW on May 15, 2022
  - ETA: Aug 2022
- Simple Example eFPGA design to tryout the framework
  - 384 logic cells
  - 128 registers
  - 4 DSP slices
- ASIC will be wire bonded to an FMC carrier and eFPGA bitstream loaded from a Xilinx development board
- **Goal:** get more familiar with the open-source framework and tools before implementing an eFPGA in a readout ASIC.



Skipper-in-CMOS

- Collaboration between FNAL, CAB, SLAC and TowerJazz
- Development of a Skipper-CCD on a CMOS process:
  - Multiple non-destructive readouts enable noise performance <0.1 e-
  - CMOS integration enables higher frame-rates
  - Prototype developed on TowerJazz 180 nm
- Several applications in neutrino, direct dark matter search, soft X-rays, quantum imaging, *etc*...

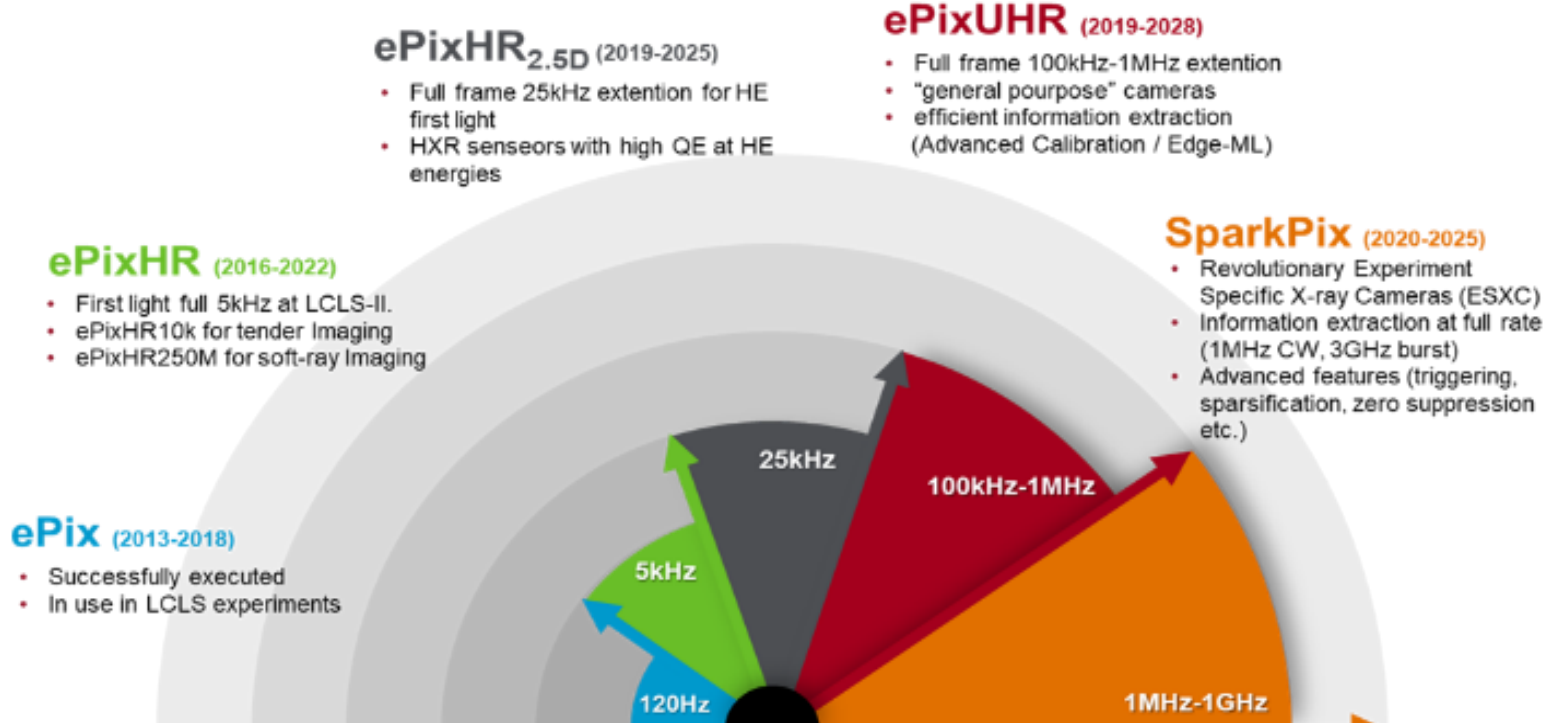
- Current and future R&D in the scope of DoE µElectronics proposal:
  - integrate Skipper-in-CMOS sensor with readout ASIC
  - target frame-rate: 1 kHz



Detectors for photon science: ePix/SparkPix families

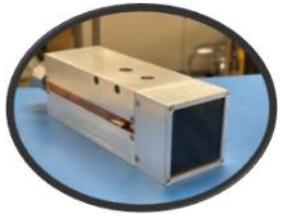
Current R&D driven by the scientific goals of LCLS-II/HE and its MHz operation. Two main class of detector needs:

- 2D direct conversion Pixel Array Detectors with large DR, high QE, frame rates of 100 kHz, full-frame readout
  → **ePixHR/UHR**, phased approach 5kHz (2021) → 25kHz (2025) → 100kHz (~2028)
- 2D direct conversion Pixel Array Detectors with MHz frame rate and real time processing capabilities, specifically designed to address the needs of classes of experiments exploiting the full potentials of the LCLS-II.
  → **SparkPix,** information extraction in real-time to push operation to 1 MHz in CW and GHz in burst

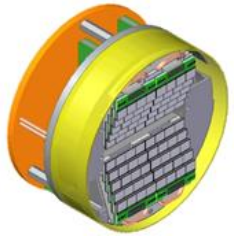


ePix highlights

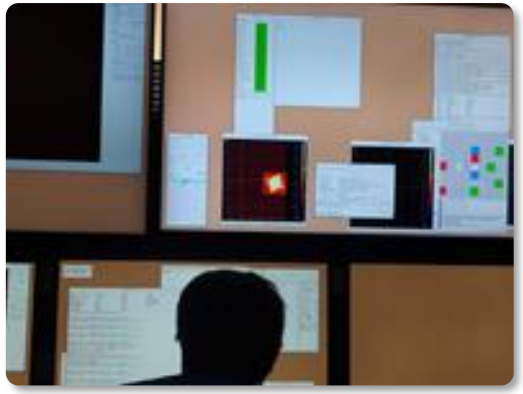
ePixHR10kt: 5 kHz frame-rate for tender X-rays



140kPix, 5Kfps
ePix10ktHR

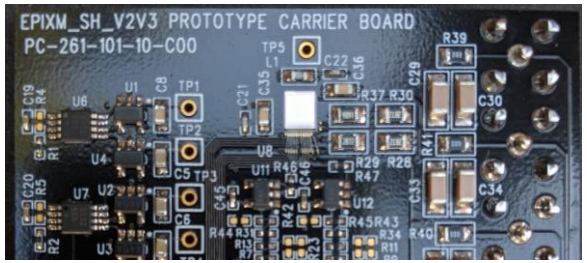


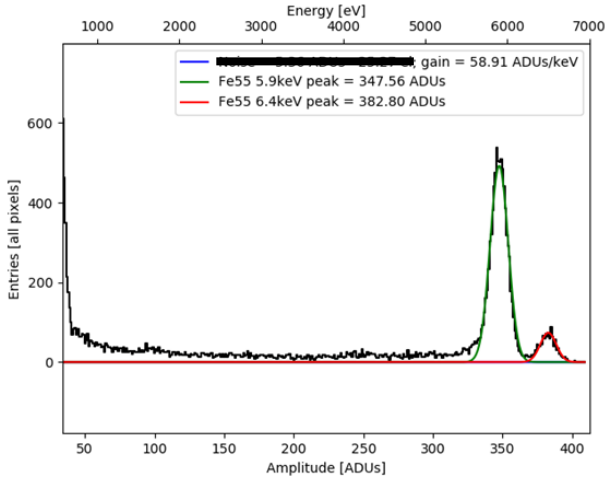
2.2MPix, 5Kfps
ePix10ktHR



RIXS control room – test beam

ePixM: 7.5 kHz MAPS on LF150nm for soft X-rays





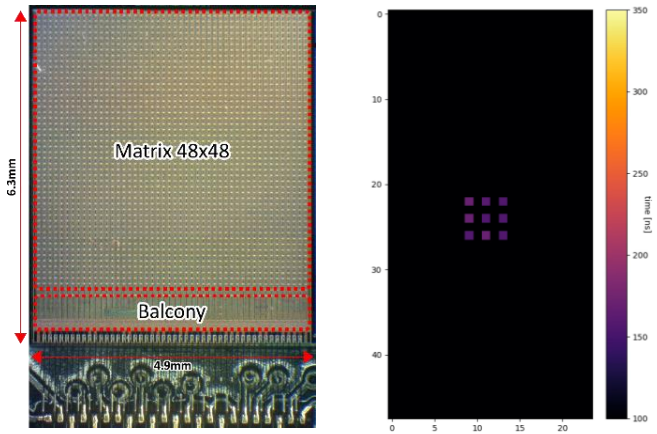
Spectrum Fe55 (raw data)

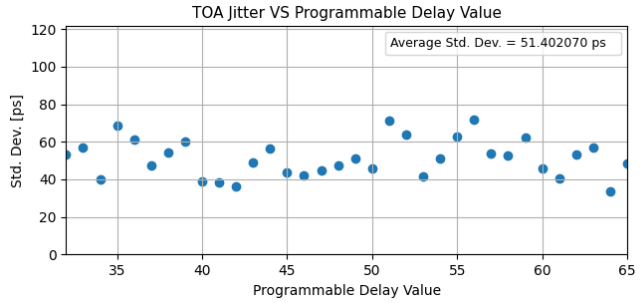
ePixUHR: 35 kHz frame-rate for tender X-rays

in progress…

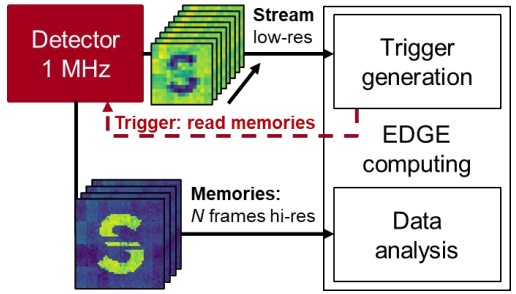
SparkPix highlights

SparkPix-T (Tixel): timing detector with 100 ps resolution and sparse read-out @ 1 MHz

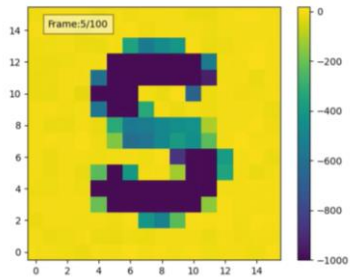




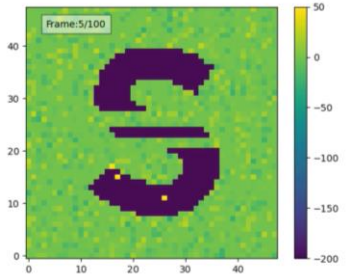
SparkPix-ED: full-frame pixel detector with adaptive resolution and trigger capabilities



Sum: 1 MHz



Hi-res: 0.1 MHz



SparkPix-S: sparse readout @ 1 MHz for XPCS experiments

In progress..