

BNL ASIC Group

G.W. Deptuch

05/15/2022



@BrookhavenLab

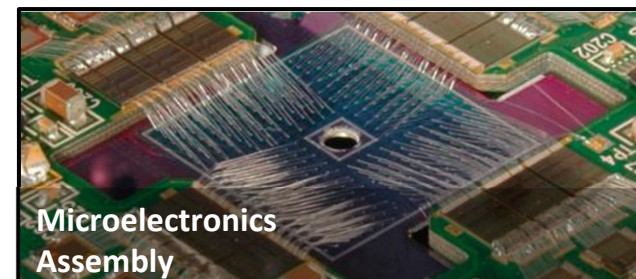
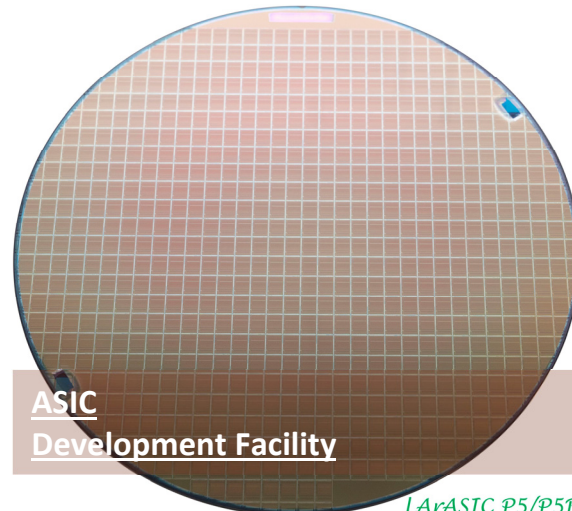
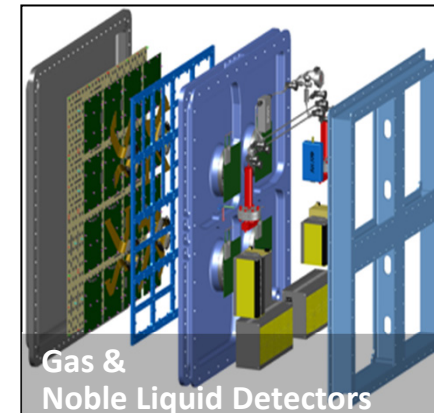
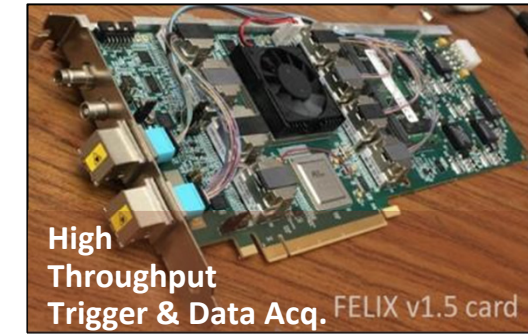
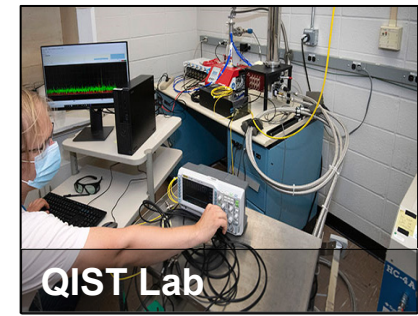
ASIC Group

Location in Instrumentation Division

Instrumentation Division Radiation Detectors Platform

key capabilities enabling BNL Science Programs:

- ✦ Sensors Si – CdTe – CdZnTe – Ge – Se – Perovskite
- ✦ Gas & Noble Liquid Detectors
- ✦ **Application Specific Integrated Circuits (ASICs)**
- ✦ CAD for Device & Board Level Circuit Design
- ✦ Microelectronics Assembly and High-Density Interconnect
- ✦ High Throughput Trigger and Data Acquisition
- ✦ Photocathode Development & Production (for detector and accelerator applications)
- ✦ Quantum Information Science Laboratory



ASIC Group

People, Tools, Collaborations, Areas of Activities and Research Interests

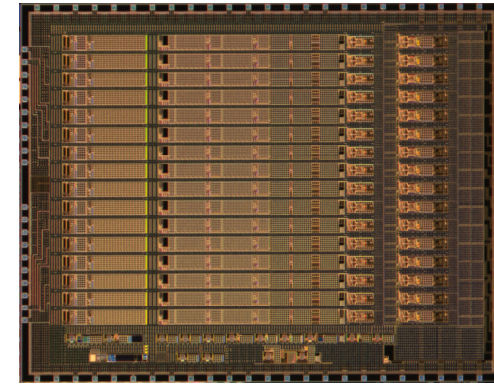
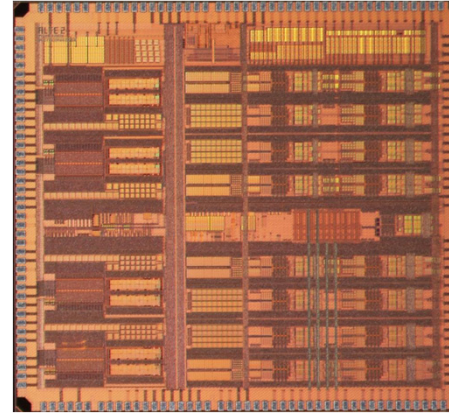
ASIC People and CAD/EDA Tools

Expertise in low-noise, low power, large mixed-signal designs

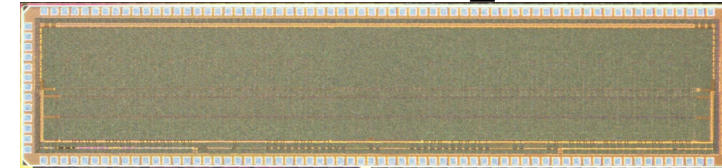
- 7 full time ASIC designers
(5 PhDs + 2 in PhD program, including industrial background)
- ongoing targeted hiring for satisfying needs across multiple programs
- open for hosting guest/visitors and grad/post-grad students
- hand-in-hand with in-house TDAQ, PCB, sensors and other groups

Design tools and methodologies

- industry-standard tools from Cadence, Siemens (Mentor), etc.
(analog on top or digital on top flows)
analog: full custom flow (VSE, VLE, ADE/Spectre, AMS, PVS, XACT3D-PEX)
digital RTL2GDS: functional simulation, logic synthesis, automated P&R, parasitics extraction, static timing analysis (XCELIUM/GENUS/INNOVUS/QUANTUS QRC/TEMPUS)
library characterization: custom standard cell libraries for designs for extreme environments: cryogenics and radiation
verification: IR drop (VOLTUS/ VOLTUS-fi), functional (SV), physical (PVS, Calibre DRC/ERC/LVS)
device modeling: TCAD, FEM solvers, transistor model parameter extraction (Silvaco ATHENA-ATLAS-VICTORY, Maxwell, UTMOTS4)
- foundry PDK's: TSMC CMOS 350nm, 250nm, 180nm, 130nm, 65nm, GF CMOS and BiCMOS SiGe 130nm, 90nm, + specialized processes: monolithic CIS on HR, sensors co-design, High-Voltage etc.
- access to foundries via: MOSIS, CERN-IMEC Foundry Services, IMEC and directly
- packaging: in house custom and through commercial sources



⬆️ LArASIC_P4 180 nm
⬅️ ALFE2 130 nm
⬇️ AVG_DEV 65 nm



ASIC Collaborations, Areas of Activities and Research Interests

Collaborations:

- Universities: SMU, UMich, UPenn, MIT, Georgia Tech, Columbia, USF, UIUC
- National Laboratories: FNAL, LBNL, ORNL, NRL
- Industry: several industrial partners + more collaborators
- International: CERN, OMEGA, KIT Karlsruhe, AGH Krakow, UBonn

Support for fast-developing scales and functionalities of modern microelectronics:

- meet customer's needs using established processes (130nm, 65nm)
- reaching for emerging technologies for R&D (28nm, specialized processes)

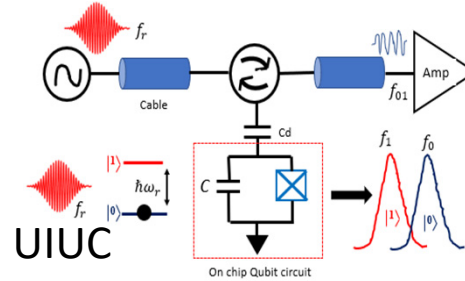
Areas of Activities and Research Interests:

Low-noise and low-power

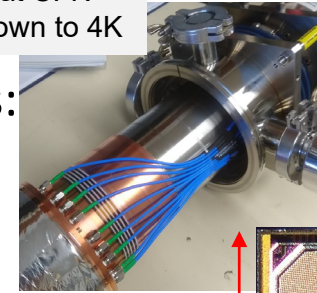
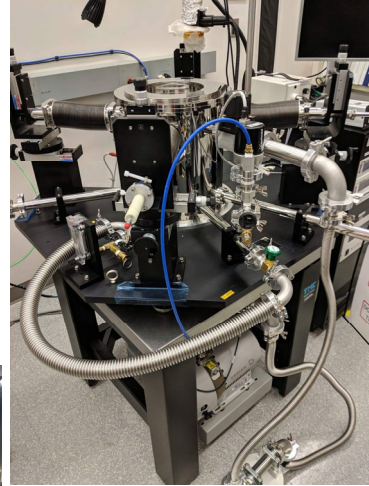
- custom analog front-end matched to a specific sensor
- front-end circuits optimized for amplitude & time-resolution
- data, event driven or zero-suppressed readout methodologies

Cryogenic operation

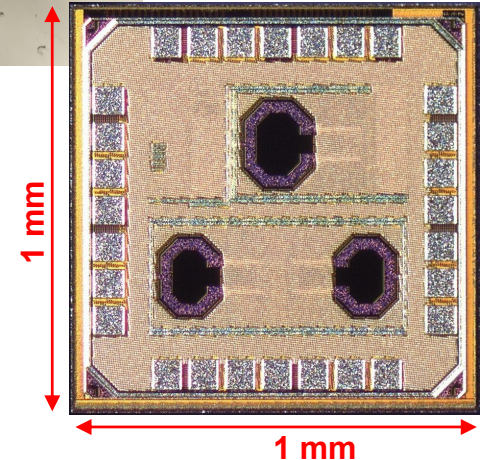
- readouts for Noble liquid TPCs – R&D on RO electronics for DUNE's VD TPC, nEXO (lAr, lXe)
- long lifetime reliability
- development & maintenance of spice-type model parameters and characterization (.lib) of standard cell libraries
- RF electronics for quantum sensors (4K, $\leq 1K$)



RF readout of qubits or quantum sensors / probe station at CFN cryostat at IO operating down to 4K



Layout of 4K RF tests structures
CryoCMOS
With 5.12 GHz center frequency
VCO and QVCO for PLL with
CML divider and interfaces
QRFIC_P1



ASIC developments - examples

DUNE 3-ASIC system

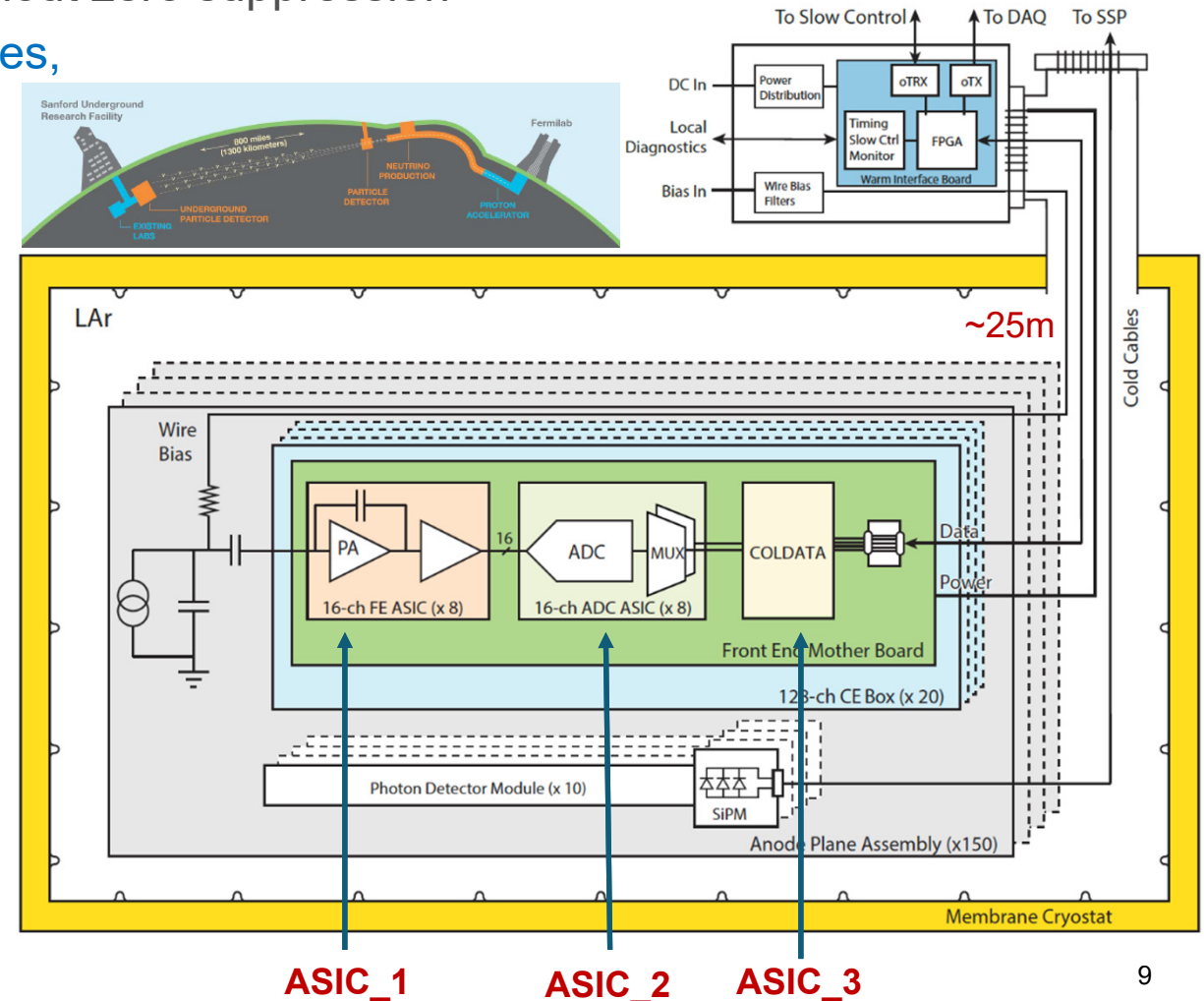
FE for LAr Calorimeter in ATLAS

Event Driven Readout for Pixel Detectors

Data Streaming or Sparsified Readout

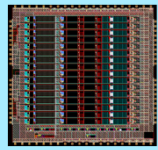
DUNE 3-ASIC LAr TPC Readout

- Integrated electronics in cryostat (giant TPC with ~5 m drift distance) in liquid Ar (80 K, not accessible for lifetime of DUNE experiment ➡ **HCE reliability**)
- Waveforms are digitized at 2 MHz and read out without zero suppression
- **Electronics circuits are mounted near the sense wires,**
 - Amplifier and Shaper 16 channels
 - ADC 16 channels
 - Data Merger and Serializer 2×1.25 Gbps
- **3-ASIC readout for DUNE far detector:**
 - Front-End: LArASIC (180 nm) by BNL,
 - Time interleaved ADC: ColdADC (65 nm) by LBNL, FNAL, BNL)
 - Data concentrator/transceiver: ColdDATA by FNAL, BNL digital implementation and P&R
- **One 10 kTon FD-1HD detector has:**
 - 3000 x 128-channel Front End Mother Boards with 24000 x FE ASICs, 24000 x ADC ASICs, 6000 COLDATA ASICs
 - **Total 12000 1.28 Gbps links (9.2 Tbps of waveform data)**

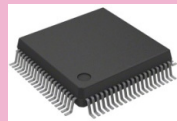


DUNE 3-ASIC IAr TPC Readout

MicroBooNE



LArASIC



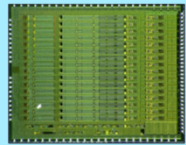
COTS ADC



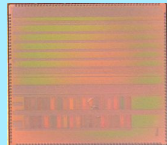
FPGA

DIGITAL LINKS
→ DAQ

proto-DUNE



LArASIC



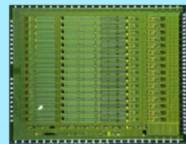
COLD_ADC



FPGA

DIGITAL LINKS
→ DAQ

SBND



LArASIC



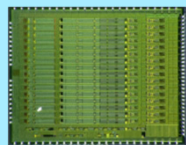
COTS ADC



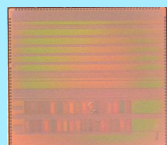
FPGA

DIGITAL LINKS
→ DAQ

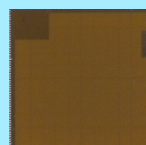
DUNE



LArASIC



COLD_ADC



COLD DATA

DIGITAL LINKS
→ DAQ

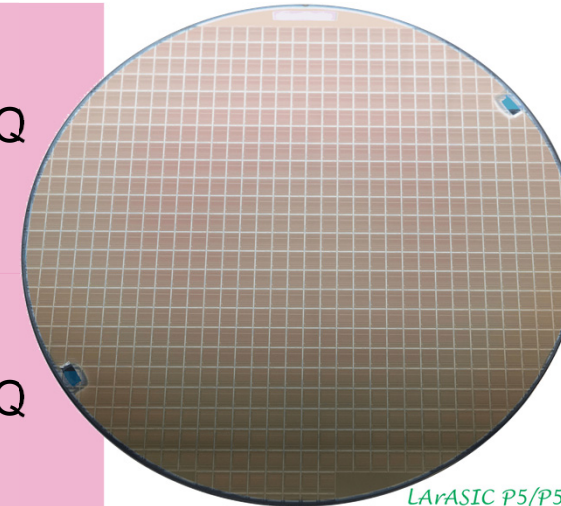
CMOS 180

CMOS 65

CMOS 65

88K

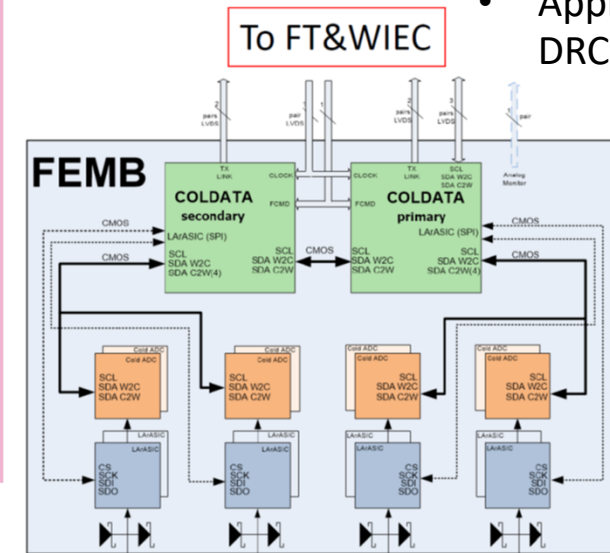
300K



8" wafer with 610 LArASICs P5 and P5A(B) w. increased ESD protection

Last modification:

- Removed "ledge" effect (saturation) causing dead time
- Improved BGR reference to avoid ~10% "no-startup" chips
- improved linearity and range of calibration DAC
- addition of strength to input pad ESD protections
- solving reset-quiescent current mismatch problem at LNT
- Improving stability of output single-to-differential converter
- Application of recommended DRC rules where possible



128 CHs FROM Anode planes (APA or CRP)

250 wafers
LArASIC
production run
for DUNE ~75k
P5 and 75k P5B
chips is under
way

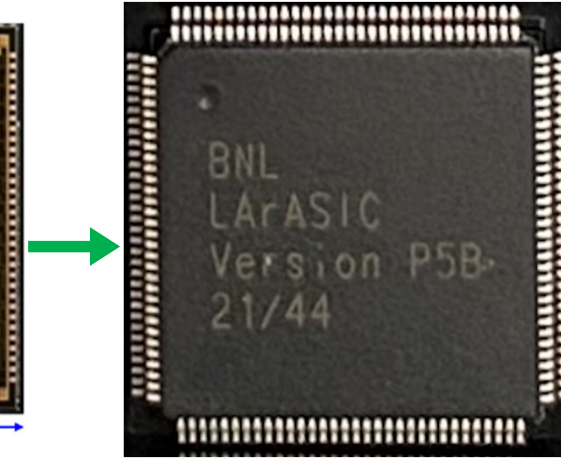
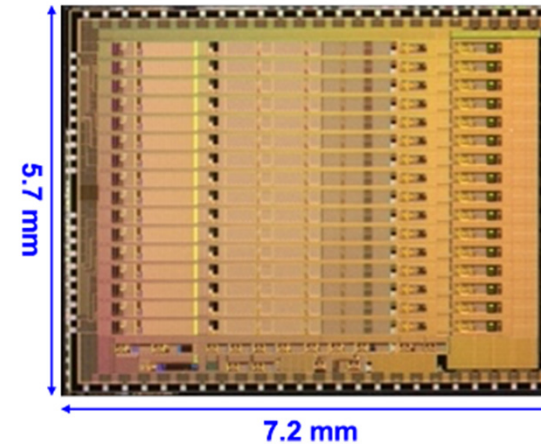
LArASIC P5/P5B Yield QA/QC testing

LArASIC MPW met all the DUNE requirements → fabricated ~1800 P5 and 1800 P5B chips (eng. run) for ProtoDUNE II

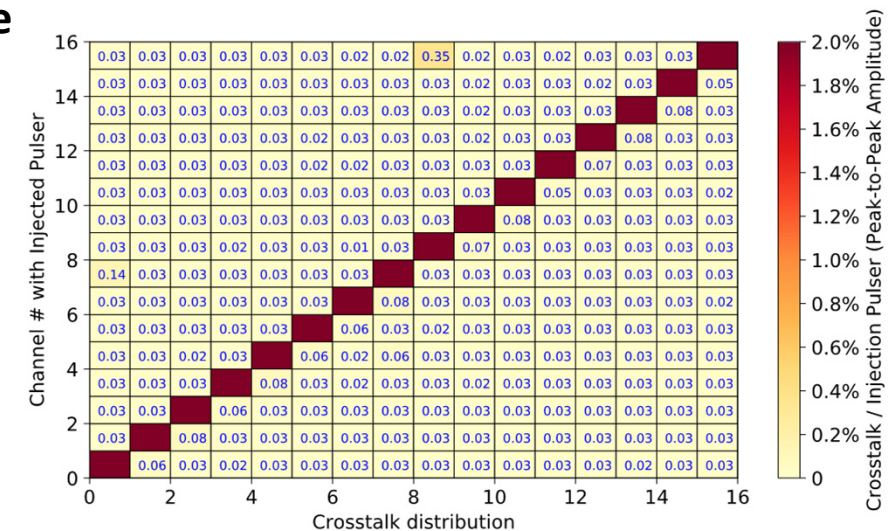
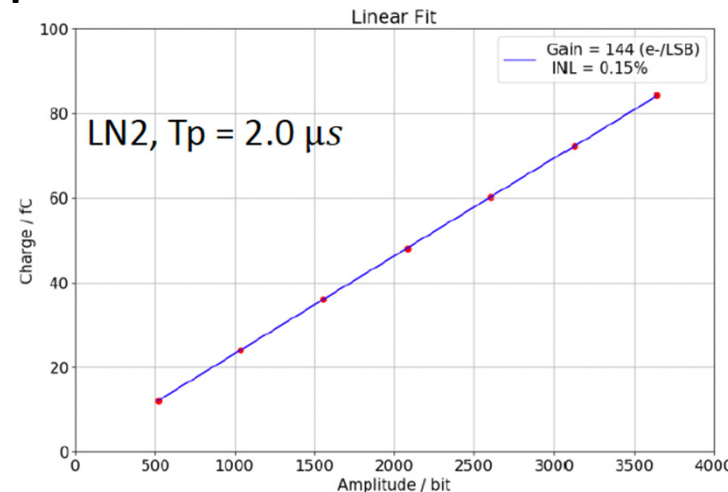
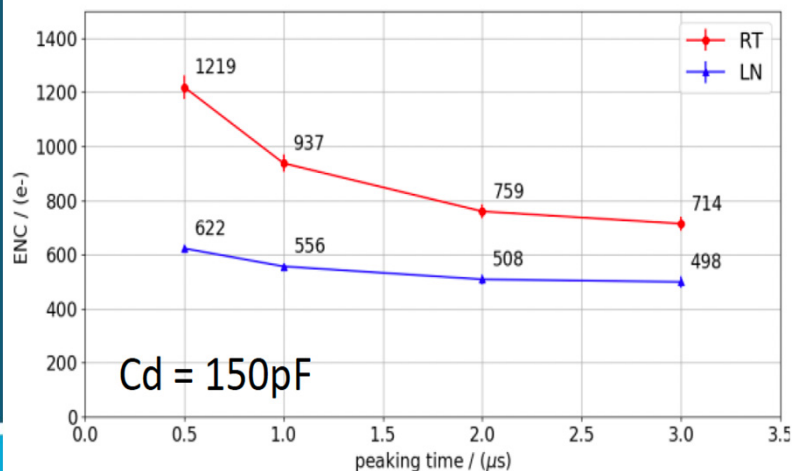
LArASIC Chips	Temp.	Tested Chips#	Good # (All channels are normal)	Yield
P5	RT	49	49	100 %
P5B	RT	1642	1635*	~99.57 %
P5B	LNT	317	317	100 %

P5B has improved input ESD protection compared to P5

*Only 1 out of 16 channels in each of the two chips are non-functional



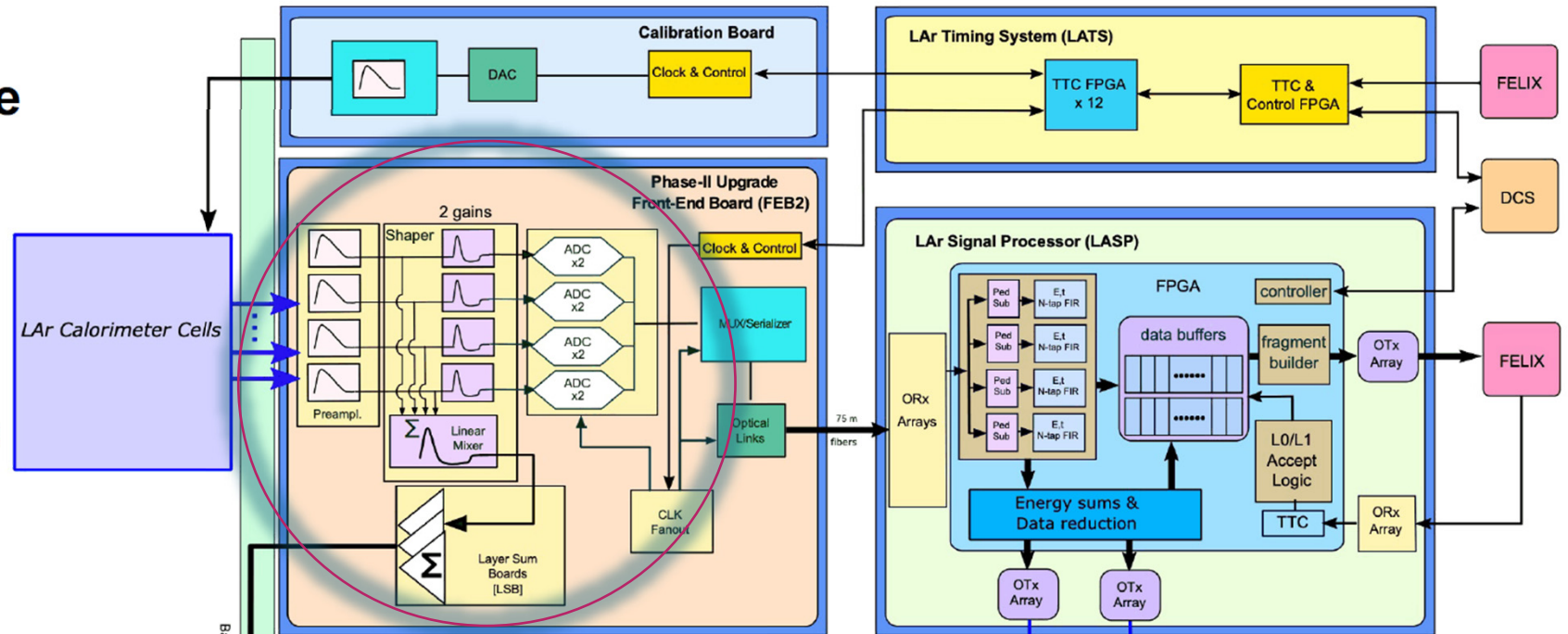
LArASIC performance with differential interface



FE for LAr Calorimeter in ATLAS

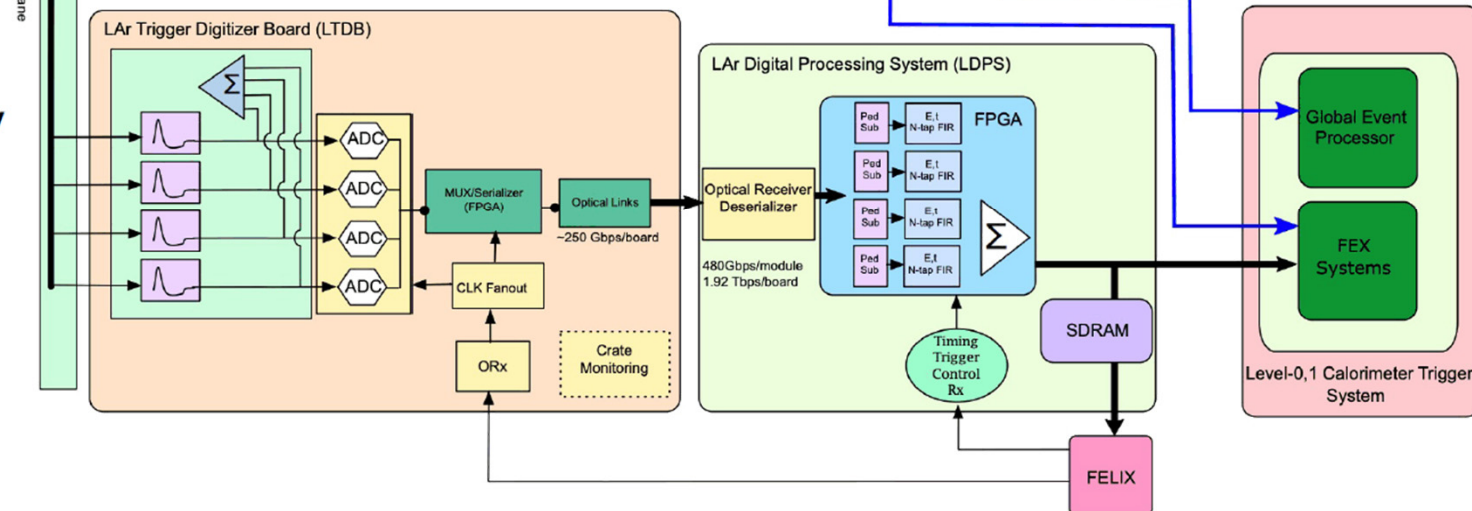
Phase-II Upgrade

Digitize and readout the full calorimeter, at 40 MHz and provide the information to Level-0 trigger systems



Phase-I Upgrade

Increase the granularity of the Calorimeter Cell sum information for Level-1 trigger system (In-installation)

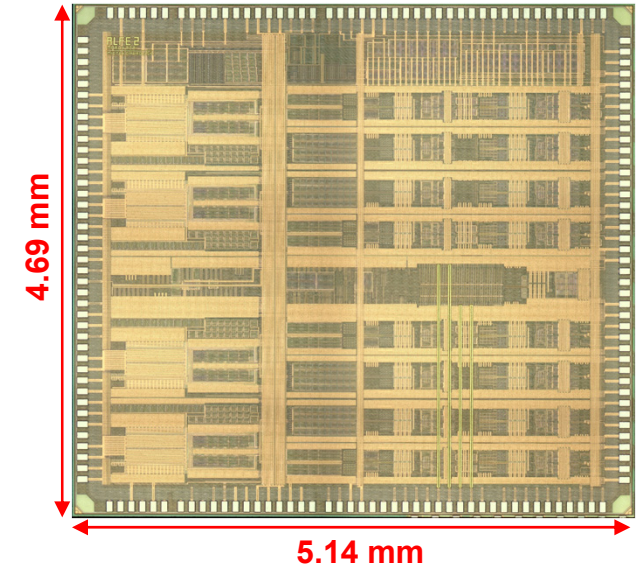
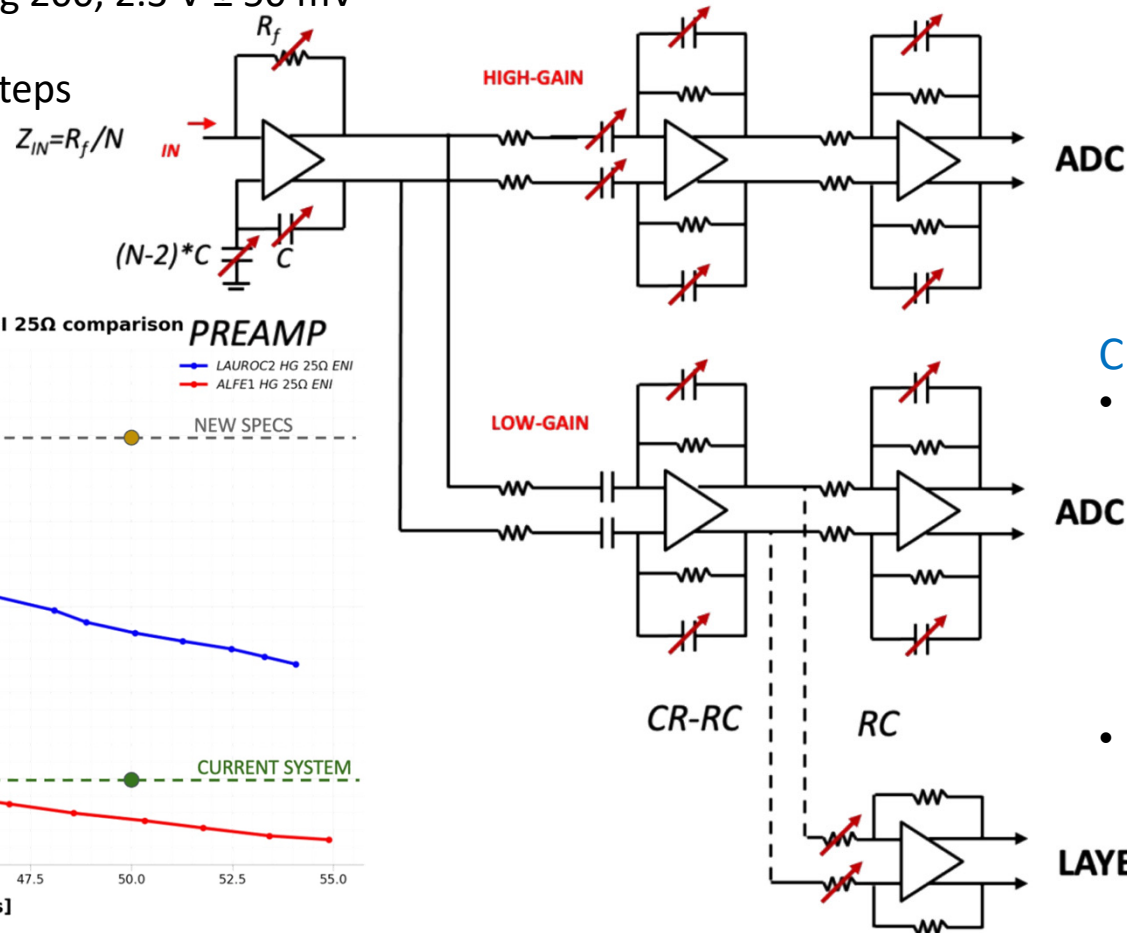
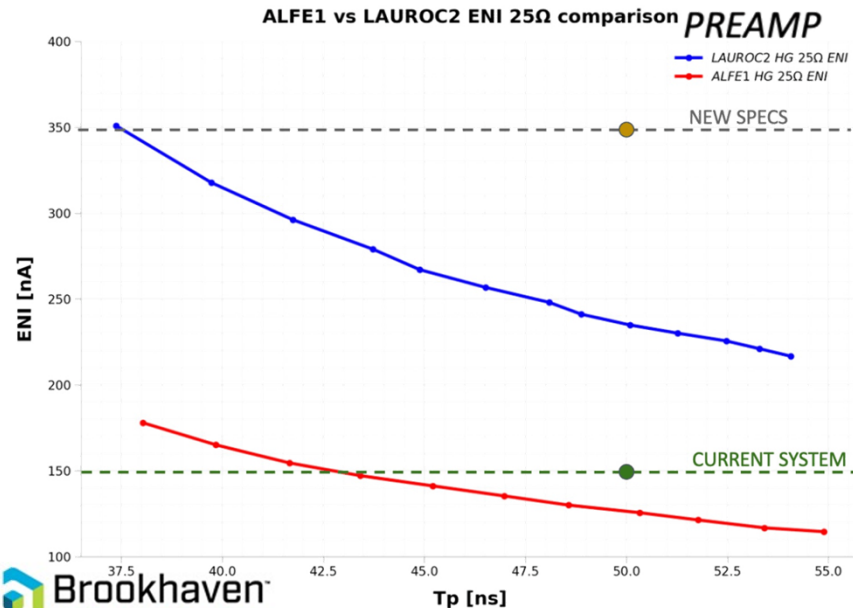


LAr Calorimeter in ATLAS

Requirements for FEB2 Preamplifier – Shaper (PA):

- 4 Channel input, 9 Channel output (4 x LG/HG + Trigger sum of 4 channels)
- Input impedance and Dynamic range programmability (25 Ohm 10 mA, 50 Ohm 2mA)
- Input impedance tuning < 2.5 % steps
- Peaking time tuning (15 ± 5 ns, 1 ns steps)
- Preamplifier DC level tuning 200, 2.3 V \pm 50 mV
- DC output tuning, 600 mV \pm 360 mV, 30 mV steps

Two Front-End designs were carried out and compared



ALFE2 CMOS 130 nm

Choice of ALFE PA:

- ALFE PA was selected for the FEB2 due to its excellent noise performance and power supply noise rejection, Non-Linearity < 0.2 % (HG) over full DR, no change in performance under irradiation up to 1 Mrad (beyond specifications)
- 48,832 ASICs will be required to populate LAr Calorimeter's FEB2

LAYER SUM BOARD

Event Driven Readout (EDWARD)

D.S. Gorni, et al., "Event driven readout architecture with non-priority arbitration for radiation detectors", 2022 JINST 17 C04027

TWEPP 2021

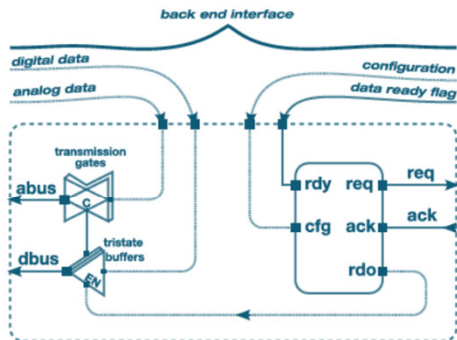
Arbitration tree

Introduction

The poster introduces an efficient system for collecting sparse data originating in multiple sources that operate asynchronously, ultimately sending data to the central data acquisition system in such a way that there is no direct relationship between spatial position of the channel and the order of the channels to be transmitted. The protocol and hardware architecture were developed for ASICs destined for reading out 1D or 2D multichannel radiation sensors that can be micro-strip or pixelated radiation sensors. The presented system can be used to read out both digital and analog data from the channels. It is done via shared digital data buses and analog wires.

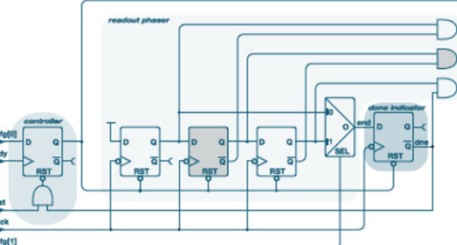
In-channel logic

Fig.2 In-channel logic general structure



- This is a logic presented in each channel and its function is to manage readout transactions between the channel and global peripheries.
- When the data ready flag 'rdy' is set by the back end electronic (e.g. peak found, ADC conversion done) the controller block issues the read request 'req' immediately.
- When 'req' is active, the readout phaser block is sensitive to the transition to the active logic state on the channel acknowledge input 'ack'.
- This transition can be describes as receiving an **acknowledge token** with assigned expiration time, after which 'ack' switches back to the inactive state.

Fig.3 In-channel logic core



- The first token initiates readout transaction.
- A single transaction may consist of **multiple readout phases** in which different data (including data from adjacent channels) may be transmitted sequentially and uninterrupted by requests from other channels.
- The maximum number of phases is determined by the number of flip-flops in the phaser chain. However, the actual number of phases can be dynamically reduced by various 'cfg' configurations.
- Only one bit of the readout control 'rdo' is active during each transaction. This active bit is used to enable the corresponding bank of tristate buffers and transmission gates.
- After the last phase is processed done flag 'dne' is set and in result next token initiates reset procedure for in-channel logic during which 'req' is cleared.

Default bus state

The 'rqr' output from the arbitration tree is effectively the logical sum of requests from all channels. This signal, however, is not synchronized in any way with the acknowledgement tokens - the request may come after token expiration or come too late, and the token will not be able to start the transaction due to too short duration of the active state in the channel. For this reason, a mechanism should be provided to distinguish between data derived from readout of a channel and an empty state. This has been implemented as a **network of up and down pulls that delineate empty data**. The pattern thus determined can then be discarded on-chip by a peripheral circuit or off-chip in the acquisition system.

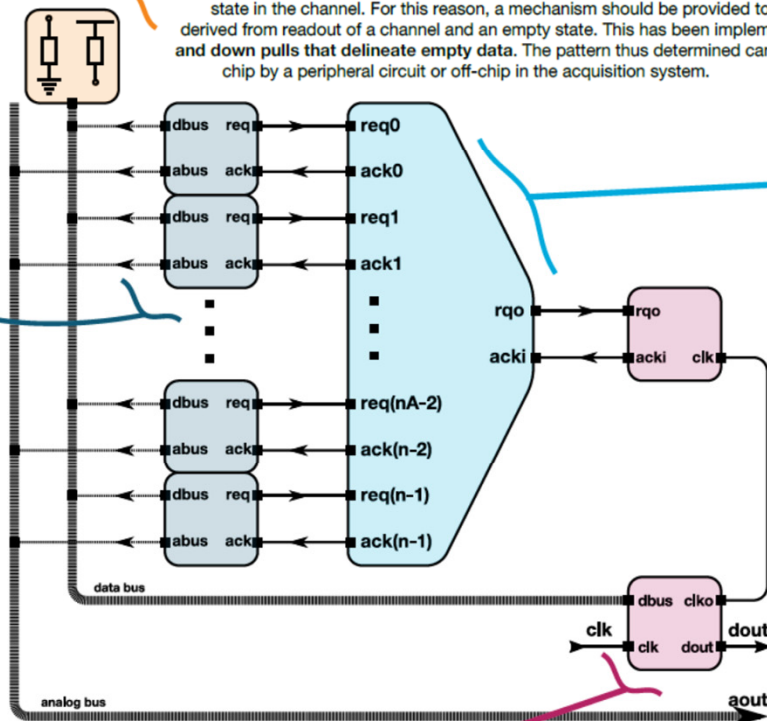


Fig.1 Block diagram of event driven readout system

Synchronization

The data are latched inside the output periphery by the clock 'clk'. Latching of the data synchronizes the readout with the data acquisition system. Data are latched before generation of each new token, yielding a new set of latched data for each token. Data can be sent serially off the chip. The **serialization clock is used therefore for generating readout tokens** through its appropriate division, whereas the duty cycle and frequency of the divided clock 'clko' can be decided with a significant level of a latitude.

Fig.5 Different embodiments of arbitration cell

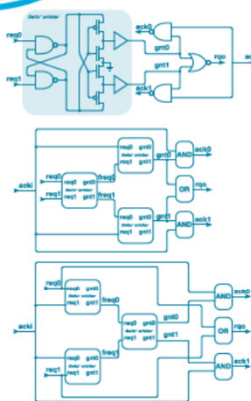
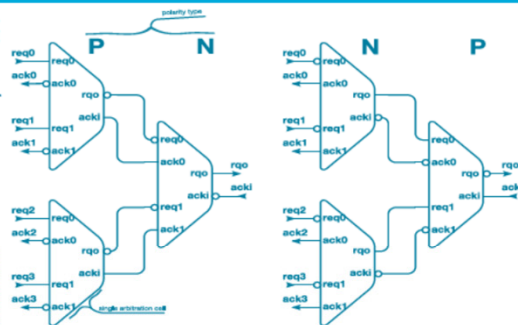


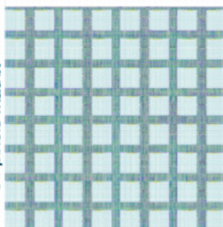
Fig.4 Arbitration tree construction using arbitration cells with different polarization



- An arbitration cell upon receiving read request signals 'reqX', selects one of the read request signals and routes an acknowledge token 'acki' that reaches this cell as routed from another arbitration cell located above in the arbitration tree to the direction from which the read request signal has been accepted. Routing is done in a form of gating of the acknowledge signal with the use of grant signals (gnt0, gnt1) generated by the arbiter. The arbiter decides which of the two read request signals is selected and there is **no priority between signals**. When two read request signals arrive simultaneously, one of them is selected, whereas the selection is random.
- Basically, almost all the arbitration cells need to be able not only to decide which of the two read request signals can be services but also whether new read request signals arrive during the active level of the acknowledge signal. The latter goal is rising a need of arbitrating between the read request signals and the acknowledge signals, leading to the general concept of the readout control system with **arbitration that is operated without distributing any system clock**.

Design and results

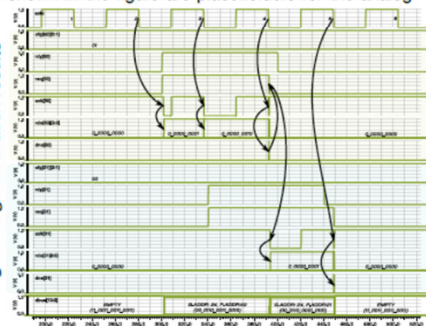
Fig.6 Layout of the 64 pixels matrix



In Fig.6 layout of the pixel matrix consisting of 64 channels is presented. Physical design was implemented with the use of the tools for automatic P&R and TSMC 65nm Standard Cell Library with added designs for Seitz' arbiters. The squares shown in the figure are placeholders for the analog frontend.

Transistor level simulation results are shown in Fig. 7. During transaction each channel sends its address (6bits) and group sends its address (8bits). Merged value is observed on digital bus. Config '00' result in one readout phase and '01' in two phases. It is worth to note how token is passed from one channel to other after transaction is done. Token is reused and no dead time is observed.

Fig.7 Design simulation results

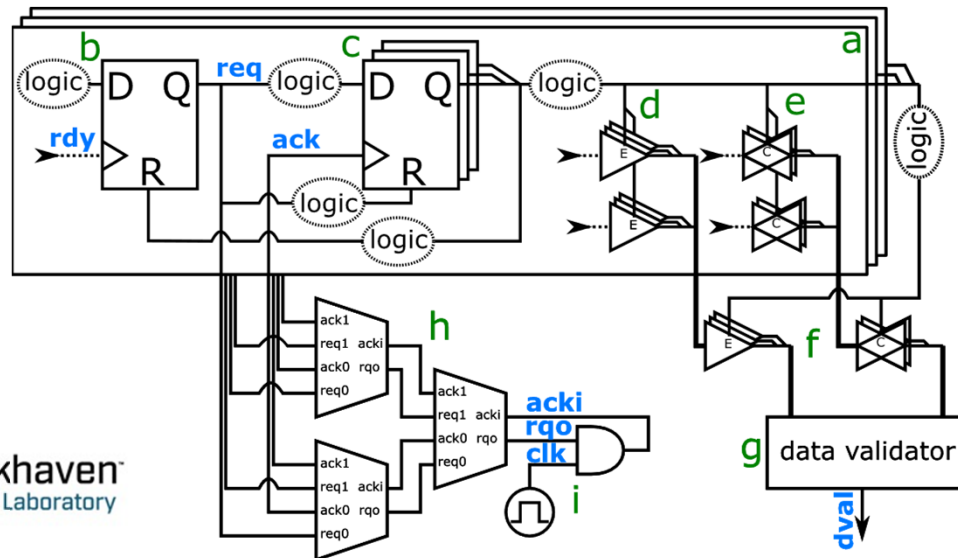


All-Digital Platform for Pixel Detectors

EDWARD –

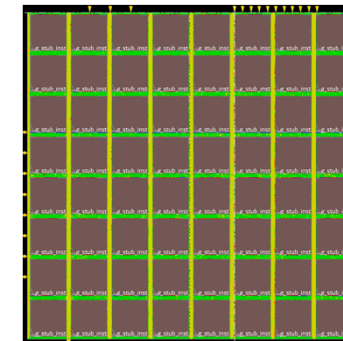
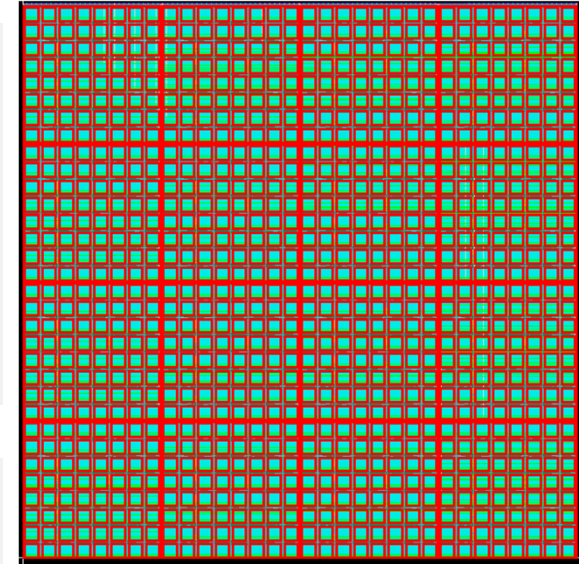
Event Driven With Access and Reset Decoder

1. receives notification about channel ready to be read out (rdy signal),
2. sends request (req signal) to access shared bus,
3. transmits request signal to synchronization unit (rqo signal) with simultaneous arbitration if there are multiple requests,
4. transmits acknowledge token (acki signals) to channel (ack signal) that wins arbitration = granting permission for exclusive access to bus,
5. lets channel drive its data to bus,
6. defines access time frame to channel and, if necessary, lets several data packets from same channel uninterruptedly in multiple phases,
7. switches immediately, without dead time, between channels if there is still at least one readout request after completing current readout,
8. establishes default bus state if no channel is currently being read out.



Universal All-Digital Platform for Implementation of Configuration-Testability-Readout Functionalities within Pixel Detectors

32 × 32 pixels matrix obtained by tiling 4 × 4 basic groups that is suitable for tiling into still larger matrix sizes. All pins are placed on one side for easy connections to peripheral circuitry logic

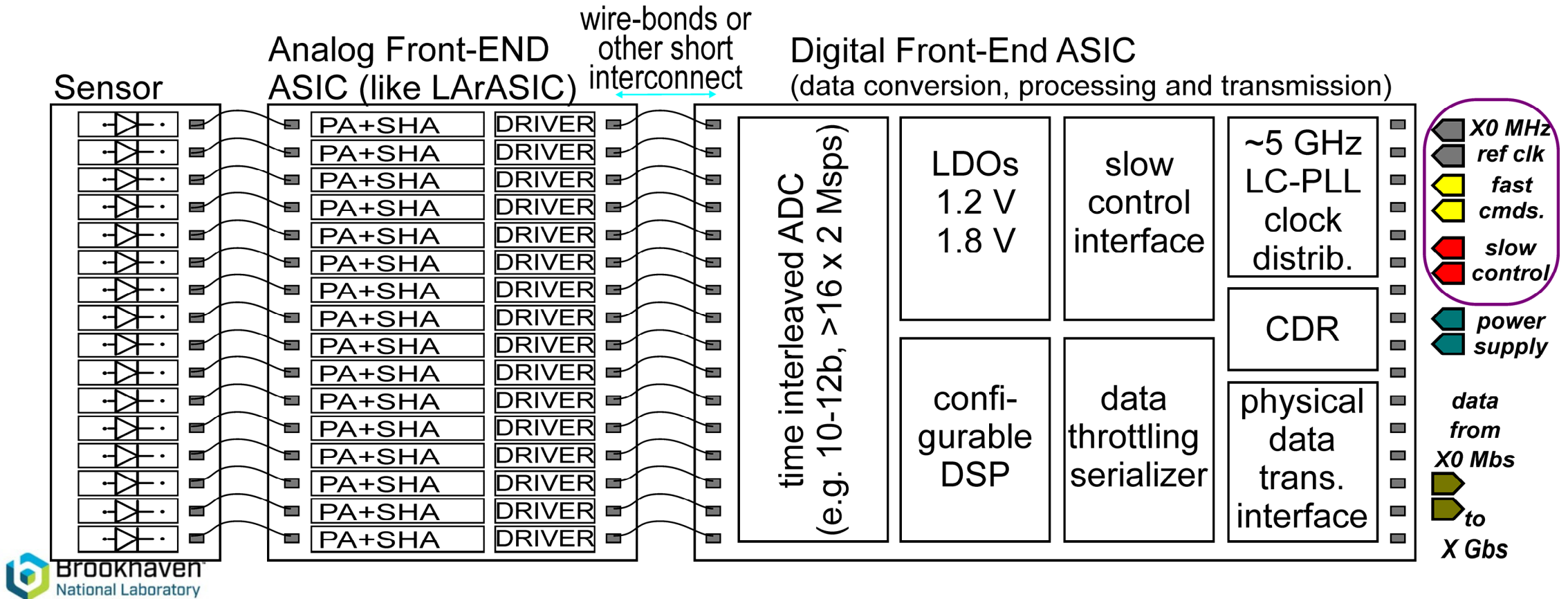


8 × 8 pixels base group layout for a 100 × 100 μm² pixel detector. Each brown square is space left for AFE (size = 90 × 90 μm²).

platform is based on developed RTL code that includes Configuration-Testability-Readout features that is parametrized and scalable to allow “virtual painting” of digital backbones of pixel detectors with high efficiency of area usage for Analog Front-End circuitry that is added on top 15

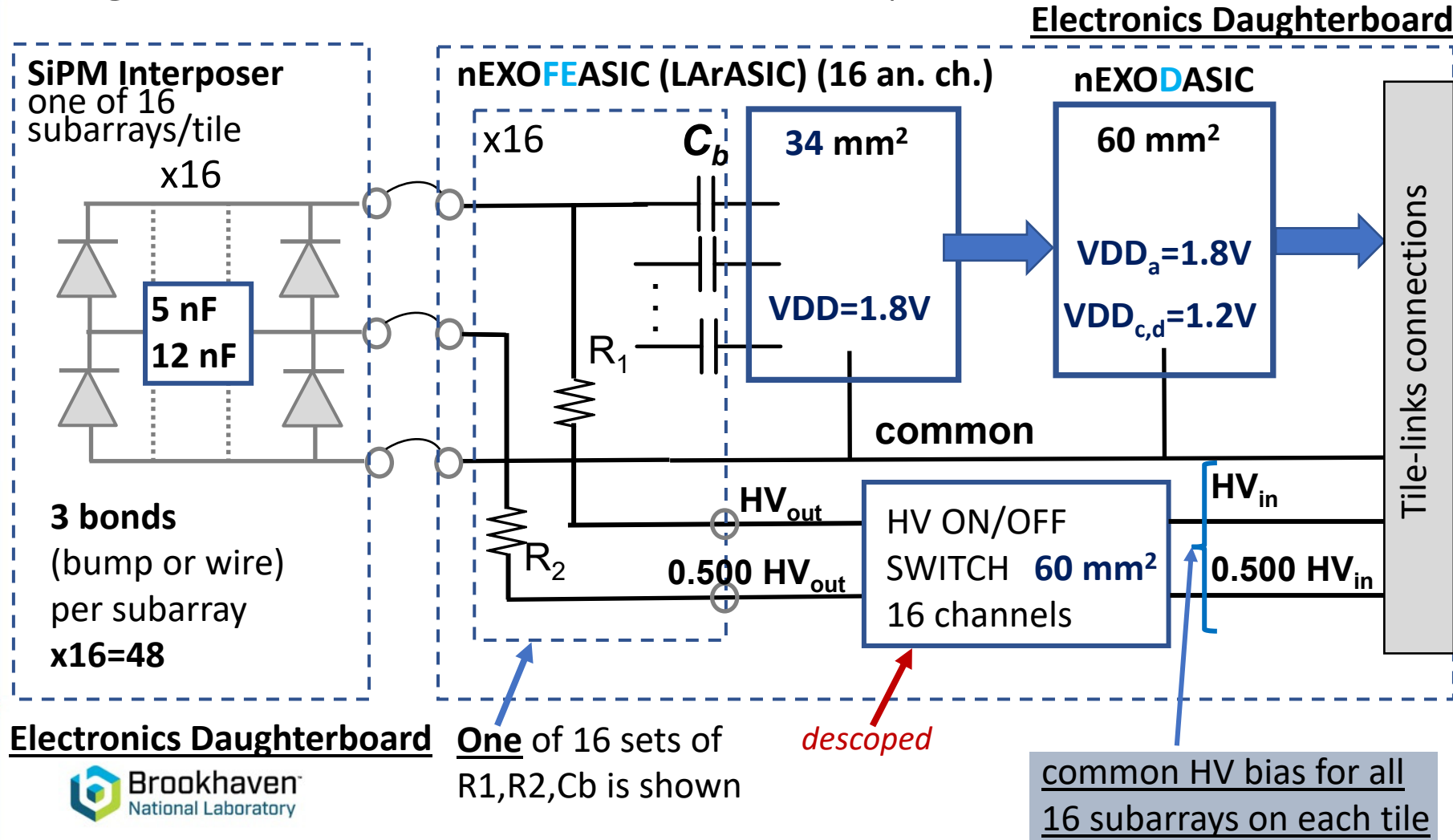
Scalable Next-Gen. Detector Front-End

- Optimized two-ASIC solution:
 - separates high-sensitivity analog from mixed-signal and digital circuits,
 - allows optimal allocation of functionality with fewer risks,
 - speeds up timeline through independent, parallel development paths,
 - does not significantly increasing packaging complexity v.s. “single ASIC
 - under active development for upcoming experiments such as nEXO



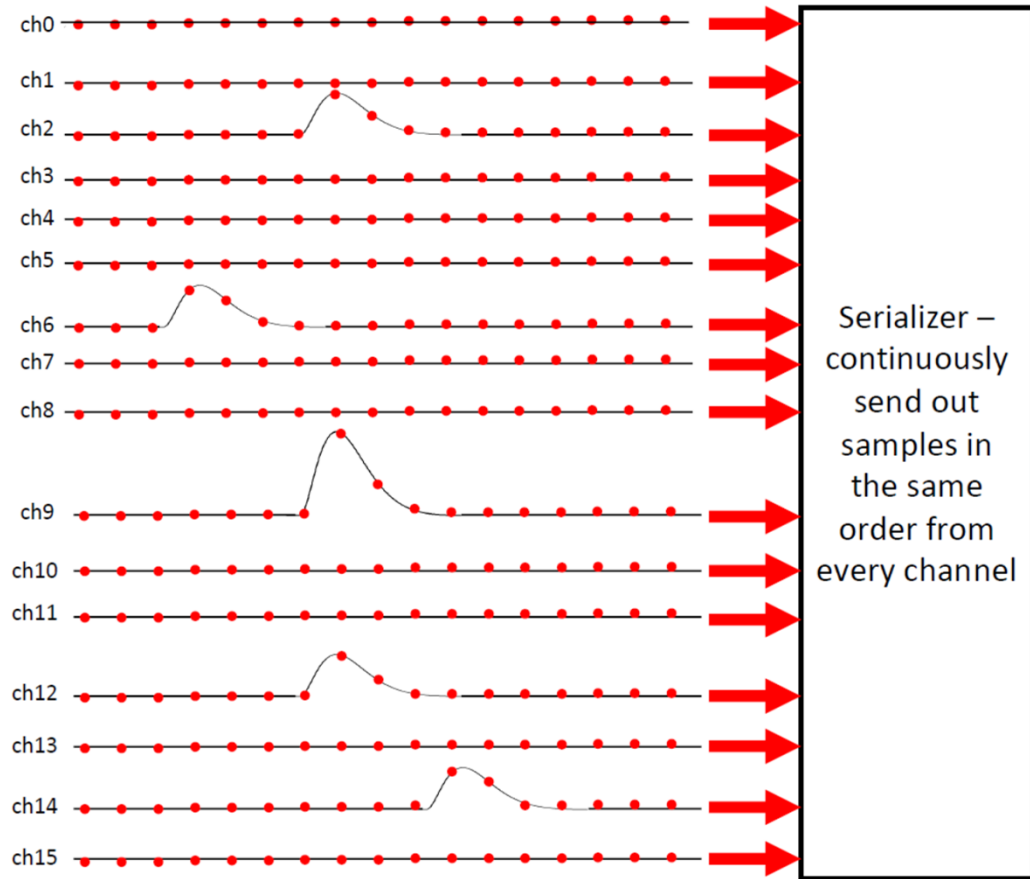
Two-ASIC Solution for nEXO

nEXO light readout SiPM Interposer and Electronics
Daughterboard Interconnections - Components

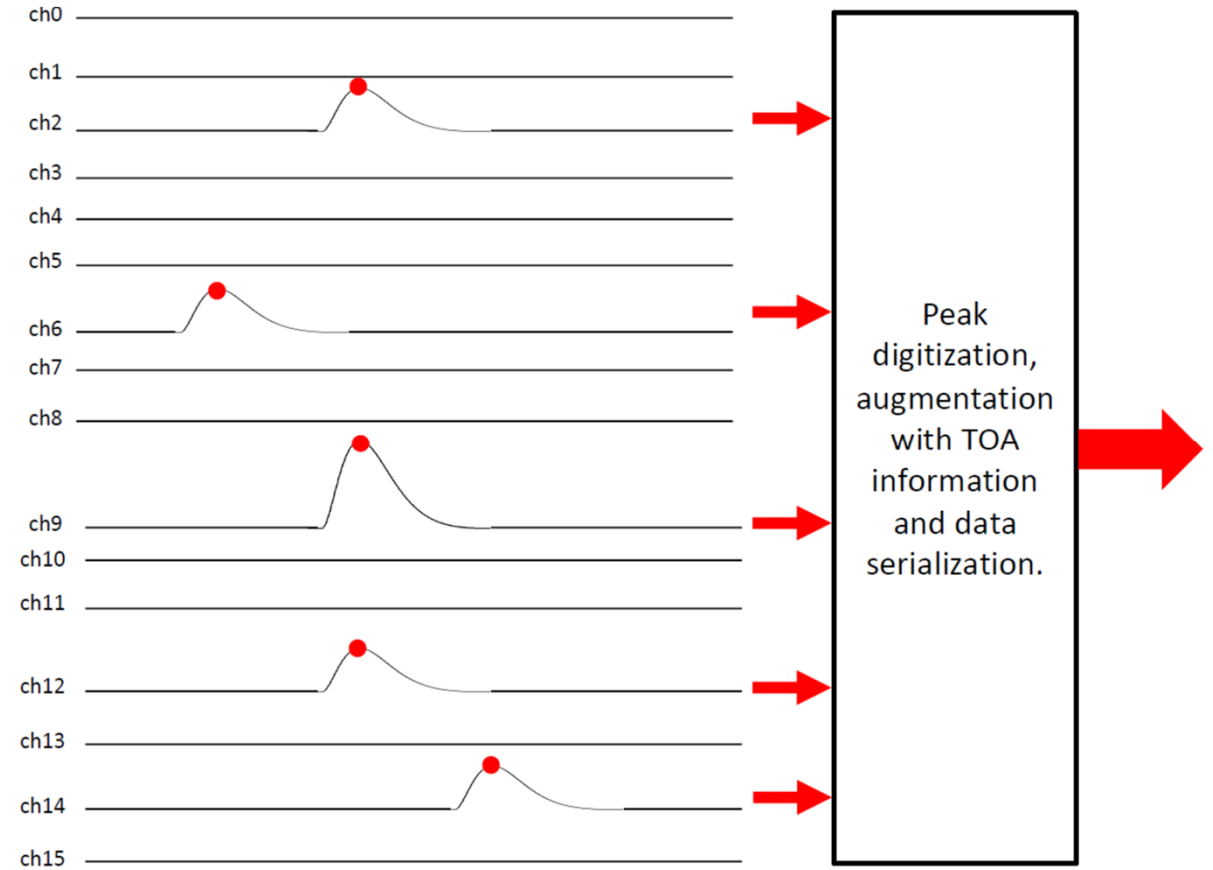


1. nEXO photo detection RO similar to DUNE TPC RO with combined ADC and data transmission in one chip while settling on a separate Front-End as a modified LArASIC for reading out SiPMs
2. Two-ASIC solution seems to be the optimal solution, allowing best using fabrication processes, separating analog and digital functionalities and allowing independent optimization of both
3. Also, the two ASIC solution allows maximal flexibility, i.e. one universal ADC-transmission ASIC can be coupled to a variety of front-end ASIC

Streaming v.s. Data Push



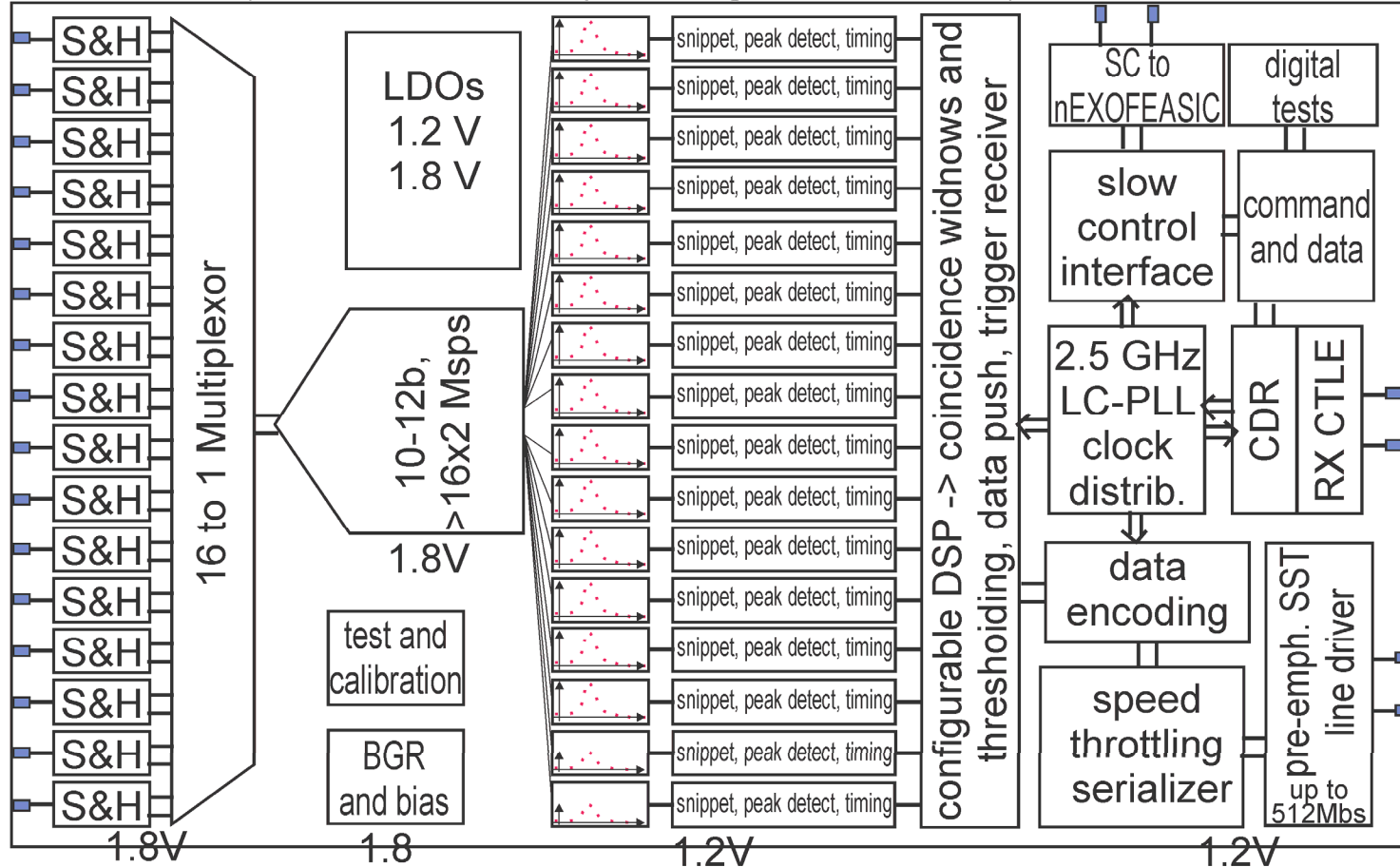
Streaming all digitized waveform samples off



Sending extracted waveform features (amplitude, ToA, pID, direction etc.) off

Two-ASIC Solution for nEXO

nEXODASIC (data conversion, data processing and transmission)



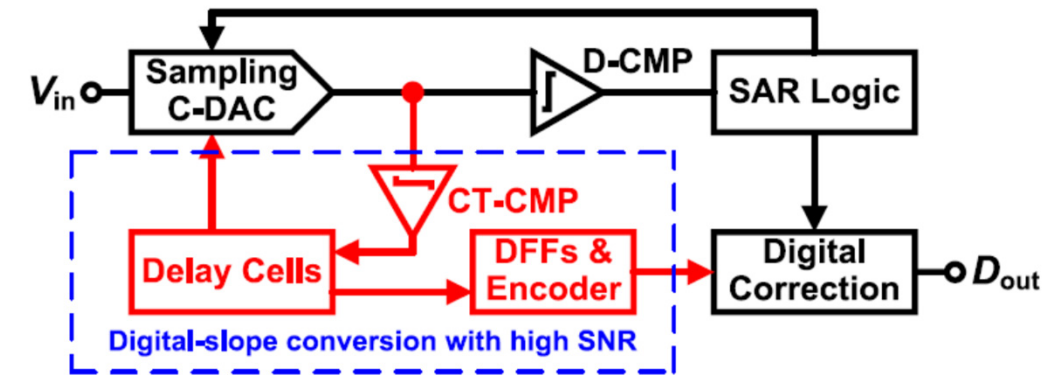
Main design components: FE buffers and multiplexor, time-interleaved ADC, DSP (AI or FIR filters), transmission encoder, serializer, X Gbps line driver, CDR-PLL, command and slow control interpreter, embedded testability, LDOs, etc.

1. Pushing most processing into the digital domain, including
 - a. finding of extremum and time of arrival
 - b. handling pileups
 - c. extraction of additional pulse features
2. Emphasis on power consumption
3. Use of 1.2 low voltage for transmitter and receiver circuits
4. Configurable transmission modes with data push as baseline (<50Mbps), but also allowing sending unprocessed data (~500Mbps)
5. Simplified interfaces: one link up and one link down
6. Combining all signals encoded into one down-link receiver
7. Configurability of embedded processing

Building Block #1: Fast, LP ADC

Low-power 12-bit hybrid ADC design in 65 nm CMOS:

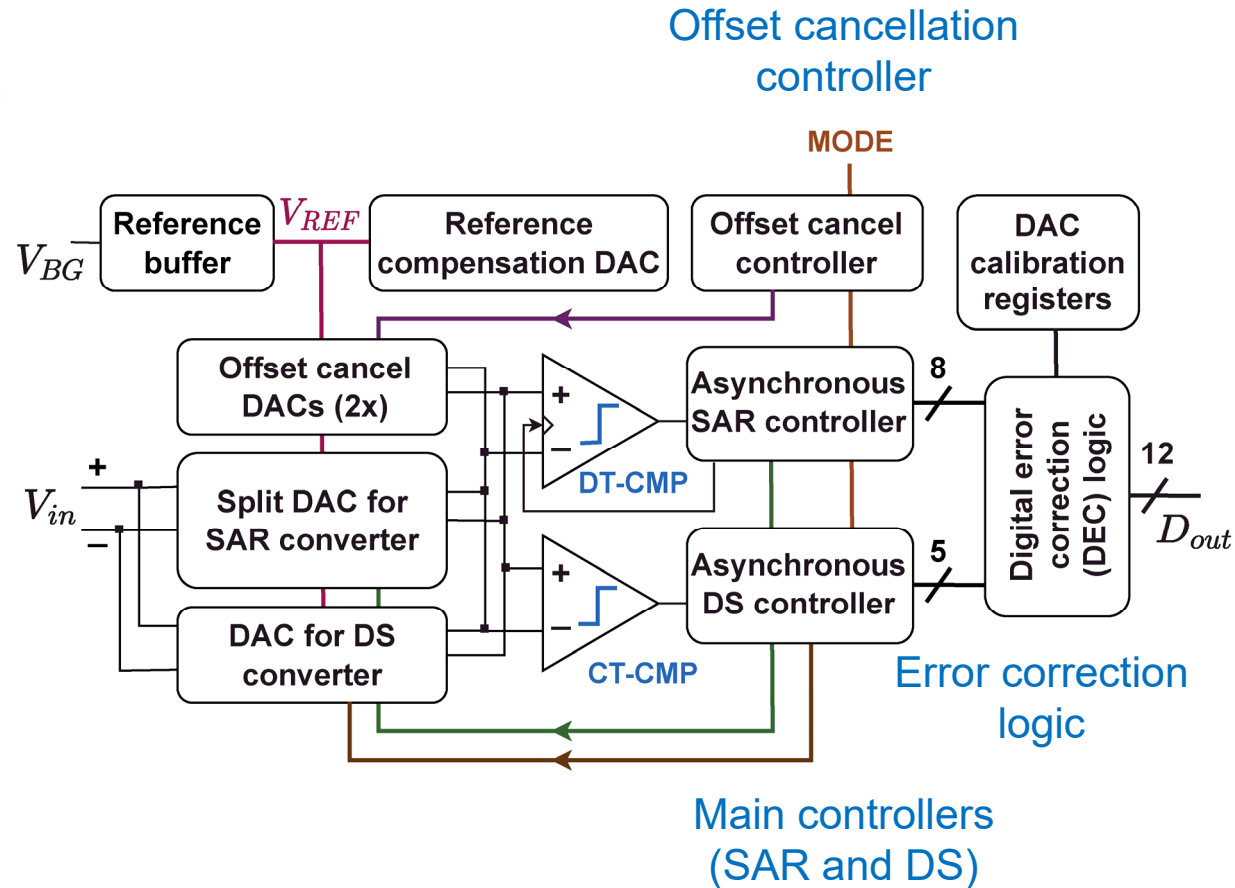
- **Overall:** 8-bit SAR (MSB) + 5-bit digital slope (LSB).
- SAR/digital slope boundary uses 1 redundant bit for robustness, thus resulting in 12-bit resolution.
- **Asynchronous successive approximation (SAR) converter:**
 - Fully-differential charge redistribution architecture.
 - Split capacitor DAC ($C_{\text{unit}} = 20 \text{ fF}$) using an energy-efficient merge-and-split (MS) switching scheme.
 - Uses one redundant conversion cycle (9 cycles for 8 bits) to obtain robustness to comparator noise and V_{REF} settling error.
- **Asynchronous digital slope (DS) converter:**
 - Asynchronous (self-timed) delay line-based architecture to ensure low power and robustness to PVT variations.
 - DS capacitors ($C_0 = C_{\text{unit}}/8 = 2.5 \text{ fF}$) are laid out within the SAR DAC to minimize SAR-DS gain mismatch and simplify calibration.
- **Additional features:**
 - On-chip reference buffer w/ cancellation of switching transients.
 - On-chip digital calibration of comparator offset; supports off-chip calibration of DAC capacitor mismatch.



Preliminary performance specifications

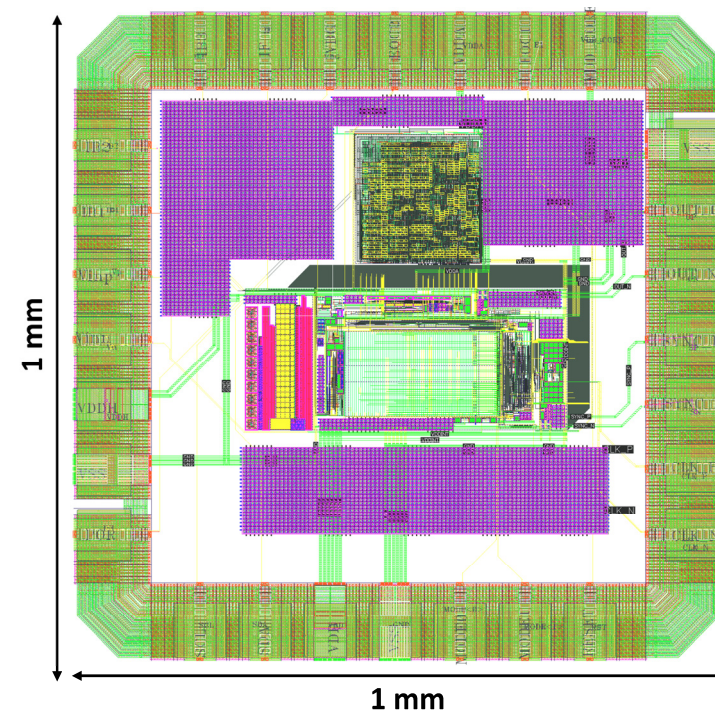
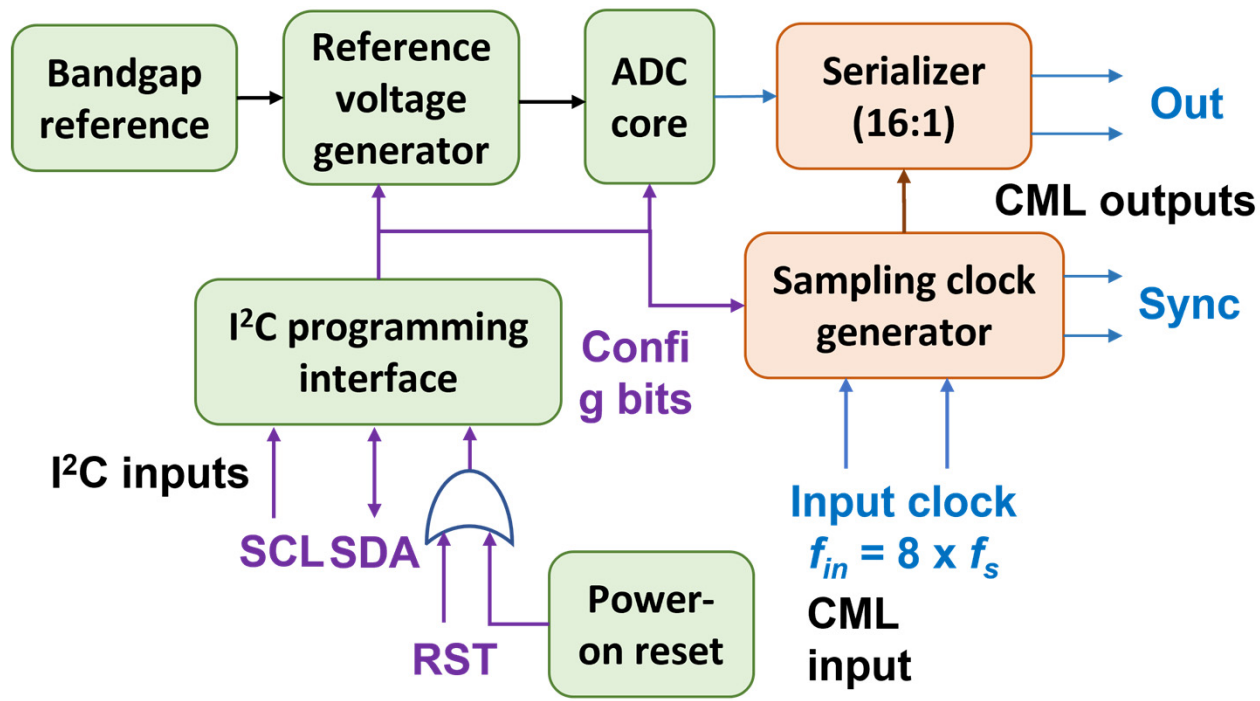
Parameter	Value
Sampling rate	Up to 50 MS/s
Output resolution	12-bit
Full-scale voltage	$1.7 V_{\text{pp}}$
Effective no. of bits (ENOB)	11.0
Core power (at 50 MS/sec)	820 μW
Reference buffer power	1.15 mW
Walden FOM (including buffer)	19.5 fJ/bit

ADC - Details



- Includes four major operating modes:
 - Normal operation
 - Discrete-time comparator (DT-CMP) calibration
 - Continuous-time comparator (CT-CMP) calibration
 - DAC capacitor mismatch calibration
- All digital logic is realized inside deep N-wells to provide isolation from on-chip analog circuits.
- Uses separate analog and digital power supplies ($V_{DD} = 1.2\text{ V}$, $V_{DDA} = 1.8\text{ V}$).
 - The analog supply is used by the band-gap reference (V_{BG}) and reference buffer.
- Delay tuning bits within the controllers can be externally set (2-bit resolution).

ADC - Test Chip

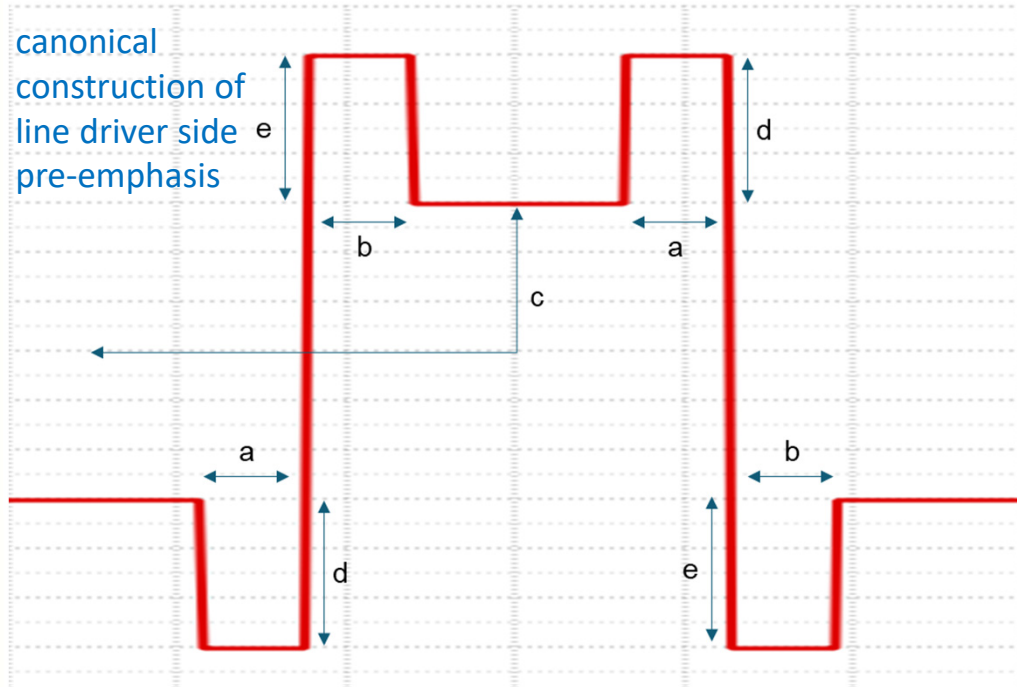


- The 1 mm² test chip integrates the ADC with accessory circuits (band-gap voltage reference, clock receiver, sampling clock generator, output serializer, serial programming interface, and power-on reset).
- Layout area of the ADC core (not including reference buffer) = 320 μm x 160 μm.
- Chip layout and verification is complete; queued for fabrication in mid-June.

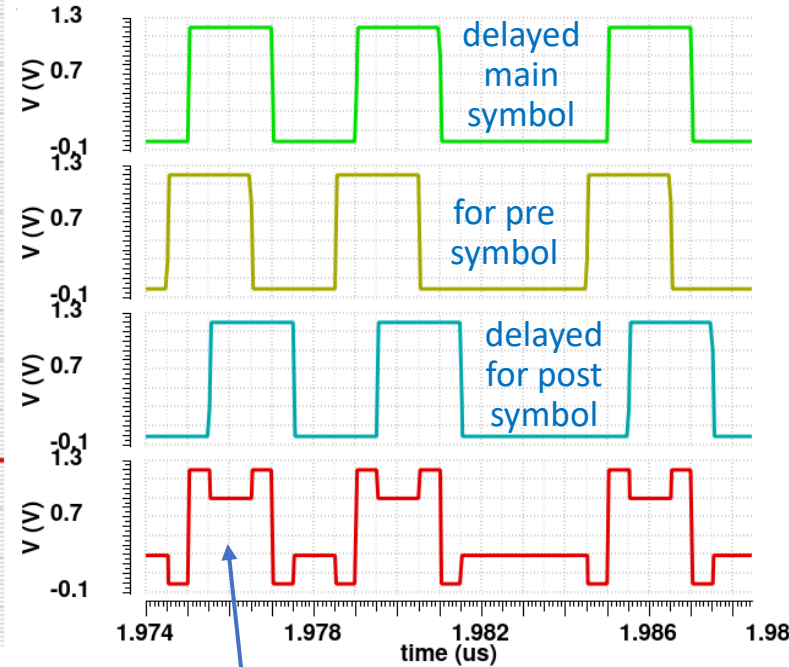
Building Block #2: LP Line Driver with User-Configurable Pre-Emphasis

Back to the definition: construction of pre-emphasis with DLLs and ganged SST drivers

- ~10% adjustability of 'a', 'b', 'c', 'd', 'e' variables with respect to UI is desired
- for the nEXO Taiflex cable, the best settings were found: 'a' \Rightarrow 10% of UI; 'b' \Rightarrow 90% of UI; 'c', 'd', 'e' \Rightarrow 0.5*VDD

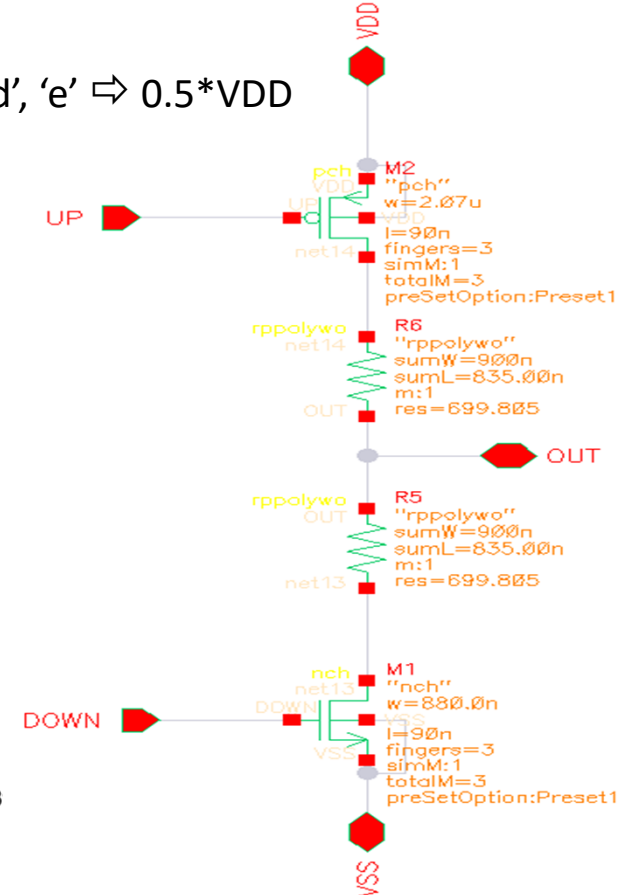


- a: Duration of pre-emphasis prior to edge transition
- b: Duration of pre-emphasis after an edge transition
 - c: Normal logic level (no pre-emphasis)
- d: Pre-emphasized level prior to edge transition
- e: Pre-emphasized level after edge transition



combined result sent onto the line

SST Driver Unit



Source-Series Terminated (SST)

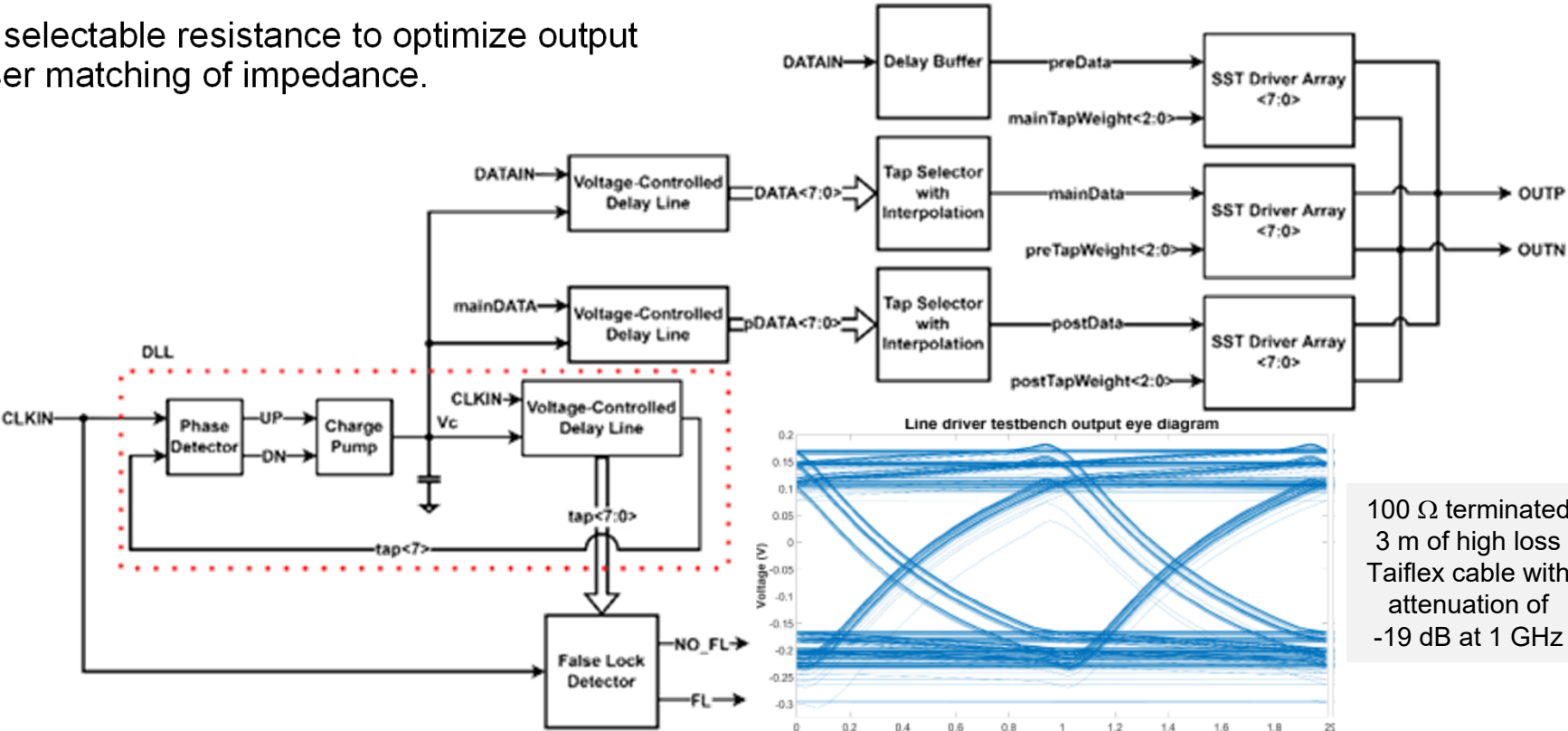
Only one side terminated

no CML driving

Line Driver

- three-tap Finite Impulse Response (FIR) filter is constructed with adjustable delays and weights for each
- adjustable delay is selected via an 8-Stage Delay-Locked Loop (DLL) and Digital Interpolators (DIs)
- False Lock Detector used for DLL to ensure no degradation in performance
- weights are configured by selecting the number of Source-Series Terminated (SST) drivers enabled in an array
- data is fed into Voltage-Controlled Delay Lines (VCDLs) controlled by the DLL to create delayed copies that are selected via the DIs
- SST drivers are implemented with selectable resistance to optimize output impedance for a low-power or closer matching of impedance.

Parameter	Value
Data Rate	Up to 2 Gb/s
Min. Relative Tap Delay	$1/16 \cdot UI$
Min. Tap Amplitude	75 mV
Non-Driver Power (at 1Gb/s)	2.4 mW
Total System Power (at 1Gb/s)	7.2 mW

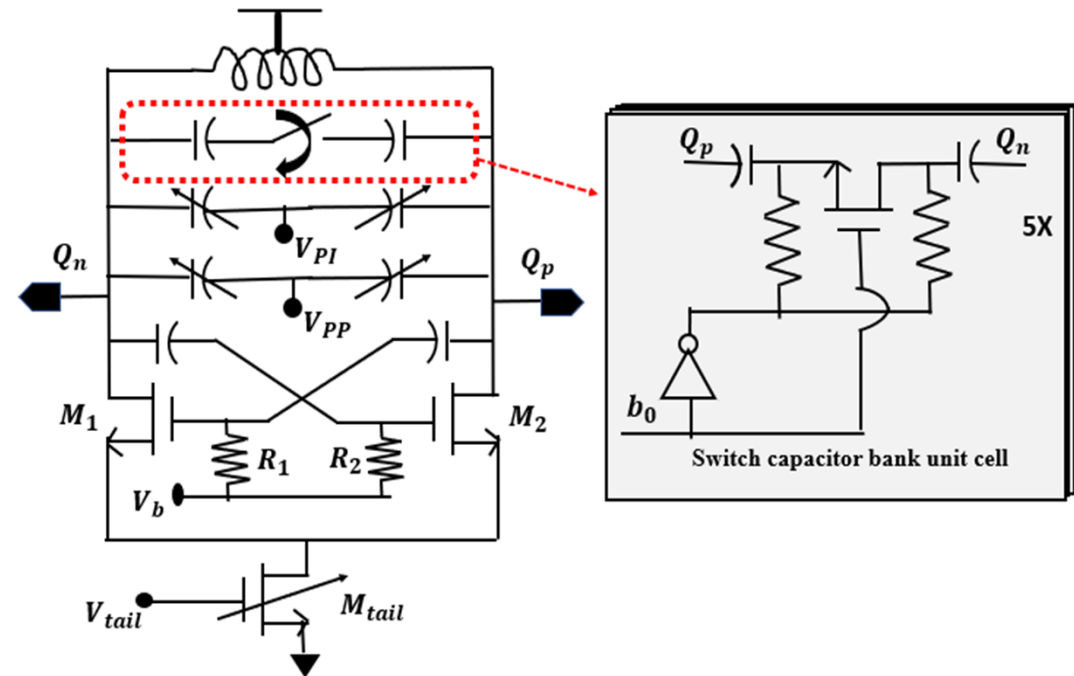


100 Ω terminated
3 m of high loss
Taiflex cable with
attenuation of
-19 dB at 1 GHz

Building block #3: Efficient data readout architectures – slides 14-15

Building block #4: LC PLL

- Potential specifications for a universal PLL/CDR for digital FE ASIC
 - VCO operating frequency ~6 GHz,
 - Programmable divider to support a variety of clock frequencies and data rates,
 - Loop bandwidth in CDR mode > 2 MHz,
 - Loop bandwidth in PLL mode > 20 kHz,
 - Extended to Cryogenic Temperature Range of operation,
 - Guaranteed operation up to 500 Mrad,
 - Immune to SEE



Summary

- Presented a few areas of the BNL's ASIC development related to HEP and NP
- Many subjects are not even touched
 - AI/ML embedded in FE
 - MAPS for the EIC
 - Pixel detectors for X-ray detection
 - Projects for other funding sources

***Work of the current BNL's ASIC team:
Soumyajit Mandala, Sandeep Miryala, Venkata
Narasimha Manyam, Giovanni Pinaroli, Nick St. John,
Dominik Gorni, Grzegorz Deptuch***

and many other designers



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He/She will be developing state-of-the-art integrated circuits in modern CMOS/BiCMOS and OPTO technologies.

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Dr. Gabriella Carini (carini@bnl.gov) or Dr. Grzegorz Deptuch (gdeptuch@bnl.gov)

