# Collaboration & Archived Effort to boost design efficiency & Intellectual input into new design

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Ideas collected in Snowmass IF7 White paper https://arxiv.org/abs/arXiv:2204.07285

"Enabling Capabilities for Infrastructure and Workforce in Electronics and ASICs"

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Background assumptions for informing the Snowmass about future needs in Readout systems increasingly supported by ASIC design capability

To maintain and evolve the expertise gained in the design of high granularity detector systems with detector mounted electronics designed to cope with extreme environments.

To educate and retain a skilled work force, as well as find ways to speed up & keep up with the pace of tool developments needed to validate our designs.

To utilize predictable needs and important ASIC support:

Design and maintain widely needed critical circuit blocks with current day technologies: pll's drivers/rcvrs delay blocks...... Make materials available that describe Design techniques and details of particular (block) designs are especially valuable to the new designer and can largely be communicated without compromise of NDA's.

Some could be shared as completed blocks either as an example or dropped into new designs in the same technology.

# Breakdown of Traditional Methods of Information preservation & designer community awareness

- Guidance from experienced designers fails by attrition as time between projects increases.
- Becomes less relevant/distributed as the evolution of tools and requirements scale inversely with feature size. Its hard to keep up...
- As Systems grow in scale/complexity: Verification techniques increase in variety & complexity and environmental requirements evolve.

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# Solutions for an evolved problem

- Provide a broad National HEP resource, a searchable Archived Memory for:
- Links to HEP detector design documentation.
- Design specific optimization approaches and test bench developments.
- Detector System specific FAQ's: how element size or modularity or other design parameters are optimized / chosen
- Include Self-guided training with examples for system/sub-system blocks.
- Hierarchical working areas for the creation and modeling (or modeling results) of from successful detector system and sub-system designs.
- sub-system interface documentation
- sub-system designs
- Lists of System requirements & system dependencies.

# continued.. Solutions for an evolved problem

- Maintain/update names of supported PCB and ASIC CAD design platforms, tools, design flow examples.
- Provide specific ASIC design examples using currently available tools and archive FAQ's (avoiding NDA violating information)
- Provide Link locations & storage for community driven technical assistance.

#### continued.. Solutions for an evolved problem

List/support Verification Techniques & tools with current examples

- PCB
- FPGA
- ASIC
- Hierarchical System
  - Functional
  - Mode tests with throughput verification

#### How & Where

#### How is not terribly difficult to imagine...

Evolve our Human Information and training systems with GIT or similar archival system that the community already uses.

Fund an Information center using technicians willing and interested in keeping up with State-of-HEP/NP- design Art

#### Where:

FNAL.. As primary host for repository & top level organizational expertise.

But with satellite (distributed) groups that follows the expertise where access and updating are natural.

Provide a communictions channel like Slack so there is reward in being informed from people that are new or just blindsided by the information revolution.

Make editing by vetted persons a priority, a privilege so that management overhead doesn't overwhelm a good idea.

#### More on Evolved issues: Design Complexity

It was recently observed that as HL-LHC Designs were coming to a close that ASICs were falling behind their projected completion schedules.

The cause seems to be that as smaller feature size technologies have been implemented to meet higher precision / channel count system requirements the number of tools, expertise and time required to bring an ASIC or a system of ASICs to production ready levels has significantly increased.

There are likely several paths to a satisfactory answer.

## Coping with Design Complexity

ASIC designers/design groups have a strong desire to provide satisfying answers to complex design requirements through the magic of modern technology.

At the outset costs and schedules are proposed in good faith but is highly likely that only one of these is revised as the planning proceeds. Incubating a Crisis in a far away future....

- → Potential Mitigations to avoid an "ASIC Crisis"
- Collaborate on Designs by sharing responsibilities exploiting design management tools to divide up the tasks among institutions.
- Set development schedules according to the time it takes for the *funded ASIC team* individuals to utilize existing and learn new tools and include conservative verification schedules adding time for not yet vetted verification techniques. Don't get behind on a schedule that your not fully supported to meet.
- → Either stretch out the time for the available team or add technical help within or outside the collaborating group.

## Collaborating on Projects. What to do & not to do

Perhaps best covered by survivors of the RD53 experience which seems pretty reasonable from the outside of the box.

And the Cold ASIC experience of the DUNE collaboration.

#### Open Access ...

Seems quite promising/enabling as an approach for both collaboration and training. We may be on the footsteps of a design revolution. So we should talk about how to engage while keeping one foot in both worlds.

## Additional Town Hall discussion Points

#### Education & Specialized Experience

The Snowmass process offer our community the chance two offer up ideas for educational initiatives along the lines of traineeships in system design and ASIC design. These go hand in hand in the design of large or small scale detector systems.

One needs to know the motivation for designing an ASIC to realize its benefit in the system.

Conversely one needs to know the plausible set of reasons for implementing an ASIC in a system to be a good reviewer as many grad students and post docs will become.

#### Potential Instrumentation Training that could be supported by DOE

Multi-year Internships at National Labs. --

 One week Schools for interested Experimental HEP grad students with a training certificate to list as a CV bullet.

See Local Adds for

**HEPIC Summer Week 2022**