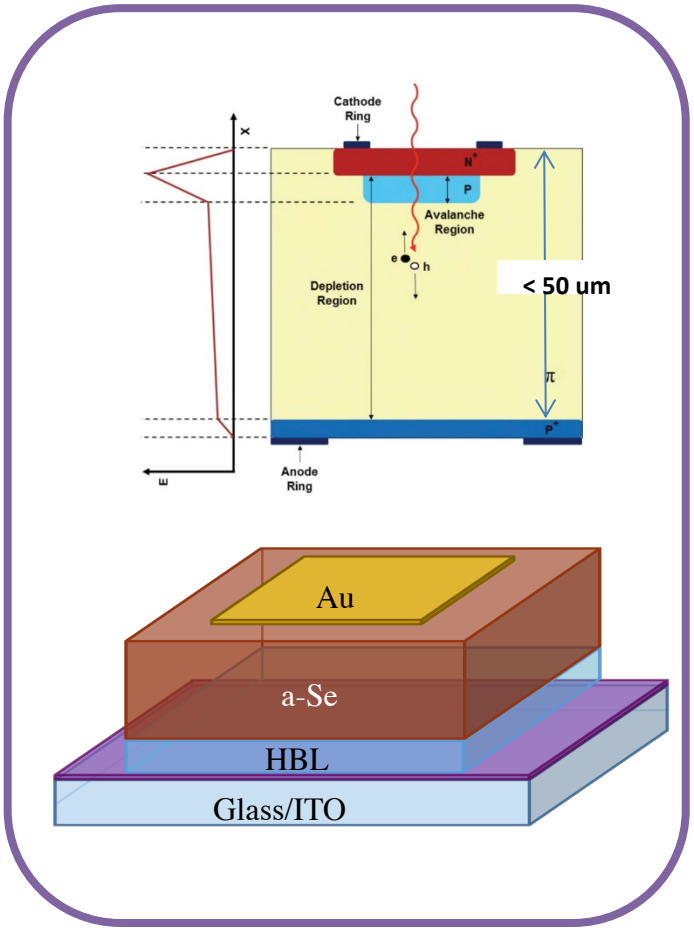


An Update on Low Gain Avalanche Detector (LGAD) & a-Se Avalanche Detector and their ASIC Integration

Hartmut Sadrozinski, Shiva Abbaszadeh

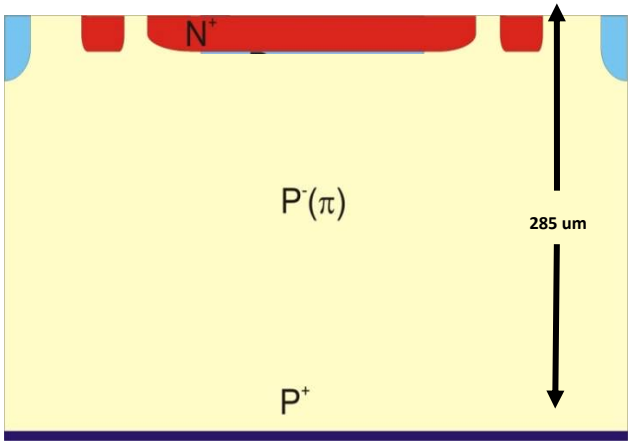
2022 HEP IC Meeting

May 18, 2022

Low-Gain Avalanche Detectors (LGAD)

"Simple" extension of silicon detector results in perfect sensor for timing

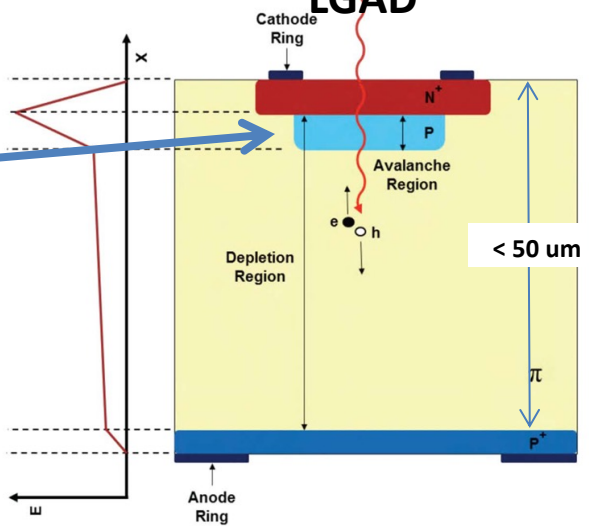
N-in-p PIN



Create **high field**
by introducing
gain layer
to increase signal

Reduce t**hickness**
to decrease
rise time

LGAD



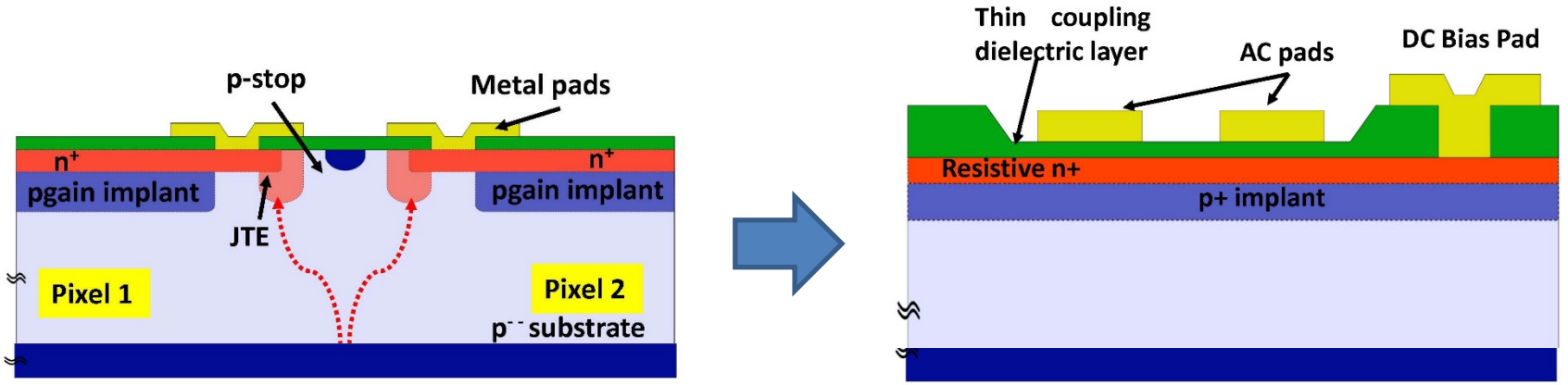
LGAD have large and fast signals

G. Pellegrini *et al.*, Technology developments and first measurements of LGAD for high energy physics applications, Nucl. Instrum. Meth. A765 (2014) 12 – 16.
H.F.-W. Sadrozinski, A. Seiden and N. Cartiglia, 4D tracking with ultra-fast silicon detectors, 2018 Rep. Prog. Phys. 81 026101.

Extension of LGAD : AC-LGAD (aka RSD)

Difference between LGAD and AC-LGAD appears to be small:

- make n++-implant at the junction slightly resistive and extend it as a continuous sheet across the entire sensor-> resistive silicon detector RSD
- add di-electric layer for isolation and AC-coupling into pads of optimized size and position



Result:

- Simplification of design and production (no p-stop, Junction Termination Extension, inter-pad gap)
- 100% Fill-factor
- Sparse readout (power savings)
- AC-coupling affords ease of testing (like usual silicon strip sensors, which are AC-coupled)

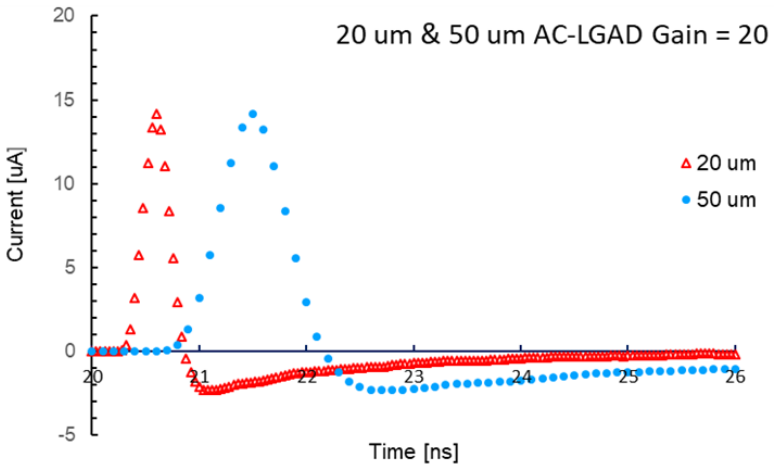
M. Mandurrino et al., "Demonstration of 200-, 100-, and 50- micron Pitch Resistive AC-Coupled Silicon Detectors (RSD) with 100% Fill-Factor for 4D Particle Tracking", IEEE Electron Device Letters, vol. 40, no. 11, pp. 1780-1783, Nov. 2019.

US patent No.: 9,613,993 B2 "Segmented AC-coupled readout from continuous collection electrodes in semiconductor sensors", H. Sadrozinski, A. Seiden (UC Santa Cruz) and N. Cartiglia (INFN Torino), granted on April 4, 2017

Fast LGAD Read-out ASICs at SCIPP

The development work of LGAD sensors was/is based on high-speed readout boards with discrete components introduced by SCIPP.
The crucial characteristics of LGAD signals were mapped out.

Measured Pulse shapes of AC-LGAD



LGAD Characteristics	50 um	20 um
Rise Time (10-90%) [ps]	455	182
Input Charge (G = 20) [fC]	11	4.6
I_{MPV} Input Current [uA]	15	15

It allowed to come up with specifications for different applications in terms of temporal and spatial resolution and the double pulse capability and translate them into required performance parameters for ASICs (“Design Goals”).

Design Goals

ASIC Parameter	50 um Sensor	20 um Sensor	Comment
Rise time (10 – 90%) [ps]	455	182	Rise time (electronics) = Rise time (sensor signal)
Jitter [ps]	10	5	< 30 % of the predicted “Landau” Noise
S/N	> 50	> 40	S/N = Rise Time / Jitter
Voltage signal [mV]	70	70	$V_{MPV}=R_{FB}*I_{MPV,}$ [R_{FB} = 5 kΩ]
Noise RMS [mV]	1.4	1.8	N = S/(S/N)
Internal Sensor Gain	> 20	> 20	

ASICs under Test at SCIPP

Based on the Specifications, three ASICs are being produced which will emphasize different performance goals.
Here we leverage our partner's familiarity with the technology and our experience with sensors and readout systems.

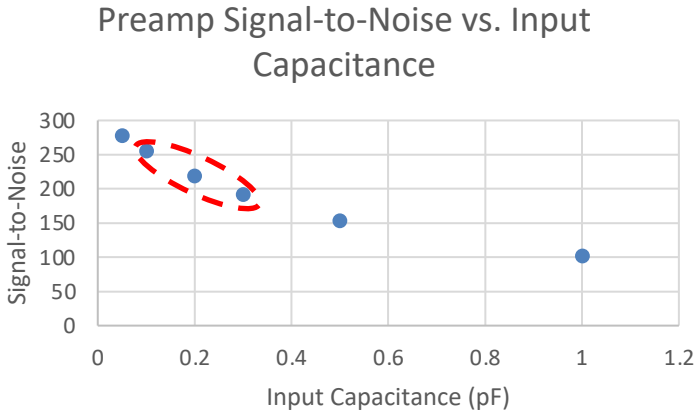
Institution		Technology	Output	# of Chan	Funding	Specific Goals	Status
INFN Torino	FAST	110 nm CMOS	Discrim.	20	INFN	Capacitance > 4 pF	Testing
NALU Scientific	HPSoC*	65 nm CMOS	Waveform	5 (Prototype) > 81 (Final)	DoE SBIR	Digital back-end	Testing
Anadyne Inc	ASROC**	Si-Ge BiCMOS	Discrim.	16	DoE SBIR	Low Power	Layout Board design

* HPSoC : High Pitch digitizer System on a Chip,
(L. Macchiarulo et al.: "Design of HPSoC - a 10GSa/s Waveform Digitizer for Readout of Dense Sensor Arrays", submitted to IEEE NSS-MIC 2022)

** ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout,
(G. Saffier-Ewing et al., "ASROC: A custom amplifier/discriminator IC designed for AC-LGAD readout " , TWEPP 2021)

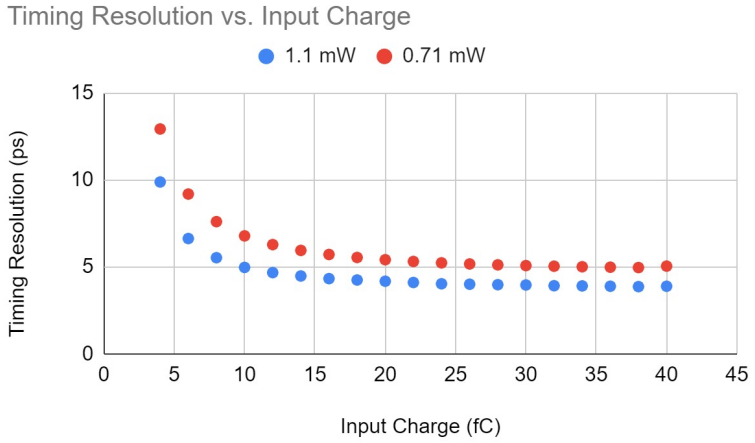
Example: Anadyne ASROC Simulated Performance

Input capacitance increases noise and rise time
"AC-LGAD's low input capacitance is very welcome"
Signal-to-noise for 10 fC pulse and 800 uW/channel is very large for pad detectors.



Jitter vs input Q for two Power Settings (preamp + discriminator) (C_{in} = 200 fF)

	Power @ R.T. [mW/channel]	
Input Q [fC]	0.71	1.1
4	13 ps	10 ps
5	11 ps	8 ps
10	7 ps	5 ps



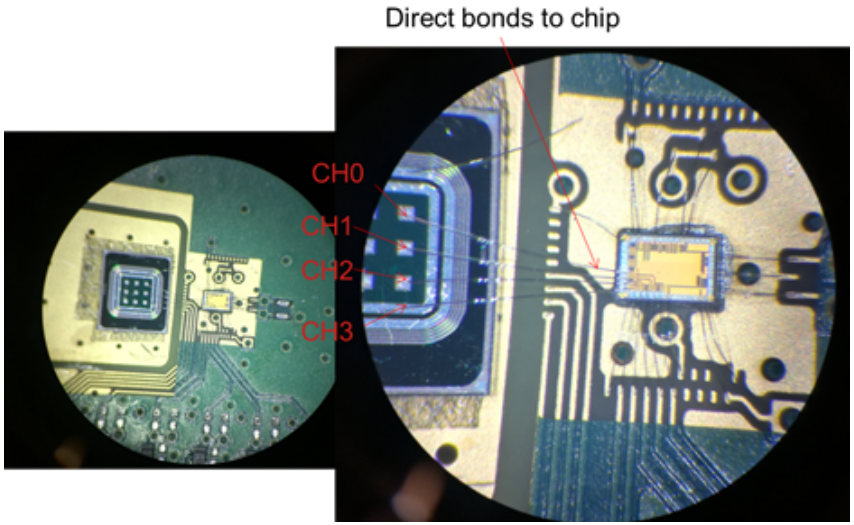
At low signals, we expect only modest improvement in jitter for large increase in power

(The power/performance tradeoff is entirely in the preamp)

Very Preliminary Test Results with HPSoC

The HPSoC was tested with fast calibration pulses to verify the performance of the first stage, the Trans-Impedance Amplifier (TIA).

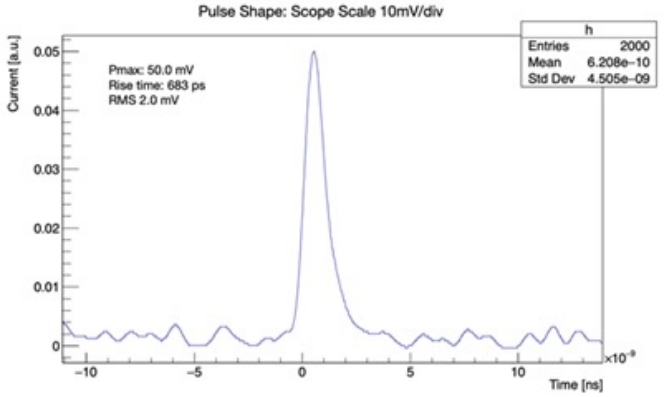
It was then mounted on a test board and wire bonded to a 60 um thick AC-LGAD pad sensor and tested with β.



The expected analog performance of the ASIC can be derived from the analysis of the pulse shapes.
The contribution to the time resolution due to the electronics is the jitter

Jitter = rise time / (S/N)

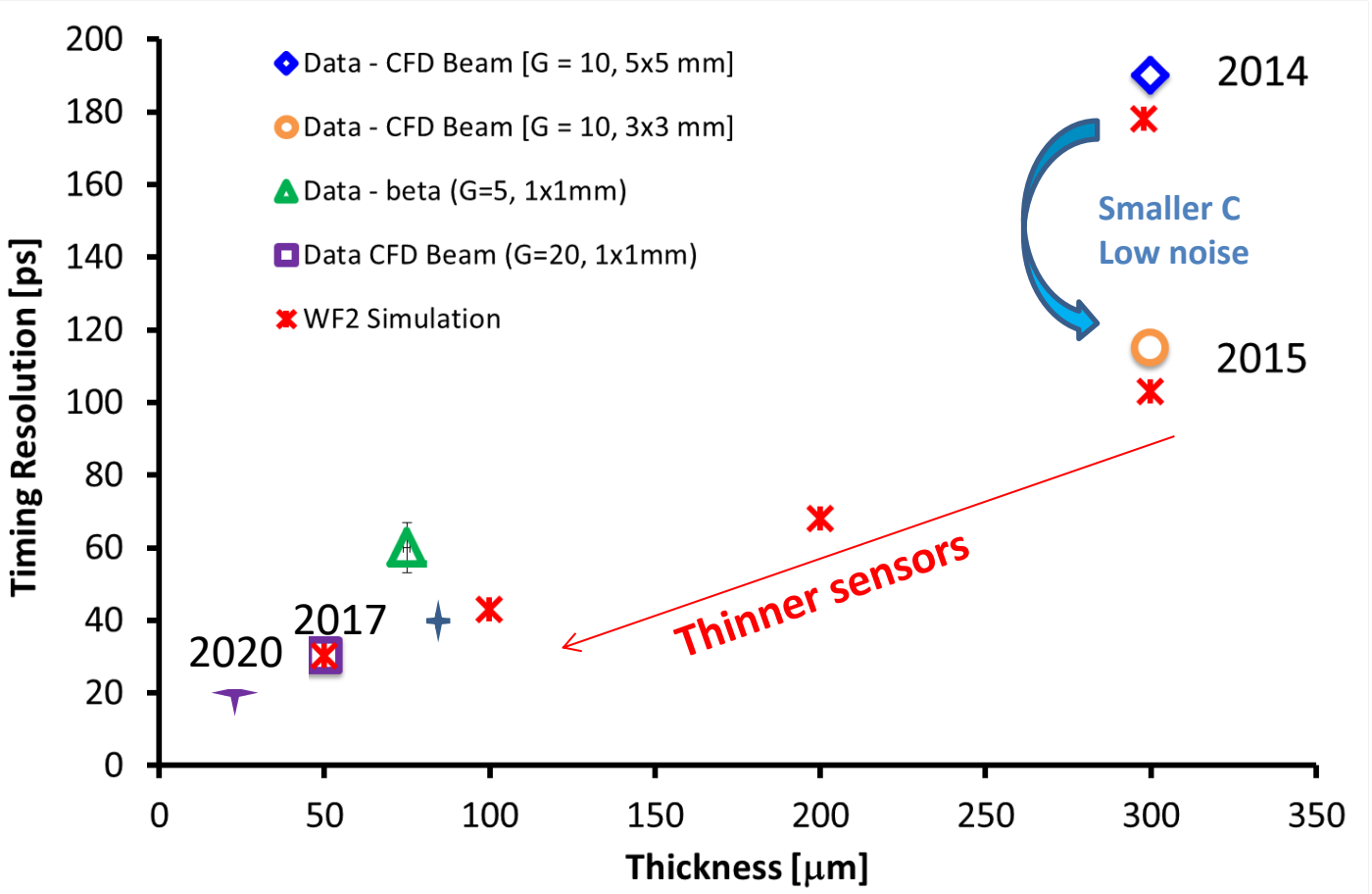
Its parameters can be measured pulse-by-pulse and then extrapolated to the final ASIC – sensor combination.



Most important is the short rise time and the very low noise which allows to predict a jitter of the order 10 - 15 ps for the final ASIC version and 50 um thick AC-LGAD.

Abstract & Summary submitted to TWEPP 2022

Phase II: Trend of Time Resolution

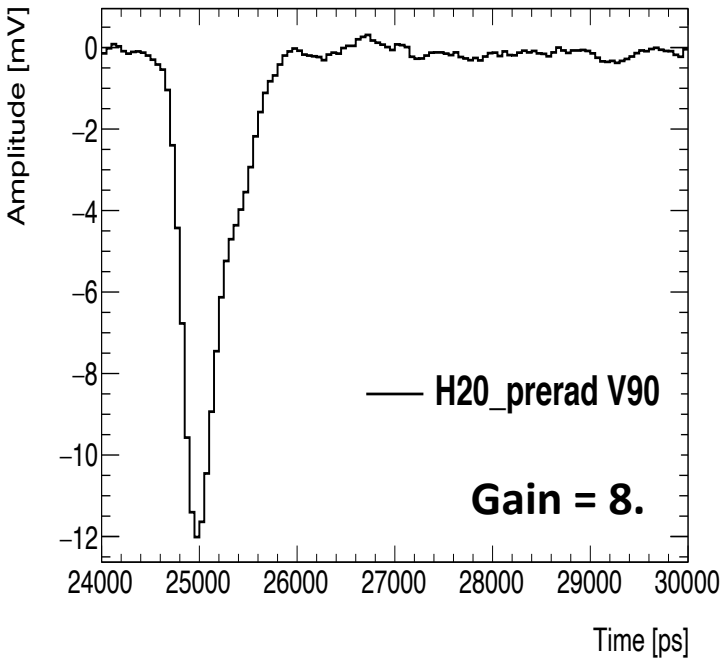


The temporal resolution as a function of LGAD thickness is well simulated by WF2.

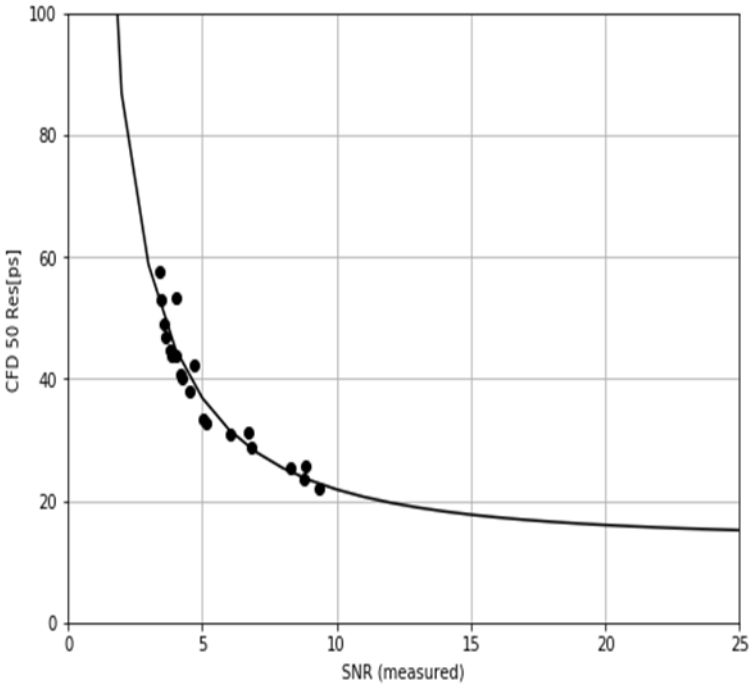
F. Cenna, et al., "Weightfield2:", NIM A796 (2015) 149

Phase II: 20 µm LGAD offer good Time Resolution

Averaged Pulse for 20 micron thick LGAD



Temporal resolution vs. Signal-to-Noise Ratio



Signal much larger than baseline fluctuations indicating very good signal-to-noise even with a gain of only 8.

Rise-time (10-90%) about 150 ps compared to about 500 ps for the 50 micron sensor.

Contribution to the time resolution from Landau fluctuations is proportional to the detector thickness so smaller for thinner detectors (expected to be ~ 15 picoseconds for the 20 micron thick sensor).

A. Seiden, et al, "Potential for Improved Time Resolution Using Very Thin Ultra-Fast Silicon Detectors (UFSDs)", https://arxiv.org/abs/2006.04241

Amorphous Selenium Avalanche Detector

Why a-Se?

High resistance → Low DC Dark Currents

High absorption coefficients from visible (E_G ~2 eV) to X-ray (<70 keV)

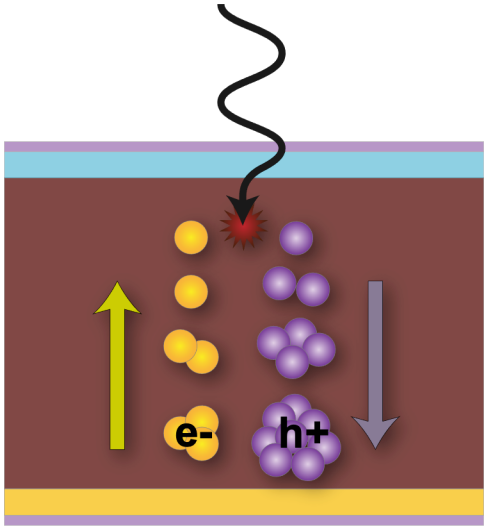
High Schubweg ($\mu\tau F < L$)

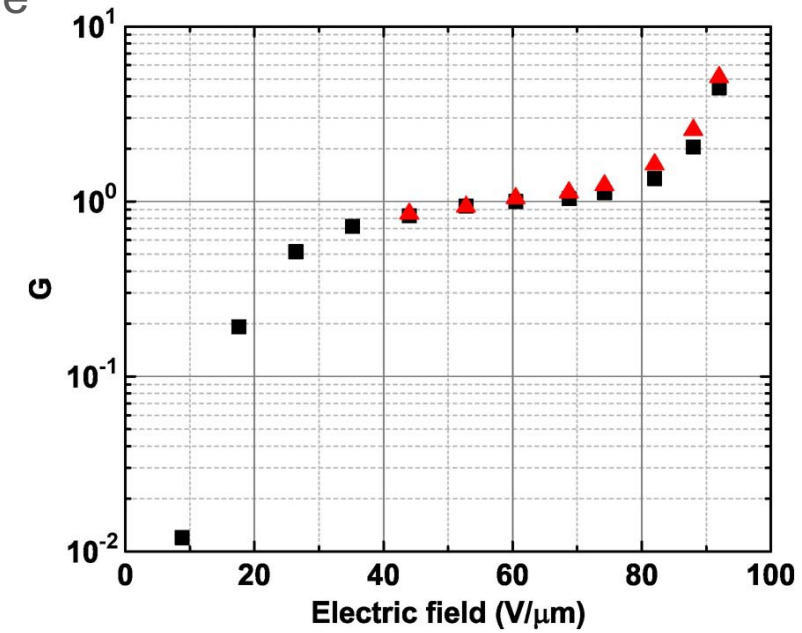
Low threshold for impact ionization/ avalanche multiplication (>65 V/um)

Low-cost, large area fabrication

Tunable properties through doping/alloying

Mature technology – already in use in mammography

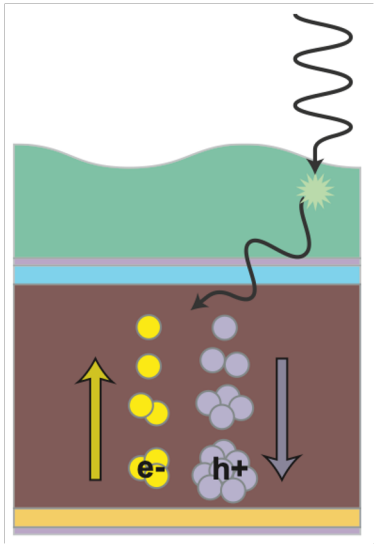


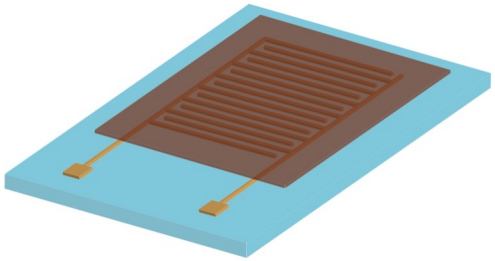


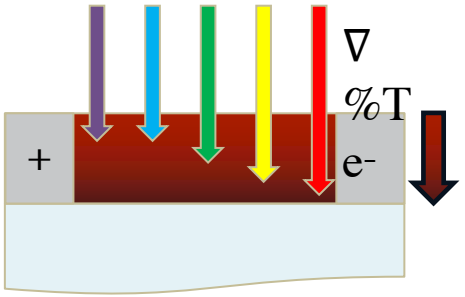
Abbaszadeh et al. IEEE Trans. on Elec. Dev. (2012)
DOI:10.1109/TED.2012.2204998

A-Se Prototype & Application

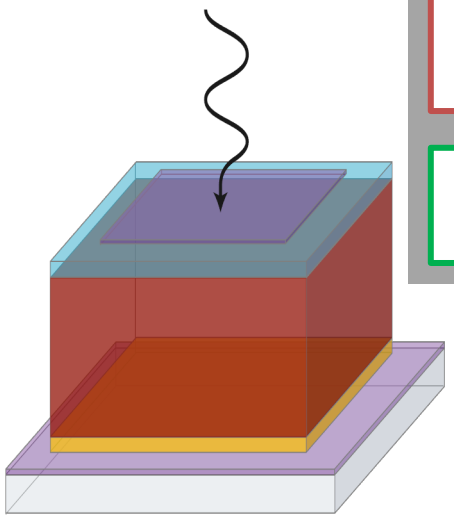
Allows for different applications in medical imaging, crystallography, high energy physics, threat detection

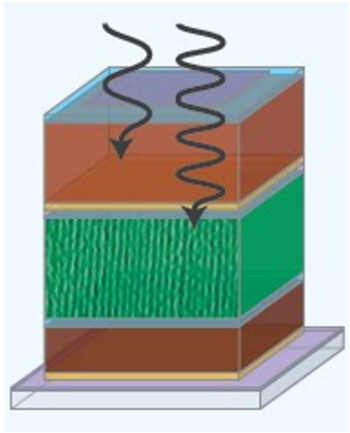






Vertical Structure	Lateral structure
Indirect conversion	UV to red detector
Up to 200 um vertical Structure	Dual Layer detector
Direct Conversion	High sensitivity w/o motion artifact



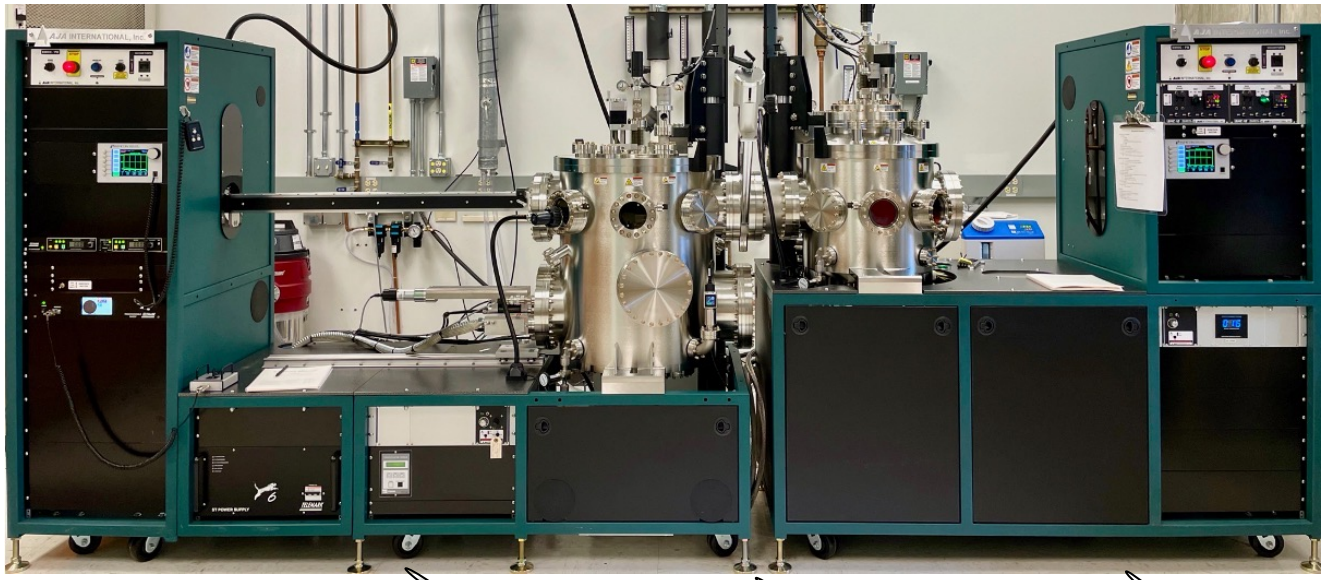


Dual-layer detector

Detector Fabrication Facility at UCSC

DTRA & DOE (High Energy Physics) Funded Active Projects

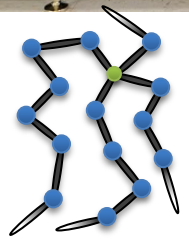
- Alloy a-Se to reduce avalanche threshold and improve gain
- Improve the stability of the device
- Explore applications in particle physics



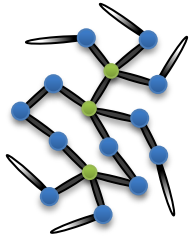
Se Alloying

Se

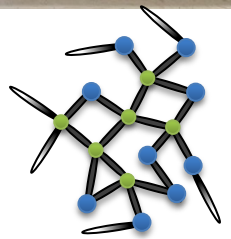
X



<r> = 2.13



<r> = 2.40



<r> = 2.80

Katie Hellier
Postdoctoral Researcher

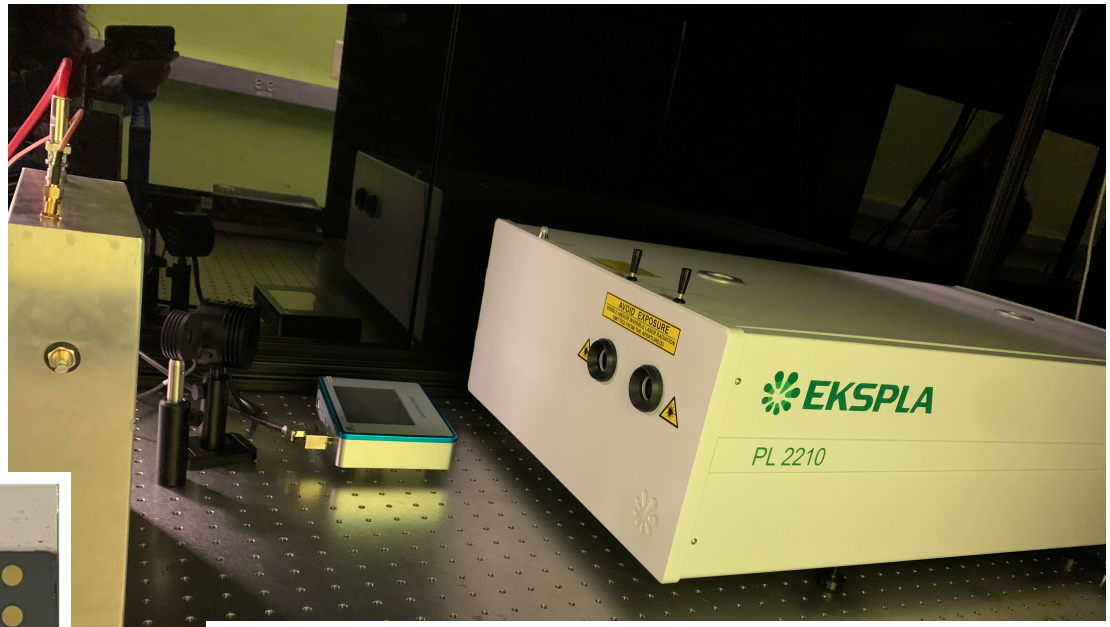
Akyl Swaby

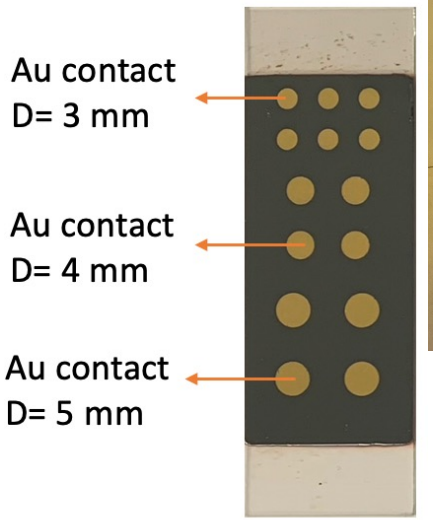
Mariana Huerta

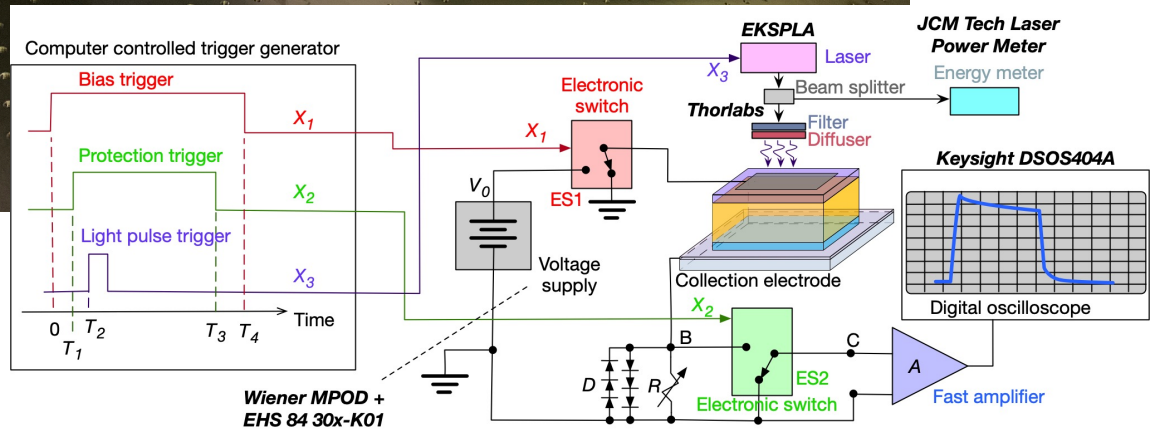
Akansha Elling

Hamed Tangestani

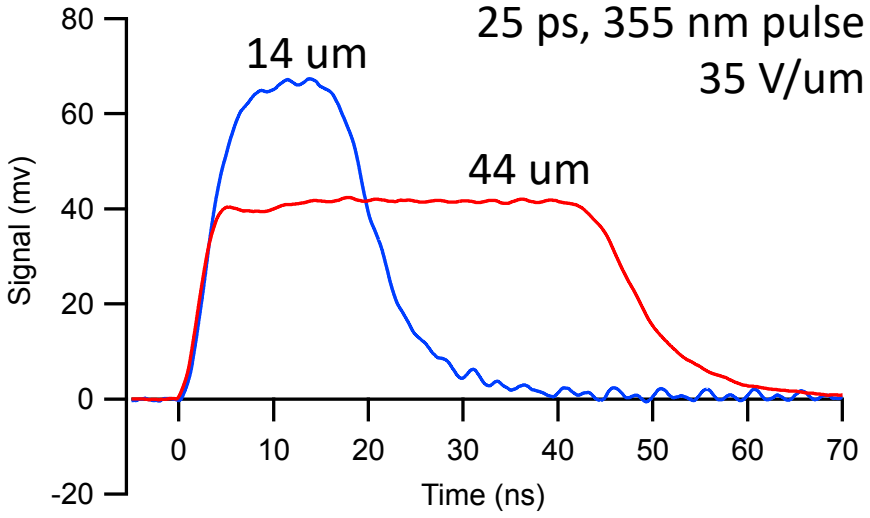
Time-of-flight Measurement



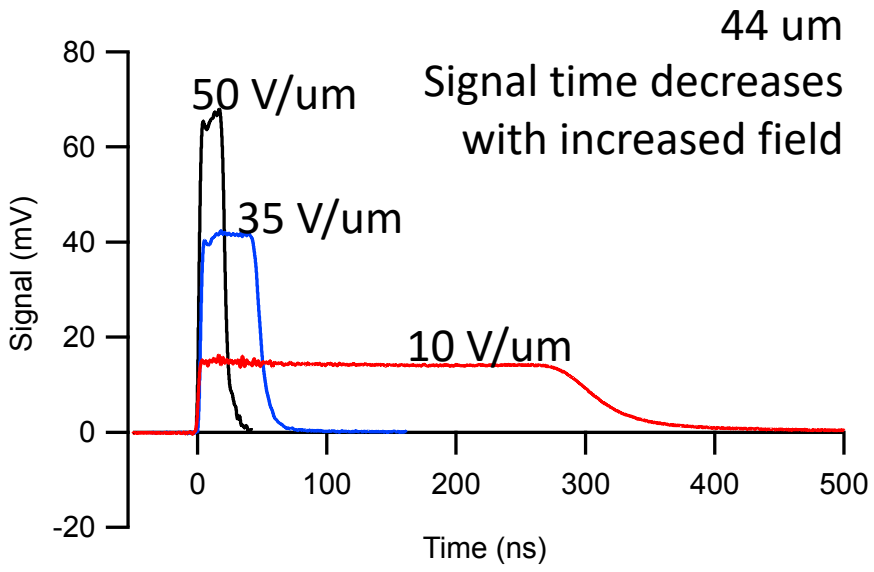


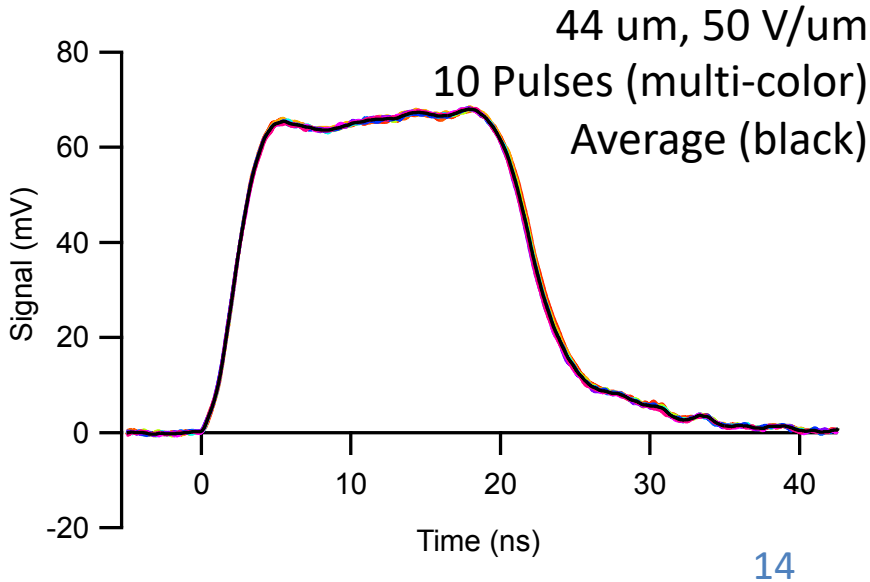


A-Se Photodetector Signal Performance



Characteristics (44 um)			
Bias	10 V/um	35 V/um	50 V/um
Rise Time (10-90%, ns)	2.5	3.1	3.3
Capacitance (pF)	24	24	24
Dark current (nA/cm^2)	0.1	0.7	1.5
Jitter (ps)	115	90	83





Available ASICs for a-Se Detector

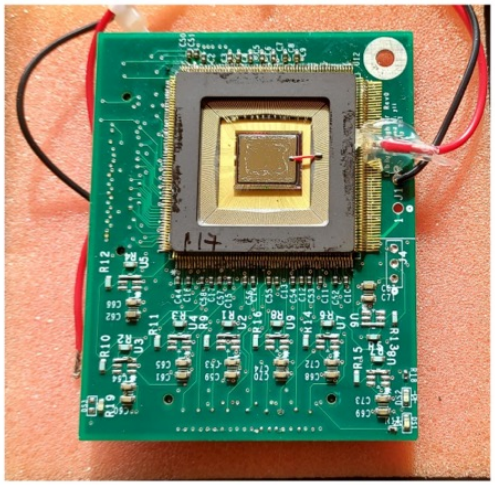
	Gain	Technology	Area (ASIC) [mm^2]	Area (Pixel/quadrant) [µm^2]	Power Consumption per pixel [µW/pixel]	ENC [*erms*]	Features
Top Metal-II *	196 mV/fC	350nm XFAB	8x9	83x83	1.2	15 (output- referred)	—-
RD53B **	—	65nm	20x11.6	50x50	~13000	100 (output- referred)	1.ToT 2.Leakage Current Compensation: 0-20 nA
KA Imaging	5 uV/e @ λ = 460 nm	180nm	3x3.4	7.8 × 8.7	—	89 (input-referred)	3T- Digital Readout

*Gao et al., "Topmetal-II(−): a direct charge sensor for high energy physics and imaging applications." JINST 11 (2016) 01, C01053. DOI: 10.1088/1748-0221/11/01/C01053.

** L. Gaioni et al., "Optimization of the 65-nm CMOS Linear Front-End Circuit for the CMS Pixel Readout at the HL-LHC," in IEEE Transactions on Nuclear Science, vol. 68, no. 11, pp. 2682-2692, Nov. 2021, doi: 10.1109/TNS.2021.3117666.

*** Y. Z. Li et al., "A Monolithic Amorphous-Selenium/CMOS Visible-Light Imager With Sub-9-µm Pixel Pitch and Extended Full-Well Capacity," in IEEE Sensors Journal, vol. 21, no. 1, pp. 339-346, 1 Jan.1, 2021, doi: 10.1109/JSEN.2020.3014073.

Integration to Readout

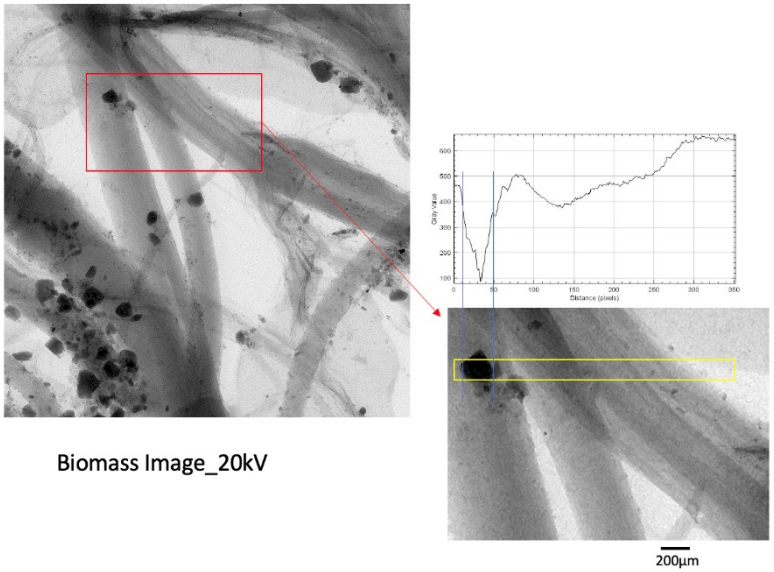


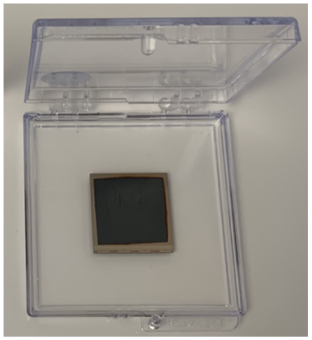
1Mp a-Se/CMOS Hybrid Detector with a 7.8 µm pixel pitch. The 1Mp detector package and analog daughter board are soldered to the test board.

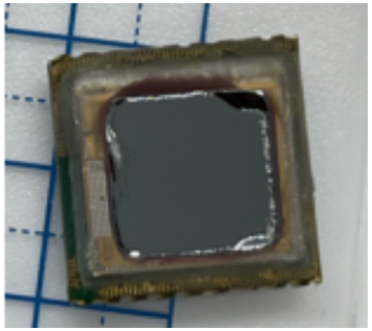
Lawrence Berkeley National Lab

Maurice Garcia-Sciveres

Yuan Mei







Development of high voltage a-Se detector on top of RD53B(left) and Topmetal II (right) CMOS ROIC.

In Summary…

- LGAD and a-Se present two different avalanche photodetector options
- There is a need for ASIC design based on the specific characteristics of a-Se device configurations for different application

Thank you!

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DOE grant number DE-SC0022343 & DE-SC0010107-005
and the DOE SBIR program