

The future is certain; it is only the past that is unpredictable

(Old soviet joke)

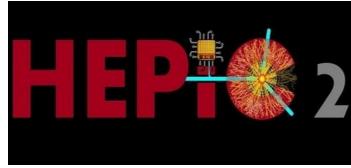
- First look back at prior HEPIC predictions
- Is there anything new after 10 years?
 - Was it predicted?



2022



2017



2013



Prediction scorecard

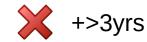
 We have been mainly working on HL-LHC chips in 130nm and 65nm CMOS.



 We are basically done with those chips and HL-LHC will start running next year



- Belle-II, Mu2e are also done (and Mu2e used ASICS)
- We are now working on ILC chips, soon to be followed by muon collider



 CMB ad WIMP detectors transitioned to ASIC readout due to high channel count



Will they ever?

LBNE (now DUNE) needs cryogenic ASICs



More than predicted, but later. Did not anticipate LArPix

- Now Under development:
 - Fast timing ASICs
 - Higher speed readout
 - SOC
 - Below 65nm CMOS
 - On-chip data reduction
 - Cryogenic CMOS (but not deep cryo)
 - Starting to use 3D integrated chips

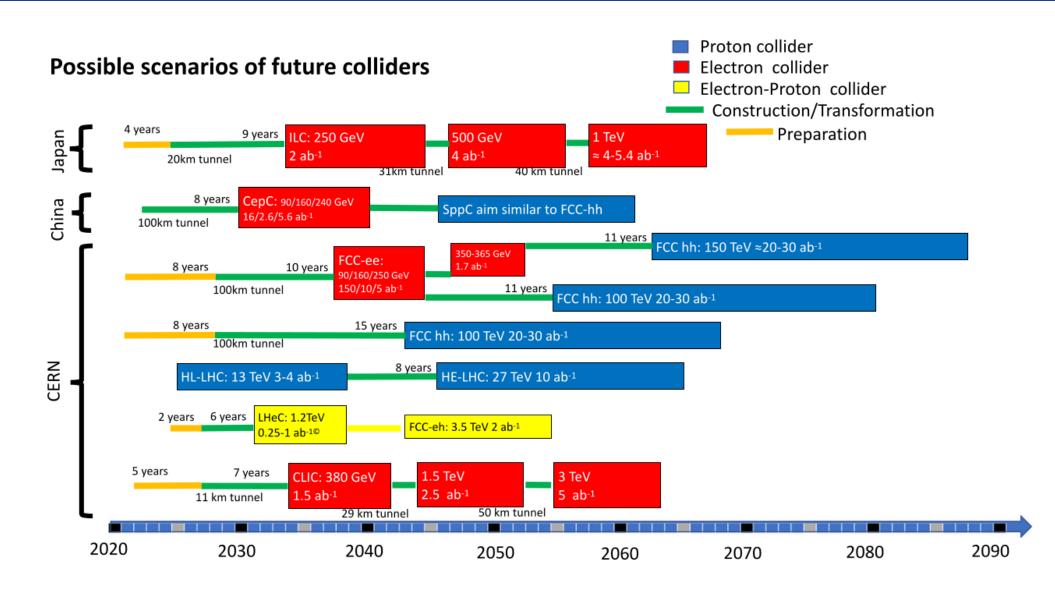


Take-away

- We're not bad at predicting incremental technology trends
- We're too optimistic with time-lines (submission impossible...)
- This makes my job easier- new things are further than we think, so 10 more years will not make a big difference (just prolong those predictions from 2013) 20 year maybe.
- But we can't really predict new things, even if they are only new to us but not really new to the World
- AI/MI
- Neuromorphic
- QIS
- Pandemics

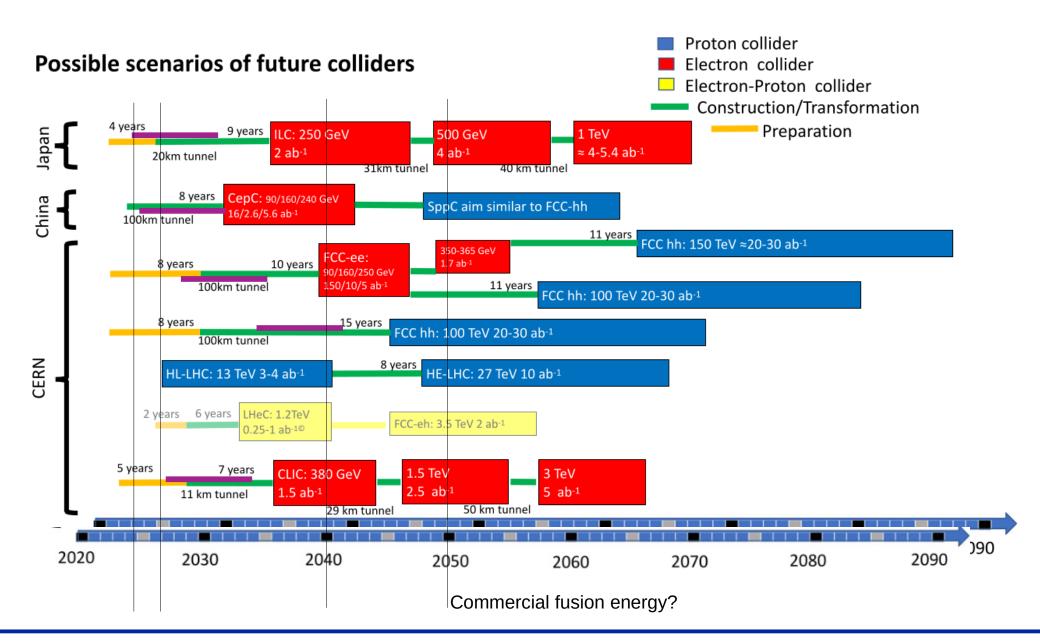
Not predicted in 2013 HEPIC + Snowmass

HEP Collider Timeline (collider detectors are biggest ASIC customer by far)



U. Bassler, CERN Council Meeting, 2019

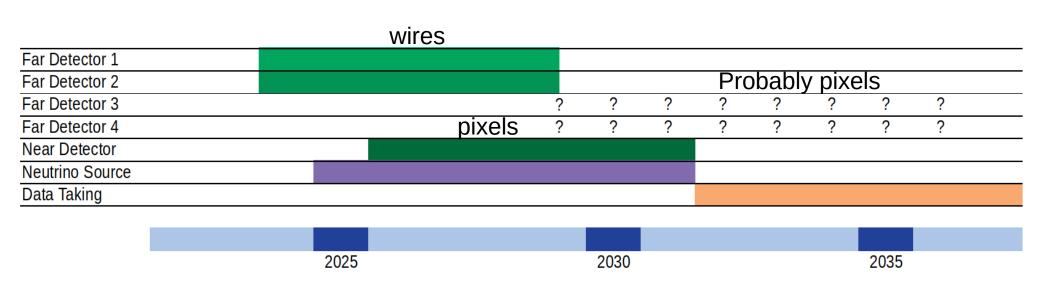
Chip development and adjusted time scale



Collider Timeline priorities & Notes

- The European Strategy process concluded that an e + e Higgs factory is the highest priority next collider
 - Will Snowmass conclude the same?
- Note: EIC is NOT in this table because it's for nuclear science, not HEP. But EIC is the next collider experiment on the horizon and will be a large consumer of ASICs.
 - (do we have a talk on EIC?)
- HL-LHC will go for a long time and HL-LHC detector upgrades will be limited.
- Main targets for new ASICs are:
 - inner pixel layer replacements
 - optical readout elements (we went through many readout tweaks and replacements in LHC)

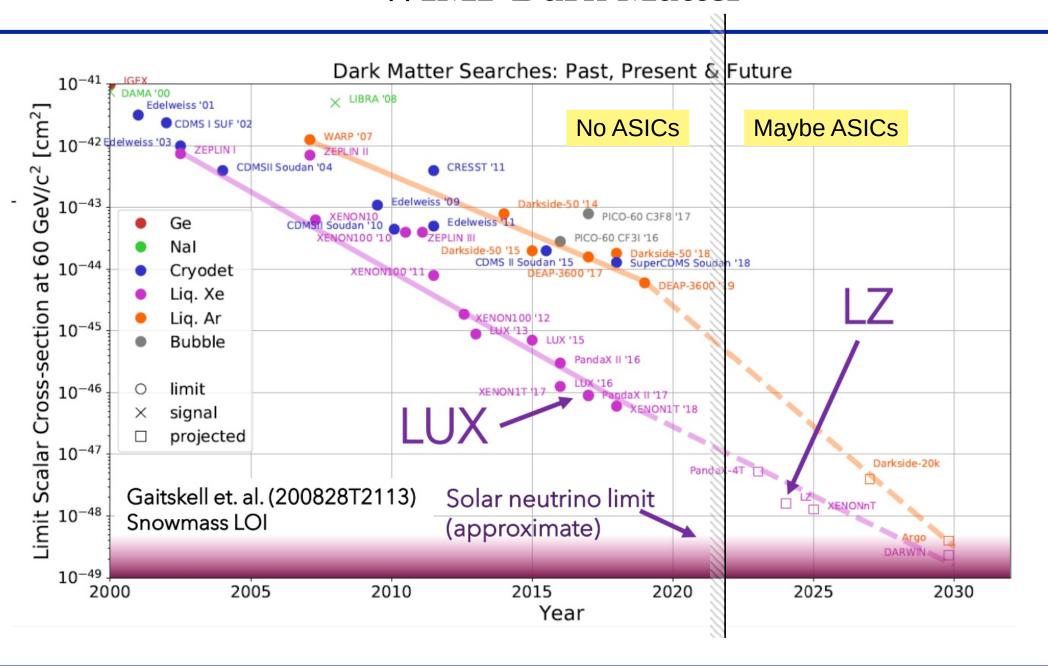
Neutrinos – DUNE



Neutrinos – 0vDBD

- nEXO experiment is using ASICs (see BNL talk)
- Other experiments may require ASICs
- Experiments currently under construction will reach important sensitivity thresholds (0vDBD search will not go on forever).
- Long term (20yr) 0vDBD ASIC prospects limited.

WIMP Dark Matter



WIMP Dark Matter and Neutrinos

- Large tanks of noble liquids want cheap granular readout
- Two main growth areas for ASICs:
 - Cryogenic chips
 - Large area pixels (charge sensitive, light sensitive, phonon sensitive, you name it)
- Because there are many experiments and they have upgrades paths, there
 will be a steady stream of required ASICs over the next 20 years.
- Need will continue to grow as cost of granular readout keeps coming down.

Cosmology & Low Mass DM

- ASICs for telescope CCD readout were significant work in the past
 - Now skipper CCD application in low mass DM and QIS need readout ASIC design (Farah's talk)
 - Future ASICs for telescopes?
- CMB detectors have not needed ASICs so far
 - CryoCMOS replacement for SQUIDs would be the killer app, but not in the plan for CMB S4.
 - CryoCMOS also could be interesting for low mass DM future experiments (eg SNSPD readout).
 - Will surely increase due to QIS.

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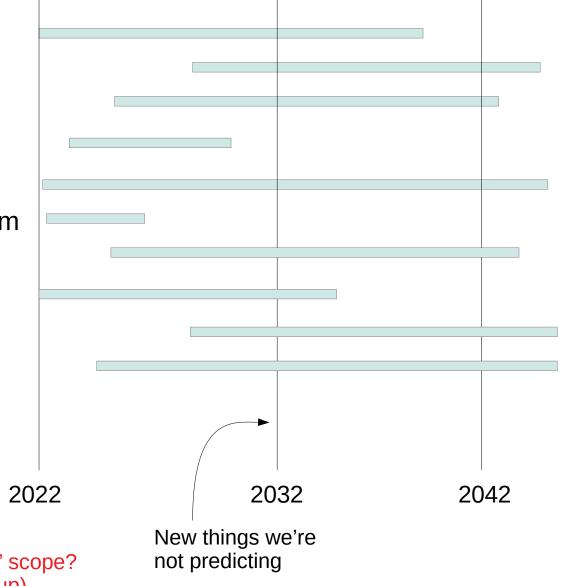
Snowmass white papers

- Another good source of trend analysis and speculation
- But in progress now, so don't have overview and conclusions
- We're supposed to write one of the white papers based on this workshop...

Evolutionary HEPASIC work next 20 years (we're good at predicting that)



- <28nm CMOS
- SOC with photonics*, SiPMs, etc.
- Photonic* driver ASICs
- On chip AI/ML and neuromorphic
- 130nm Open source kit and platform
- 65nm and below open source
- QIS related and deep cryo-CMOS
- ASIC SQUID replacement
- Wireless



^{*} Should silicon photonics be part of ASIC groups' scope? Did not see in morning overviews (1 slide in backup)

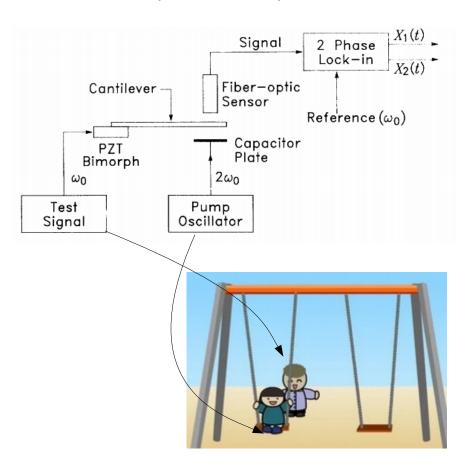
Poor Track Record to Guess New Things

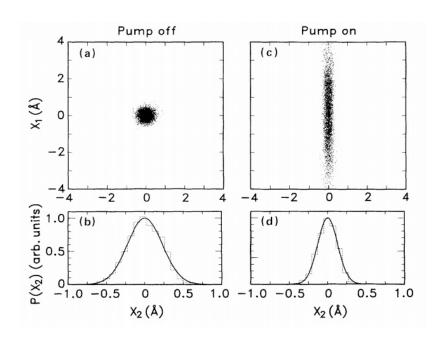
- Still Can't resist some speculation...
 - Just a couple of thoughts
 - 1) Borrow techniques for QIS in ASICs: noise squeezing
 - 2) Borrow superconductor detector techniques: phonon amplification

- (AI/ML, Nuromorphic, Open Source, not new any more)
- (BML I don't see becoming something we can use in the 20 year horizon)

Squeezing is Jst Good Old Parametric Amplification

- An old technology enjoying a revival in quantum computing/sensing under the name "squeezing" (K. K. Kharkevich, "Nonlinear and Parametric Phenomena in Radio Engineering", K. Pullen, Ed. New York: Rider, 1962.)
- A short, easy to follow paper illustrating the basic principle:
 "Mechanical parametric amplification and thermomechanical noise squeezing" Phys. Rev. Lett. 67 (1991)

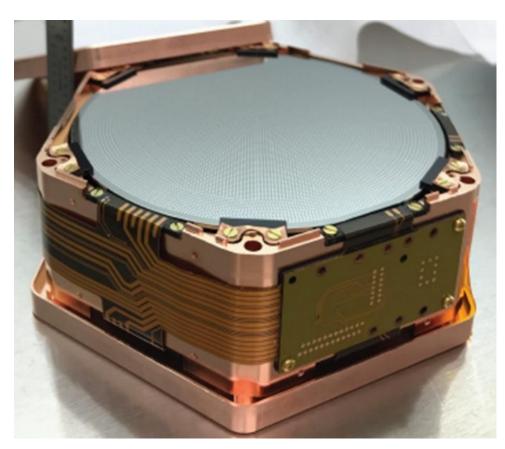




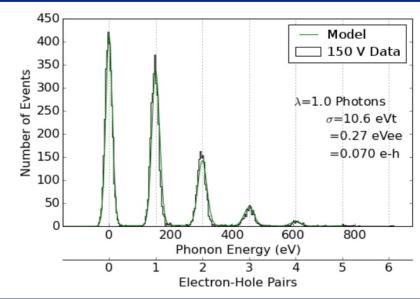
What about moving away from ionization?

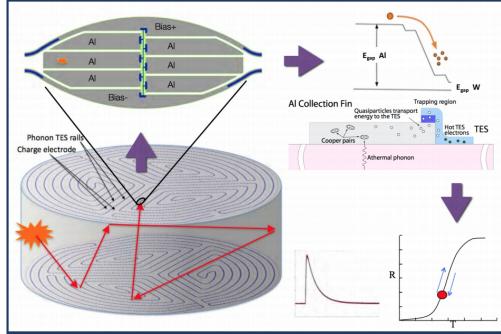
- Charged particles in B-field and material do more than ionize:
 - Synchrotron radiation
 - EM very fast impulse (but very weak). High BW SQUIDs?
 - Phonons in crystals
 - Transition radiation

Phonons instead of chargebut it has to be cold



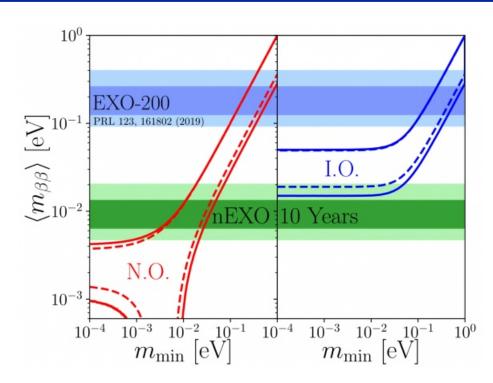
SuperCDMS Silcon HV detector With Athermal phonon Transition Edge Sensor reaadout

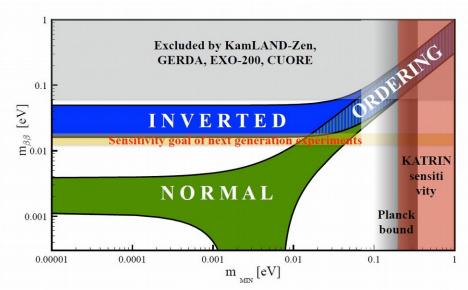


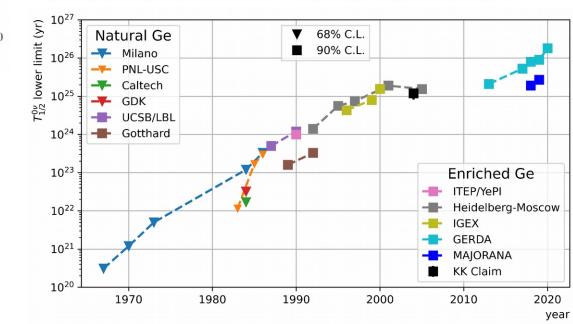


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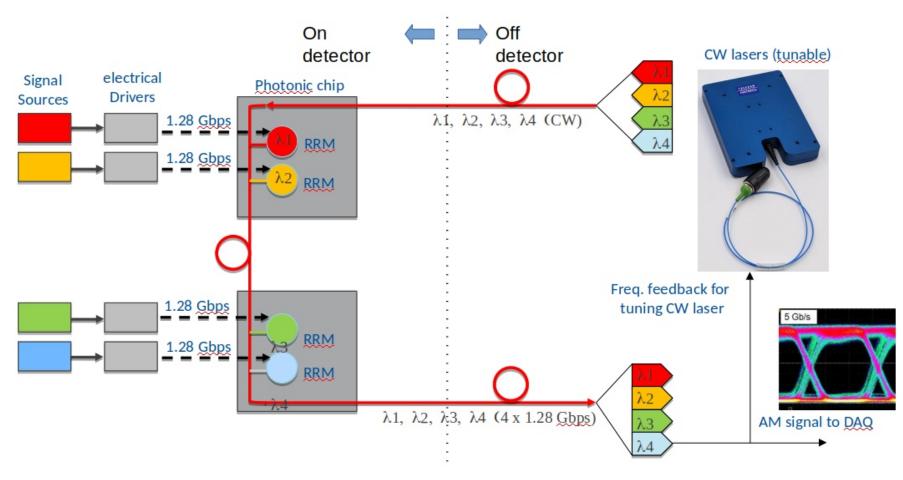
OvDBD Projections







WDM readout with silicon photonics











Phase 2 SBIR in progress. Will have devices to irradiate later this year