“DOE microelectronics: Tools and IP access program”

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Microelectronics (ASIC) Design for DOE

Requires 3 main building blocks

- **CAD-EDA Design Tools**
- Basic Design IP (Building block for ASIC design)
- Access to fabrication facilities (semiconductor foundries)

Main requirements and challenges

- Access to low cost – high volume research licenses: currently CAD companies categorize licenses as educational (~ almost free) or professional licenses ($$$)
  - CREATE a MIDDLE GROUND: Research licenses?

- Enable collaborative research across DOE Labs and university/ international partners while preserving the possibility of commercial private partnership

- A collective strategy for negotiation of terms and conditions (instead of each lab individually negotiating which often takes several months of effort)

- Labs have different requirements – hence a one size fits all model is not sustainable

Why do we need a strategy?

- Cost of CAD-EDA tools is a major bottleneck in growth of ASIC groups across the DOE labs
- Current terms are an impediment to setting up collaborative efforts with universities and other labs
- Collective bargaining provides economies of scale
- Impediment to US Competitiveness (EU has solved this problem decades ago by creating Europractice)

ASIC Design for DOE – 3 key elements

Electronic Design Automation – Computer Aided Design (CAD-EDA) Tools

- 3 major CAD tool vendors + other subsidiary vendors
- Cost of licenses is high (these are already discounted prices (60 – 90%
- Obstacles with growing design teams
- EU – has successfully setup "Europractice" for research licenses at education prices (<<< prices available in the US)
- Consolidated effort required to negotiate low cost – high volume licenses

Design IP

- Fundamental IP for IC design
- Basic IP provided by foundry or 3rd party.
- Free basic IP – essential for design
- Paid IP also available (e.g. building blocks such as ADC, high speed drivers and receivers etc.)
- Requires changes to legal framework as a workaround to indemnification clauses
- Multi- party NDA for collaboration

Foundry – Fabrication

- MPW vendors (IMEC, IMEC-USA, MUSE, *MOSIS* etc.)
- Large foundries – e.g. GF, TSMC, Tower Jazz
- Several smaller foundries (Skywater, IHP)
- CERN negotiated lower-price, smaller sizes, easier access for TSMC (previously similar agreement with IBM)
- Multi-party NDAs for collaboration across labs and universities
- Smaller die size to enable easier R&D

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DARPA Tool box

- https://www.darpa.mil/work-with-us/darpa-toolbox-initiative
- 2 tier agreement
  - 1st level of light-weight agreement with several EDA/IP vendors + Negotiated lower cost licenses (DARPA shared this with us)
  - Each Prime contractor then individually mix and match different EDA/IP vendor packages
  - All subcontractors of the prime contractor are automatically covered by the agreement
- Current NASA is setting up something similar
- Long term plan for a 3rd party to takeover to provide the service

- **Flexible & Expandable**

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- Why a slightly different model required?
  - Unlike DARPA program DOE requires production volumes
  - Higher volume licenses are required to support lab teams (DARPA team – public/private partnerships)
  - Easiest if legal issues are sorted out at the DOE level (makes it equally applicable to all DOE labs)
- Feedback from vendors
  - Like to consolidate contract Terms and Conditions (see this as a major time-consuming activity)
  - Need a sustainable model **(DARPA – chances of commercialization is much higher than DOE path to commercialization: Value proposition for vendors)**
  - Would prefer higher volume discounts

Business Model - Requirements

- Include all aspects of the design chain - CAD Licenses, Design flows and Design IP, Support and Training
- Conducive to collaboration between National labs & Universities pursuing federally funded research projects. Ability to engage in global partnerships for international scientific research.
- Model-based on research licenses to develop basic science experiments. But also enable technology transfer, work with commercial entities from startups to large established businesses with an additional fee to the vendor or low-cost professional licenses.
- An ecosystem that allows all CAD vendors and open-source tool developers to participate, with an overlook to a broader engagement beyond just chip design to enable system engineering.

Current set of vendors (Preliminary discussions)

ORDER of importance

- Cadence – All IC design + Photonics + PCB design tools
- Siemens – All IC design + PCB design tools + other EE/ME tools
- Synopsys – All IC design + Photonics + Detector development tools
- Ansys – Simulation + EE/ME tools
- Silvaco – All detector development tools
- Keysight – All RF design tools

ICPT Engagement

Consists of member from each of the 17 national labs

Currently started vendor discussions with:

- Cadence, Siemens and Ansys
- Looking to start discussion with other vendors (waiting for other ICPT reps to volunteer)

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ICPT process

- Data call from National labs: All national labs have provided information to ICPT reps directly regarding past 3-5 year spend on tools along with a wish list
- Data call for CAD tool vendors
- DOE approval for sole source justification
- Call for pricing proposal and negotiate uniform terms and conditions across the DOE complex for each of the CAD tool vendors and all their offerings
  - Vendors have requested a growth forecast for next 10 years – we have provided this in the form of the various BRN study reports across DOE for various initiatives requiring microelectronics

- Any national lab can then utilize the pre-negotiated pricing to customize their own license portfolio [They also have an option not to utilize the ICPT negotiated packages]

Summary

- ASIC development is critical to a wide number of DOE projects and mission space
- The cost of ASIC design licenses has steadily risen over years (US based labs don't have the equivalent of Europractise)
- The type of licenses required for our new projects has also contributed to the increase of costs. (e.g. Smaller geometry nodes, integrated photonics)
- Lack of CAD tools for basic research create a high barrier of entry for new labs to start microelectronics teams (one of the reasons)
- All of DOE coordinated approach will create a win-win situation for both lab teams as well as CAD-EDA vendors
  - Lower cost uniform rates
  - Pre-negotiated terms and conditions

Backup