GRAIN: optical readout with Hadamard masks

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OUTLINE

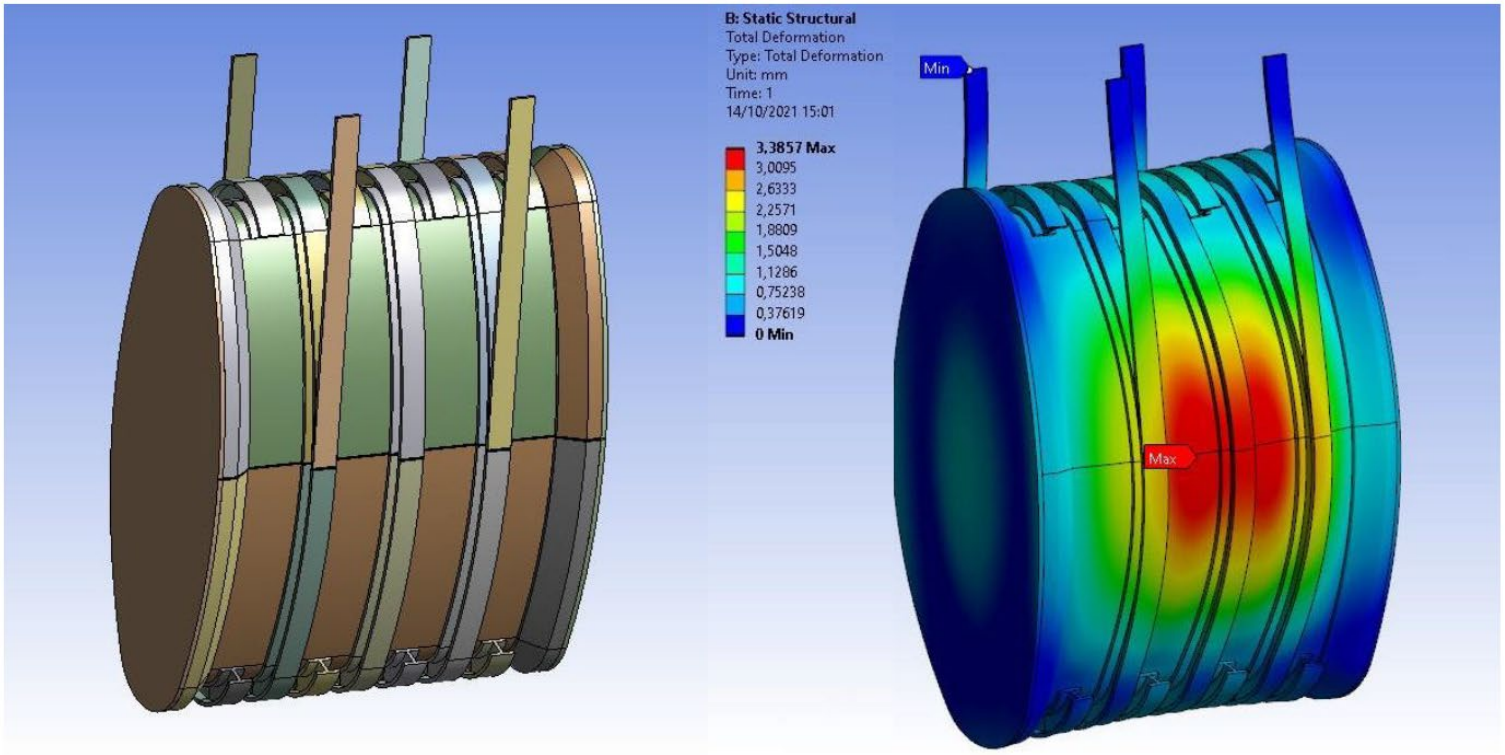
Not major updates since last presentation on 30 Nov 2021

- **Mechanics** detailed simulation in progress
- **Optics** for VUV scintillation light:
  - coded aperture (Hadamard masks)
  - 3D voxels recontruction
- Cryogenic **readout electronics**

GRAIN structural analysis

Detailed studies being carried out by a certification engineering company to be fully compliant with US rules: **first preliminary results under evaluation.**

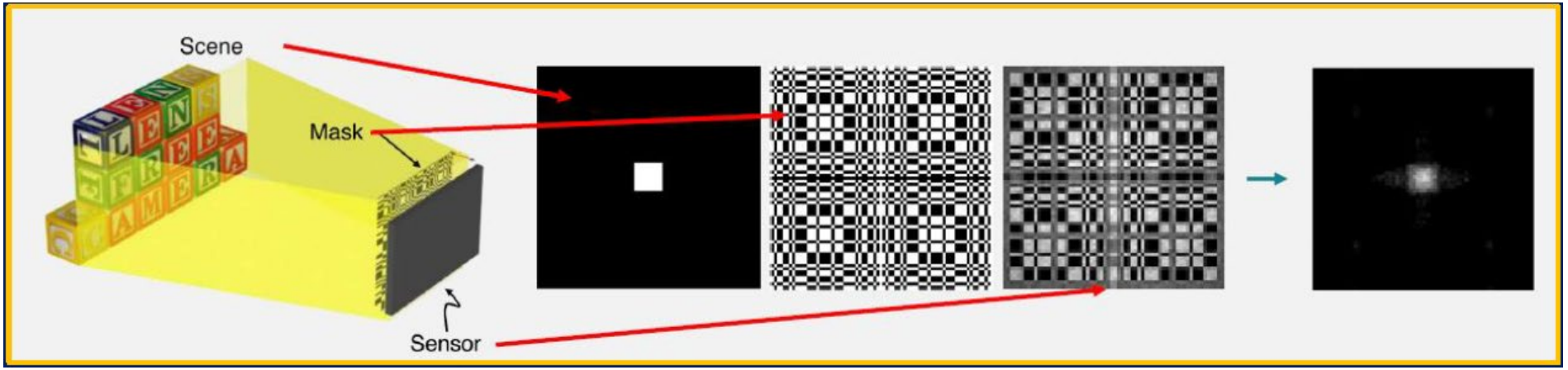
Press = 3 bars



Coded aperture optics

Principle of coded aperture technique: many pinholes arranged so that the resulting light pattern can be reconstructed to the original image.

It is a non focusing device, which trasmits 50% of the light



Coded aperture: simulation

- A full simulation chain has been setup: from **physics events** to GEANT4 **simulation of particles in LAr**, **light emission** and **propagation**, **model of SiPM matrix response**, **front-end electronics**
- A lot of work done to build a versatile simulation suite able to reproduce **different geometries** and **sensor+masks** configurations simply by changing some parameters
- Run on a **HPC facility** based on GPUs (courtesy D.Cesini-CNAF)
- Image reconstruction in very advanced status with two appraches under study:
  - 2D reconstruction based on mathematical algorythms (3D obtained by combining 2D projections). Masks geometries follow well defined rules.
  - 3D combinatorial approach: volume divided in voxels and light sources propagate to the sensor and filter by holes in mask.

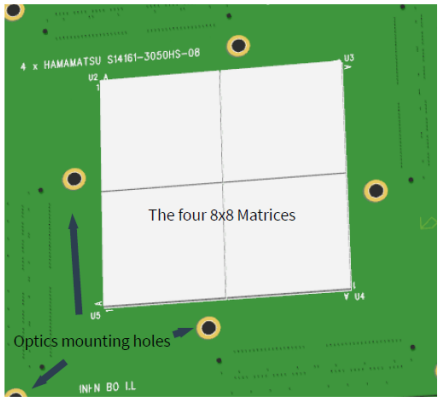
Roadmap

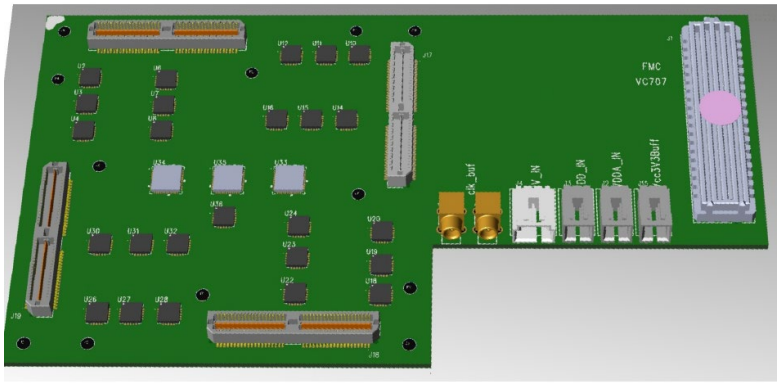
- Build a hardware prototype ("Cold Demonstrator") to validate the technique and using presently available sensors and electronics:
  - Liquid Nitrogen (Argon) working condition
  - Low power consumption and minimal number of cables
  - Cold electronics based on dedicated ASIC ("Alcor" from INFN-Torino, cryogenic, 32 ch)
  - Commercial matrices of SiPMs (16x16 rank, 3x3 mm^2 SiPM, 256 ch)
- Test demonstrator in Liquid Argon (cryostat in Genova)
- Validate simulation with Cold demonstrator

- Fully simulate GRAIN optical readout with N cameras with 32x32 matrices): test different configurations to find best compromise (cost, power, performance) for track reconstruction

Cold demonstrator hardware

- Mezzanine board with sensor mounted on a motherboard with 8 ASIC for a total of 256 channels

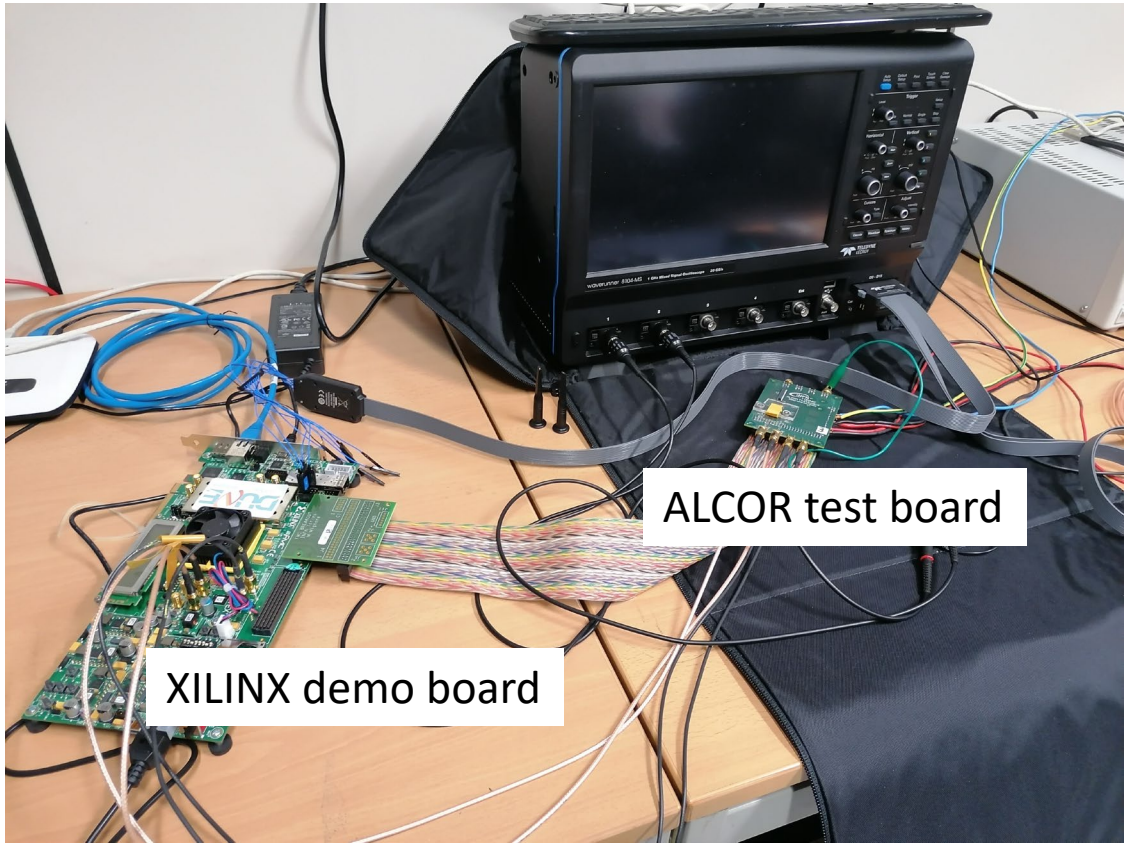




- Project submitted to external firm for layout of motherboard, pcb production and component mounting. Three complete cameras with available ASICs. Deliver expected end of January 2022.
- Readout with commercial Xilinx demo board

Preliminary test with ALCOR

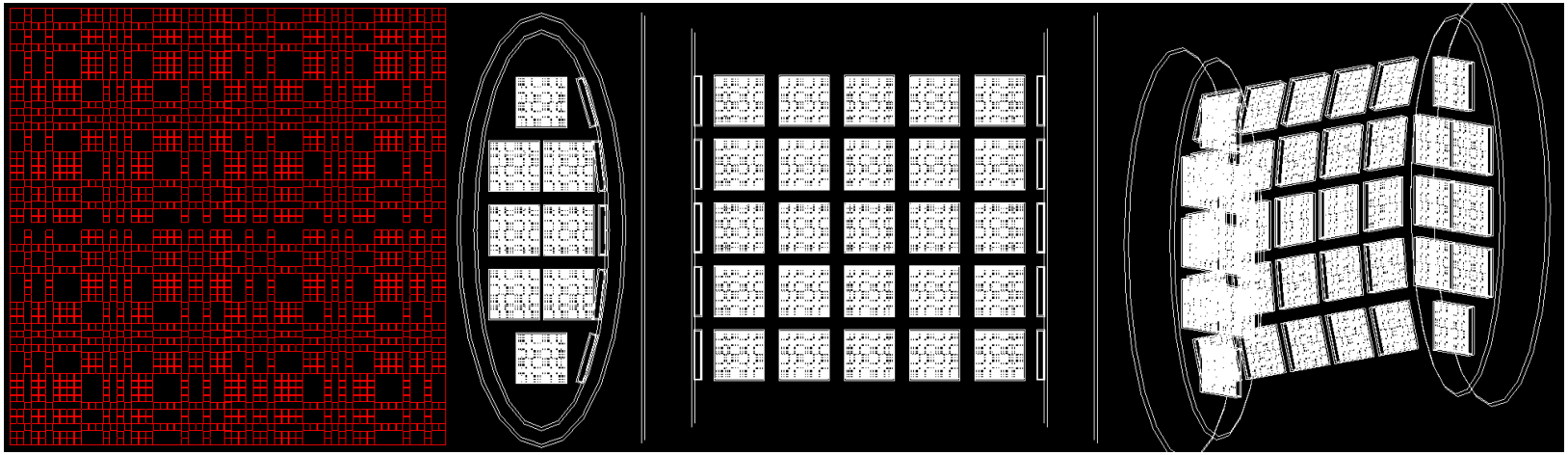
- Firmware for control and DAQ for AISC is under development



Simulation of advanced cameras

8 cameras on each lateral face
25 cameras on each curved face
32x32 sensor matrix with 3.2x3.2 mm^2 SiPMs (102.4 x 102.4 mm^2)
61x61 mask with 2.71x2.71 mm^2 holes (177.6 x 177.6 mm^2, including an extra border)

Cameras on one curved faces are omitted in the pictures.
Image reconstruction can be tested also with a reduced set of cameras.

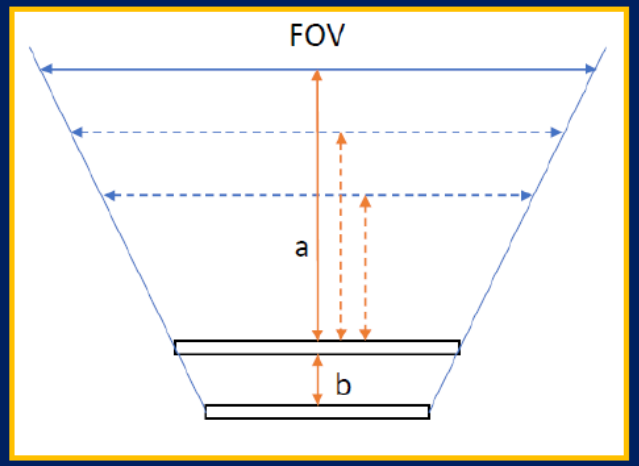


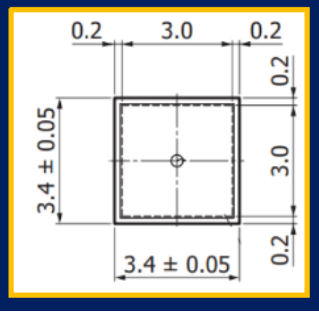
BACKUP SLIDES

Coded aperture :16x16 demonstrator

A simulation of the hardware of a first prototype camera (see later) was setup.

- Matrix SiPM Rank: 16
- Mask Rank: 17
- Mask Pitch: 3.15 mm
- Sensor Pitch: 3.4 mm
  - active area 3.0 mm
- Mask to Sensor Distance: b = 2.0 cm
- Focal Plane: a = 25 cm
- SiPM Efficiency: hypothesized 25%

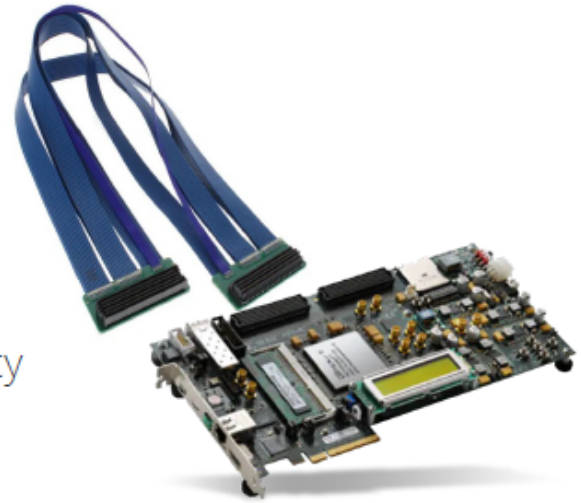




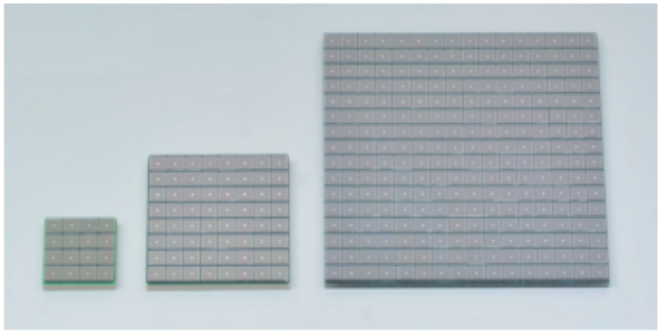
Back End FPGA

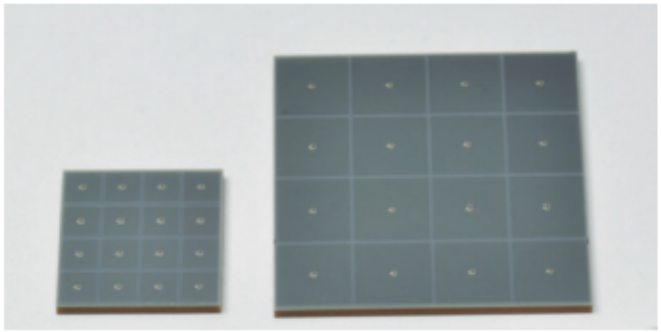
Commercial, choice dictated by ALCOR connectivity

- Each ASIC requires 12 LVDS pairs, of which 6 @ 320 MHz / 640 Mbps DDR
- Could go slower, but cannot decouple TDC clock from I/O clock
  - Some slow pairs can be buffered
  - Some testing was needed to select LVDS buffer working in cryo conditions
- Still around 70 pairs => Requires full HPC FMC
- Very few boards have this fully routed
- Selected Xilinx VC 707, somewhat old but quite powe
  - Use commercial Twinax FMC extension cable for better integrity



SiPM matrices from Hamamatsu





One 16x16 S13615-1050N-16

Cell pitch 50 um, pixel area 1 mm^2

Active area 256 mm^2, total area 368 mm^2

Four 8x8 S14161-3050HS-08

Cell pitch 50 um, pixel area 9 mm^2

Active area 2304 mm^2, total area 2641 mm^2

Other options exist in Hamamatsu catalogue, with pixel area up to 36 mm^2

Outlook: GRAIN scalability

Primary concern for GRAIN: this ASIC does not scale

It's the first of its kind, could not expect more!

The final ASIC needs

More channels per die AND more channels per I/O link

Lower power consumption per channel

Larger buffers to exploit beam duty cycle and relax peak link throughput

Decoupled TDC clock (as is or higher) from I/O clock (prefer lower)

Charge Integrator ADC in addition or instead of ToT (wishful thinking)

Simulation of advanced cameras

8 cameras on each lateral face
25 cameras on each curved face
32x32 sensor matrix with 6.2x6.2 mm^2 SiPMs (198.4 x 198.4 mm^2)
31x31 mask with 5.61x5.61 mm^2 holes (192 x 192 mm^2, including an extra border)

Cameras on one curved faces are omitted in the pictures.