Rad-Hardened Front-End for the Beam Loss Monitoring at CERN

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Summary

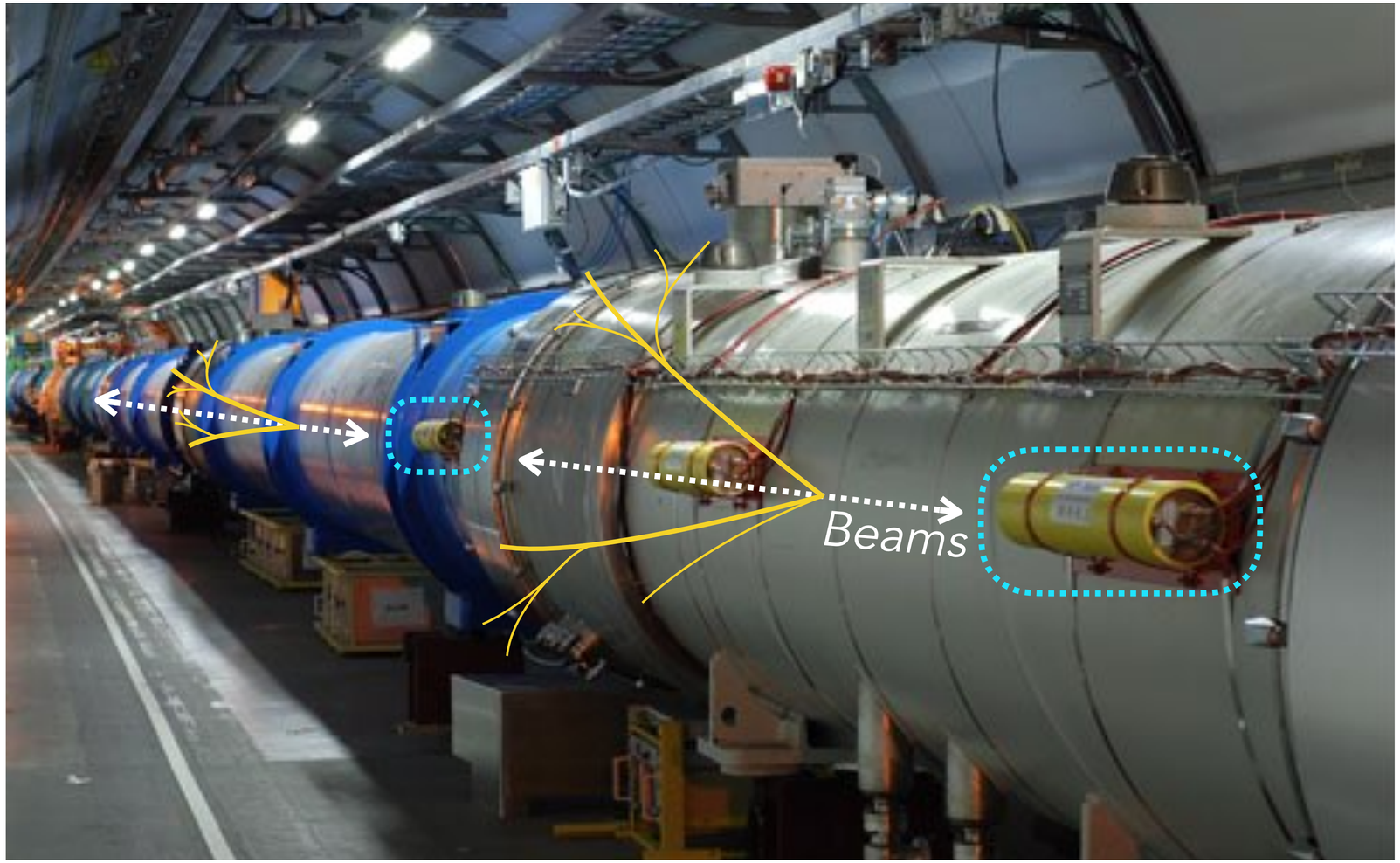
- *Beam Loss Monitoring (**BLM**) system overview*
- *SoA Electronics and upgrades in view of HL-LHC*
- *Specifications of the integrated converter and the Front-End*
- *Results of devices characterisation*
- *Brief production status and costs overview*
- *Timetable*

The Beam Loss Monitoring Aims

It measures the radiation produced by lost beam particles and their secondary cascades

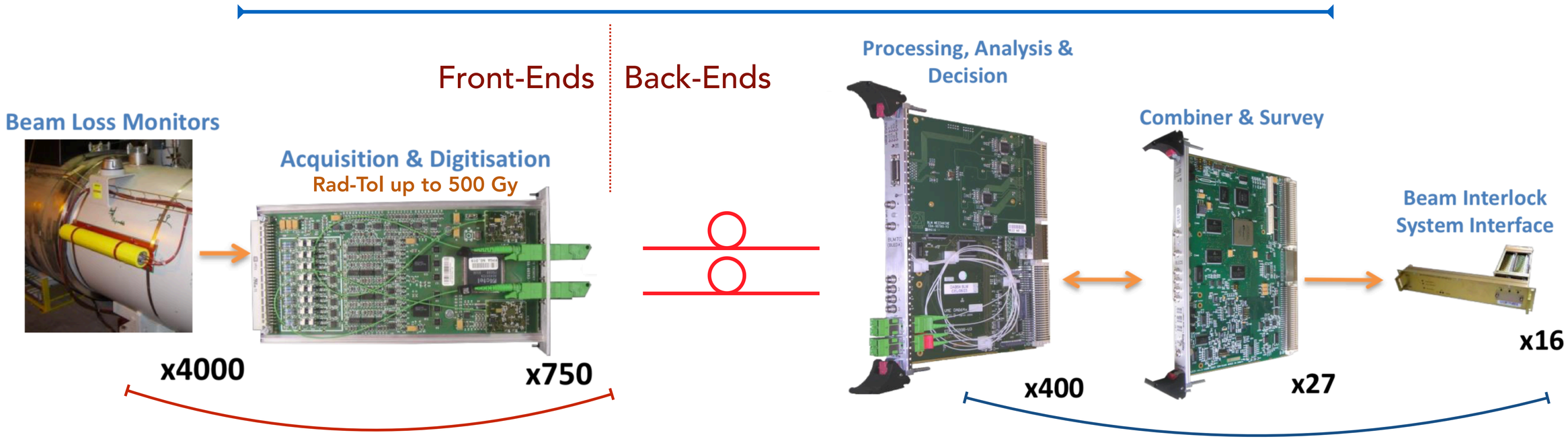
A Critical Protection System preventing damages and quench of the magnets

A flexible diagnostic tool for tracking the accelerator complex behaviour



BLM ion-Chamber detectors on LHC

BLM Electronics State of the Art



ion-Chamber Detectors produce a current proportional to the loss shower radiation

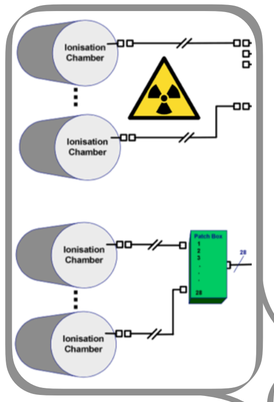
Front-End cards convert the analog currents into digital data stream

The data are processed and measurements are compared with thresholds

A beam interlock signal is eventually triggered

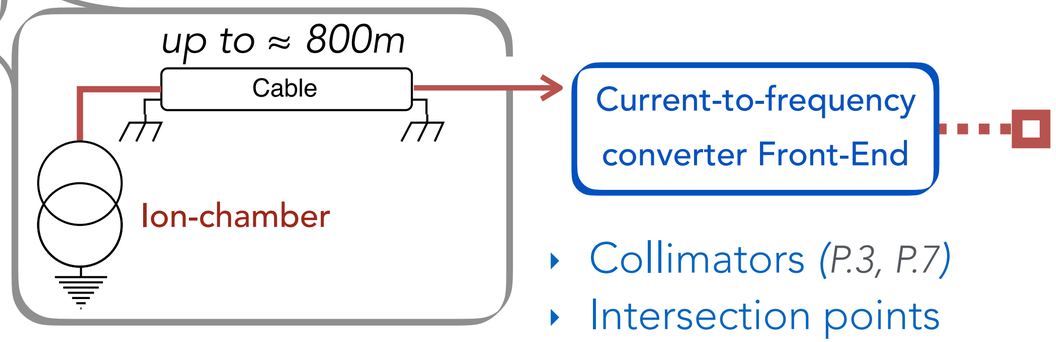
Issues in view of BLM / HL-LHC Upgrade

- *Higher beam loss radiation is expected throughout the accelerator.*
- *The conversion front-end shall be moved closer to the ion-chamber detectors.*
- *Even more effective machine protection will be allowed by a four time faster response of 10μs (i.e. newer ATLAS/CMS triplets).*
- *Long term maintainability would be ensured at limited costs.*



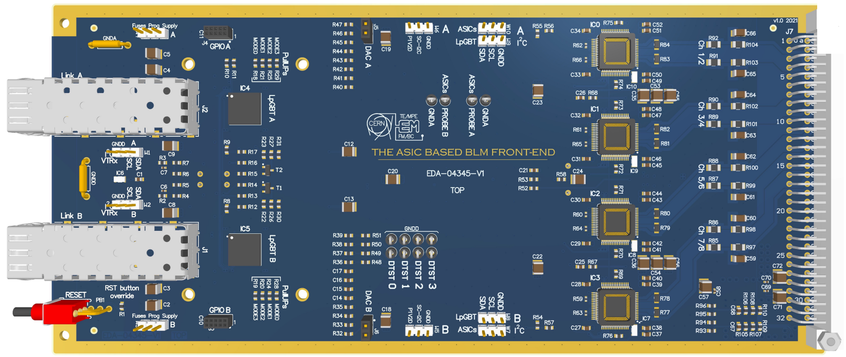
High Radiation Environment

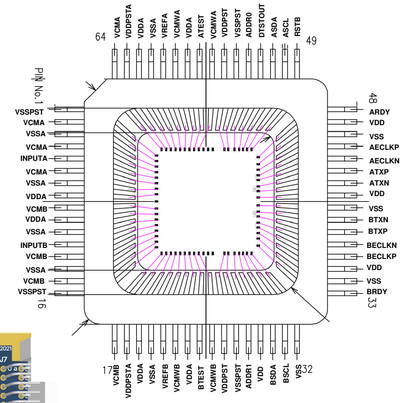
Analogue Transmission Bottleneck



- Collimators *(P.3, P.7)*
- Intersection points
- P1 and P5 Triplets

BLEIC card

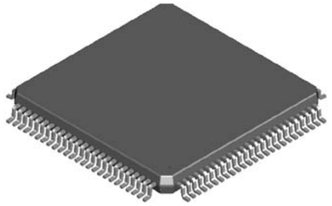




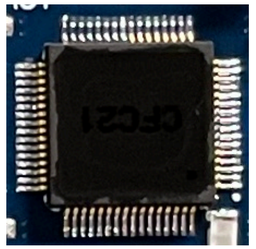
BLMASIC

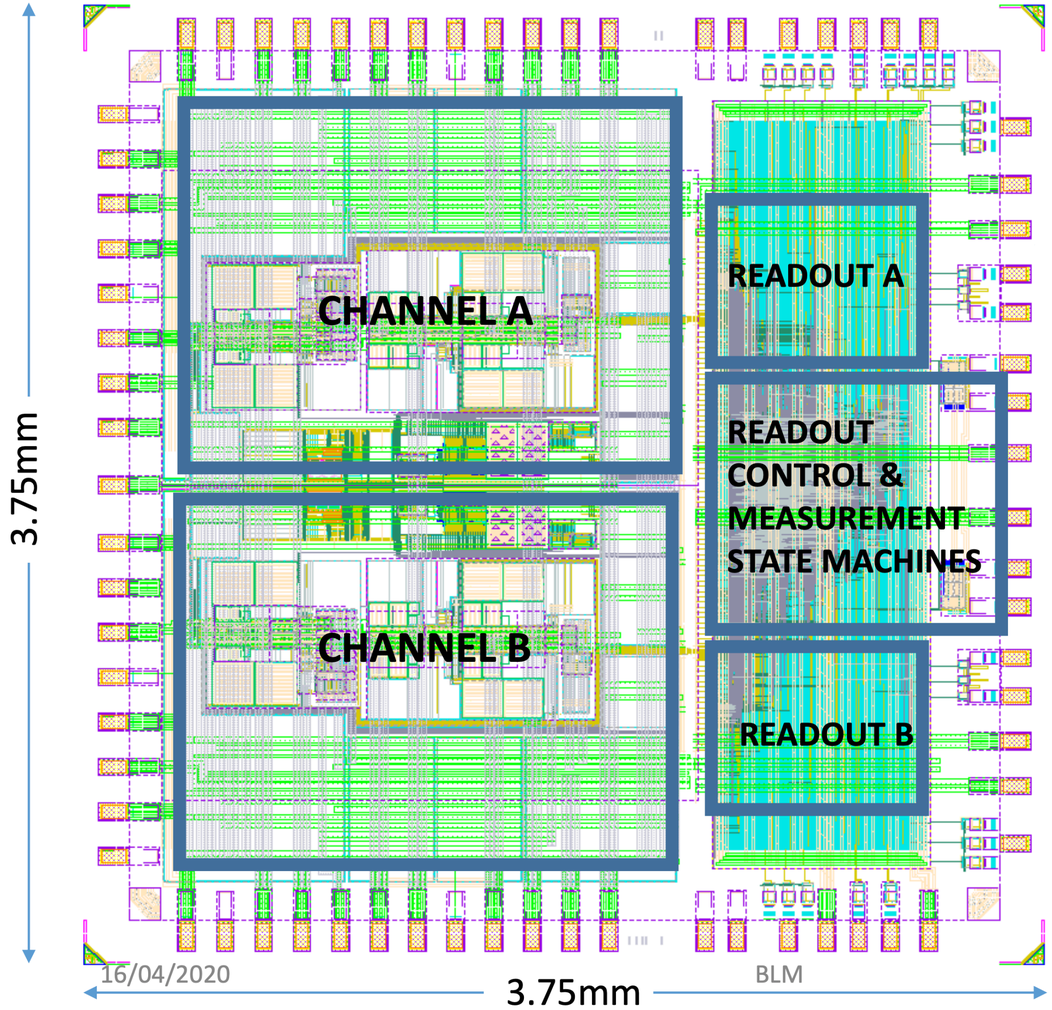
BLMASIC Key Specifications

- **Dual** measurement inputs
- Measurement time response **down to 10µs**
- Input measurements range: **1pA to ~ 1mA**
- Relative **Error < 10%** (Integration time dependent)
- Chamber and cable impedance compatible:
  ~ 350pF + 50m cable (**5nF tot**)
- **HL-LHC** environment **compatible** (temp./humid.)
- Tolerant to **SEU, EMI** and **ESD/Overload**
- **LpGBT e-links compatible**
- Radiation-Hard features: up to > **100 kGy (10Mrad)**
- TSMC CMOS **130nm** technology



Standard 64-pin Quad



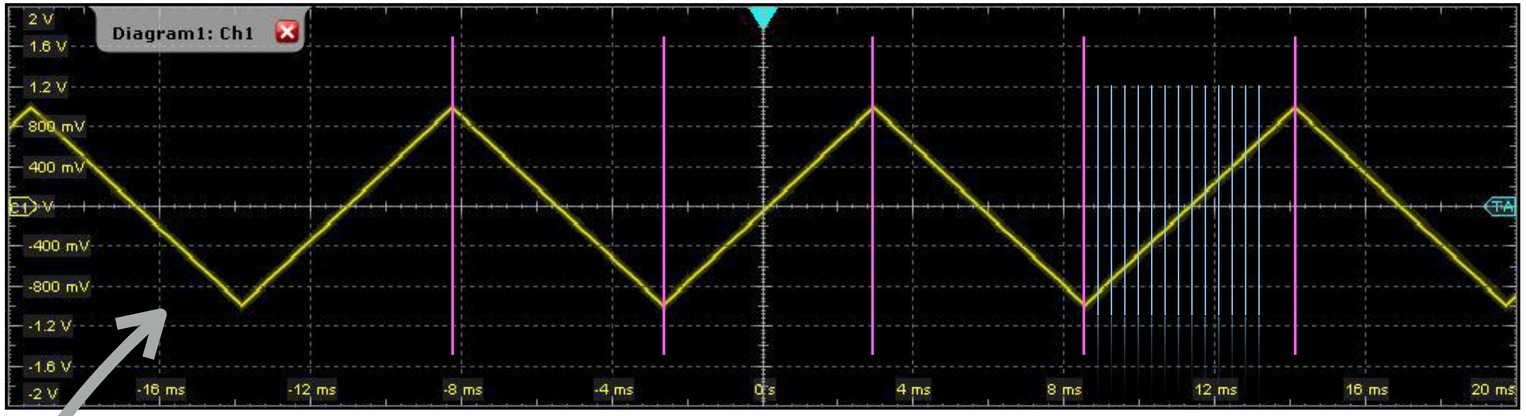


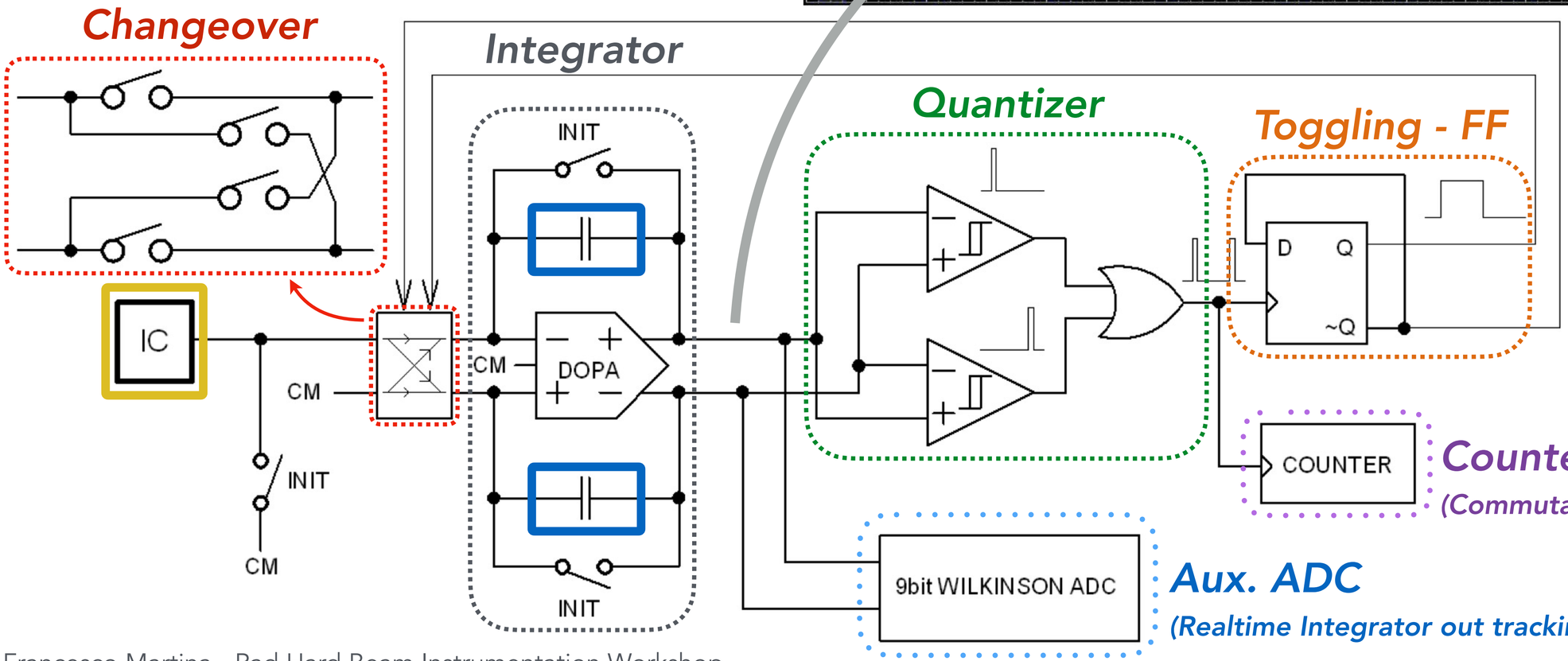
Designed by **EP-ESE-ME** and **SY-BI-BL** teams

BLMASIC Conversion Architecture

$$v_{(t)} = \frac{1}{C}\int_{-\infty}^{t} i_{(\tau)}\, d\tau$$

$$\frac{dv_{(t)}}{dt} = \frac{i_{(t)}}{C}$$





Counter
(Commutations in 10μs)

Aux. ADC
(Realtime Integrator out tracking in 10μs)

Steady State

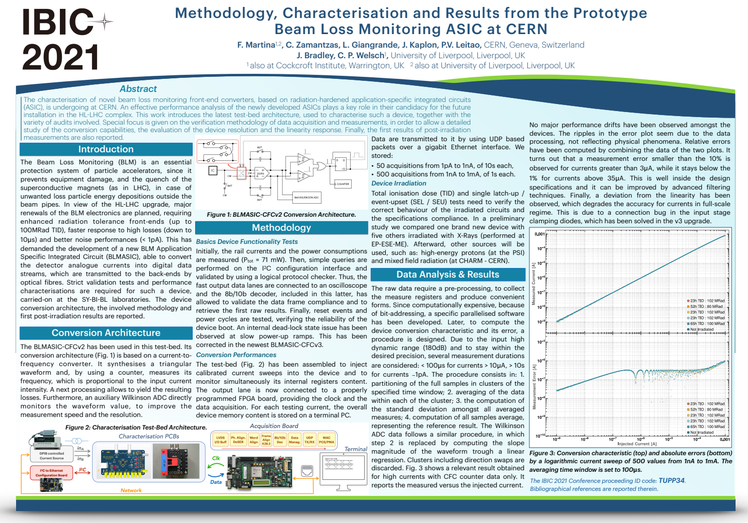
$$T_{rise} \approx T_{fall} \propto \frac{C\,V_{swing}}{\langle i \rangle}$$

$$Freq = \frac{1}{T_{rise} + T_{fall}}$$

$$Freq \propto \frac{\langle i \rangle}{C\,V_{swing}}$$

BLMASIC Test-Bed

- The tests carried out reported performance well inside the specification so far.
- The electronics noise is below 500fA.
- The characterisation methodology procedures have been consolidated
- X-Rays test at TID of 1MGy does not reported conversion behaviour drifts


IBIC 2021

Methodology, Characterisation and Results from the Prototype Beam Loss Monitoring ASIC at CERN

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Abstract

The characterisation of novel beam loss monitoring front-end converters, based on radiation-hardened application-specific integrated circuits (ASIC), is undergoing at CERN. An effective performance analysis of the newly developed ASICs plays a key role in their candidacy for the future installation in the HL-LHC complex. This work introduces the latest test-bed architecture, used to characterise such a device, together with the variety of audits involved. Special focus is given on the verification methodology of data acquisition and measurements, in order to allow a detailed study of the conversion capabilities, the evaluation of the device resolution and the linearity response. Finally, the first results of post-irradiation measurements are also reported.

Introduction

The Beam Loss Monitoring (BLM) is an essential protection system of particle accelerators, since it prevents equipment damage, and the quench of the superconductive magnets (as in LHC), in case of unwanted loss particle energy depositions outside the beam pipes. In view of the HL-LHC upgrade, major renewals of the BLM electronics are planned, requiring enhanced radiation tolerance front-ends (up to 100MRad TID), faster response to high losses (down to 10μs) and better noise performances (< 1pA). This has demanded the development of a new BLM Application Specific Integrated Circuit (BLMASIC), able to convert the detector analogue currents into digital data streams, which are transmitted to the back-ends by optical fibres. Strict validation tests and performance characterisations are required for such a device, carried-on at the SY-BI-BL laboratories. The device conversion architecture, the involved methodology and first post-irradiation results are reported.

Conversion Architecture

The BLMASIC-CFCv2 has been used in this test-bed. Its conversion architecture (Fig. 1) is based on a current-to-frequency converter. It synthesises a triangular waveform and, by using a counter, measures its frequency, which is proportional to the input current intensity. A next processing allows to yield the resulting losses. Furthermore, an auxiliary Wilkinson ADC directly monitors the waveform value, to improve the measurement speed and the resolution.

Figure 2: Characterisation Test-Bed Architecture.

Figure 1: BLMASIC-CFCv2 Conversion Architecture.

Methodology

Basics Device Functionality Tests

Initially, the rail currents and the power consumptions are measured (P_{tot} = 71 mW). Then, simple queries are performed on the I²C configuration interface and validated by using a logical protocol checker. Thus, the fast output data lanes are connected to an oscilloscope and the 8b/10b decoder, included in this latter, has allowed to validate the data frame compliance and to retrieve the first raw results. Finally, reset events and power cycles are tested, verifying the reliability of the device boot. An internal dead-lock state issue has been observed at slow power-up ramps. This has been corrected in the newest BLMASIC-CFCv3.

Conversion Performances

The test-bed (Fig. 2) has been assembled to inject calibrated current sweeps into the device and to monitor simultaneously its internal registers content. The output lane is now connected to a properly programmed FPGA board, providing the clock and the data acquisition. For each testing current, the overall device memory content is stored on a terminal PC.

Data are transmitted to it by using UDP based packets over a gigabit Ethernet interface. We stored:

- 50 acquisitions from 1pA to 1nA, of 10s each,
- 500 acquisitions from 1nA to 1mA, of 1s each.

Device Irradiation

Total Ionisation dose (TID) and single latch-up / event-upset (SEL / SEU) tests need to verify the correct behaviour of the irradiated circuits and the specifications compliance. In a preliminary study we compared one brand new device with five others irradiated with X-Rays (performed at EP-ESE-ME). Afterward, other sources will be used, such as: high-energy protons (at the PSI) and mixed field radiation (at CHARM - CERN).

Data Analysis & Results

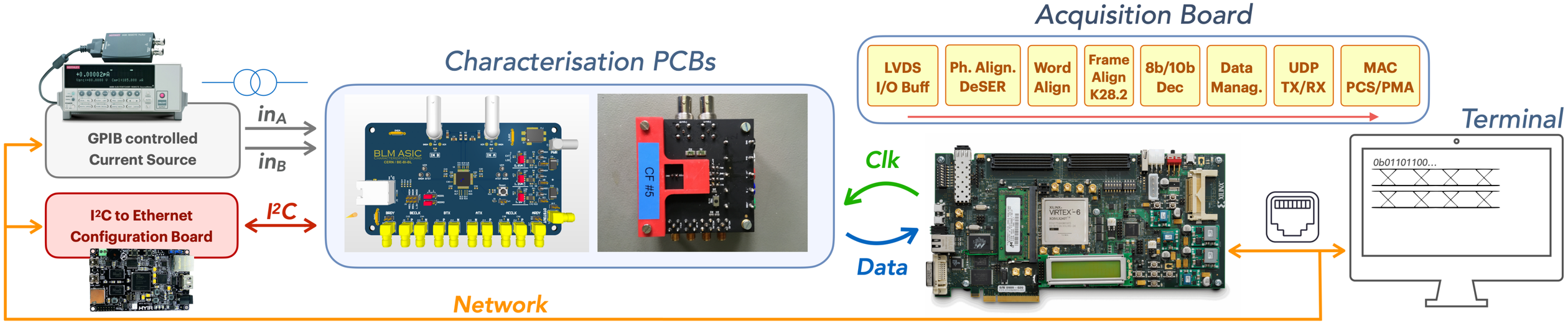
The raw data require a pre-processing, to collect the measure registers and produce convenient forms. Since computationally expensive, because of bit-addressing, a specific parallelised software has been developed. Later, to compute the device conversion characteristic and its error, a procedure is designed. Due to the input high dynamic range (180dB) and to stay within the desired precision, several measurement durations are considered: < 100μs for currents > 10μA, > 10s for currents < 1pA. The procedure consists in: 1. partitioning of the full samples in clusters of the specified time window; 2. averaging of the data within each of the cluster; 3. the computation of the standard deviation amongst all averaged measures; 4. computation of all samples average, representing the reference result. The Wilkinson ADC data follows a similar procedure, in which step 2 is replaced by computing the slope magnitude of the waveform trough a linear regression. Clusters including direction swaps are discarded. Fig. 3 shows a relevant result obtained for high currents with CFC counter data only. It reports the measured versus the injected current.

No major performance drifts have been observed amongst the devices. The ripples in the error plot seem due to the data processing, not reflecting physical phenomena. Relative errors have been computed by combining the data of the two plots. It turns out that a measurement error smaller than the 10% is observed for currents greater than 3μA, while it stays below the 1% for currents above 35μA. This is well inside the design specifications and it can be improved by advanced filtering techniques. Finally, a deviation from the linearity has been observed, which degrades the accuracy for currents in full-scale regime. This is due to a connection bug in the input stage clamping diodes, which has been solved in the v3 upgrade.

Figure 3: Conversion characteristic (top) and absolute errors (bottom) by a logarithmic current sweep of 500 values from 1nA to 1mA. The averaging time window is set to 100μs.

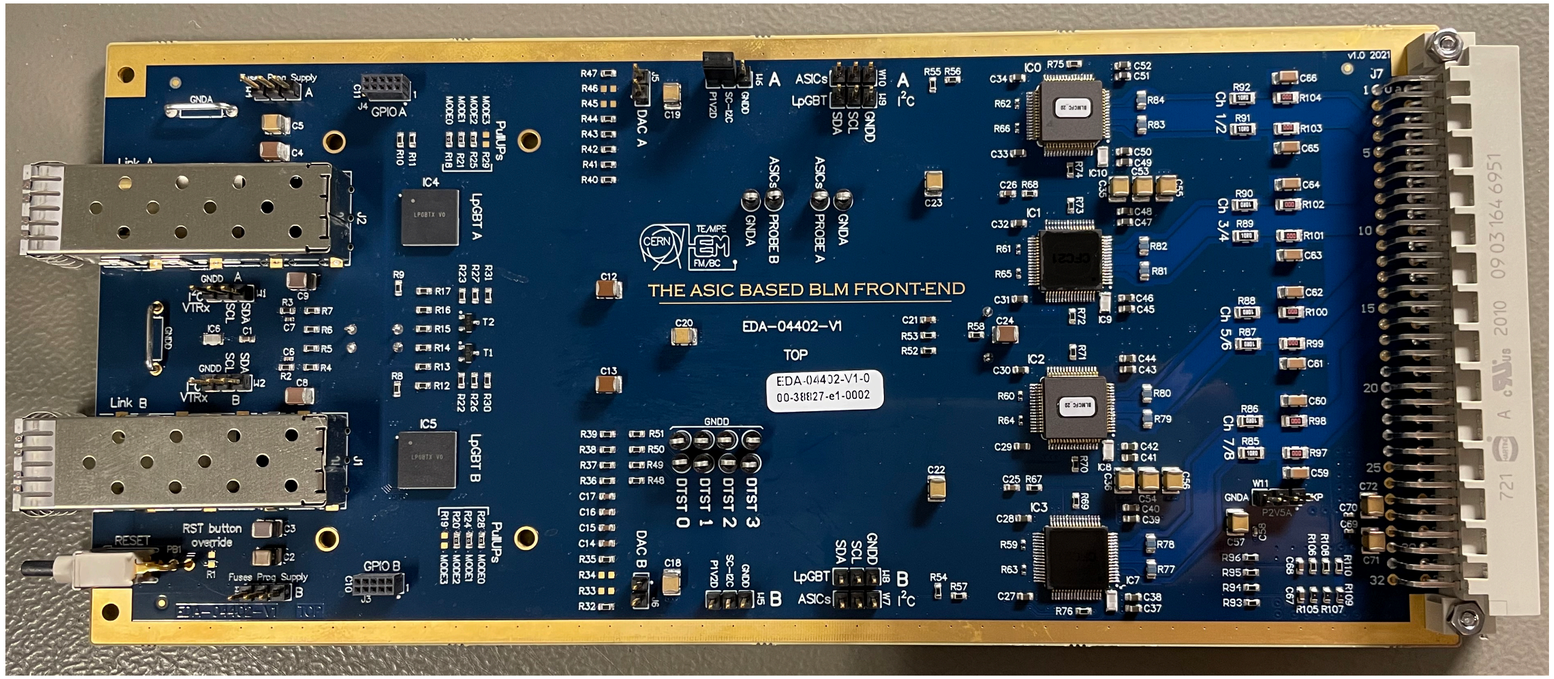
The IBIC 2021 Conference proceeding ID code: TUPP34. Bibliographical references are reported therein.

*F. Martina et Al, **"Methodology, Characterisation and Results From the Prototype Beam Loss Monitoring ASIC at CERN"**, 10th Int. Beam Instrumentation Conf. (IBIC'21), Pohang, South Korea, Sep. 2021, paper TUPP34.*

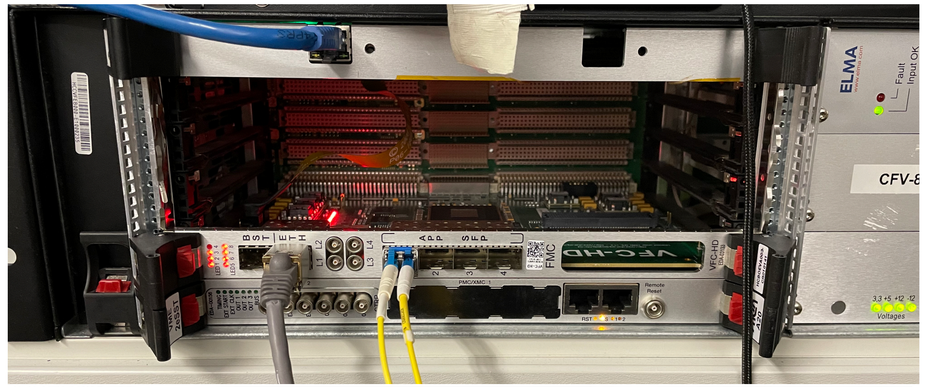


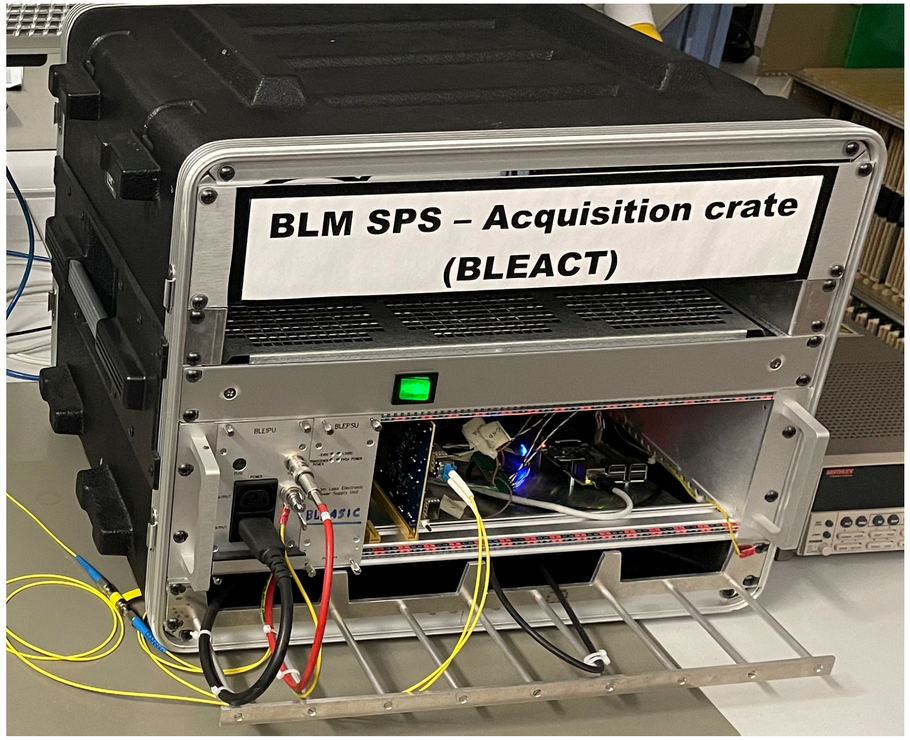
ASIC based BLM Front-End

- 4xBLMASICs → 8 ion-Chamber input channels
- Radiation tolerant up to > 10kGy (w/ optical transceivers)
- Redundant LpGBT for data transmission
- Wide range of diagnostic / debugging features
- Backward installation compatibility
- IPC Class 3 Dev/Production on Panasonic MEGTRON$_6$ PCB

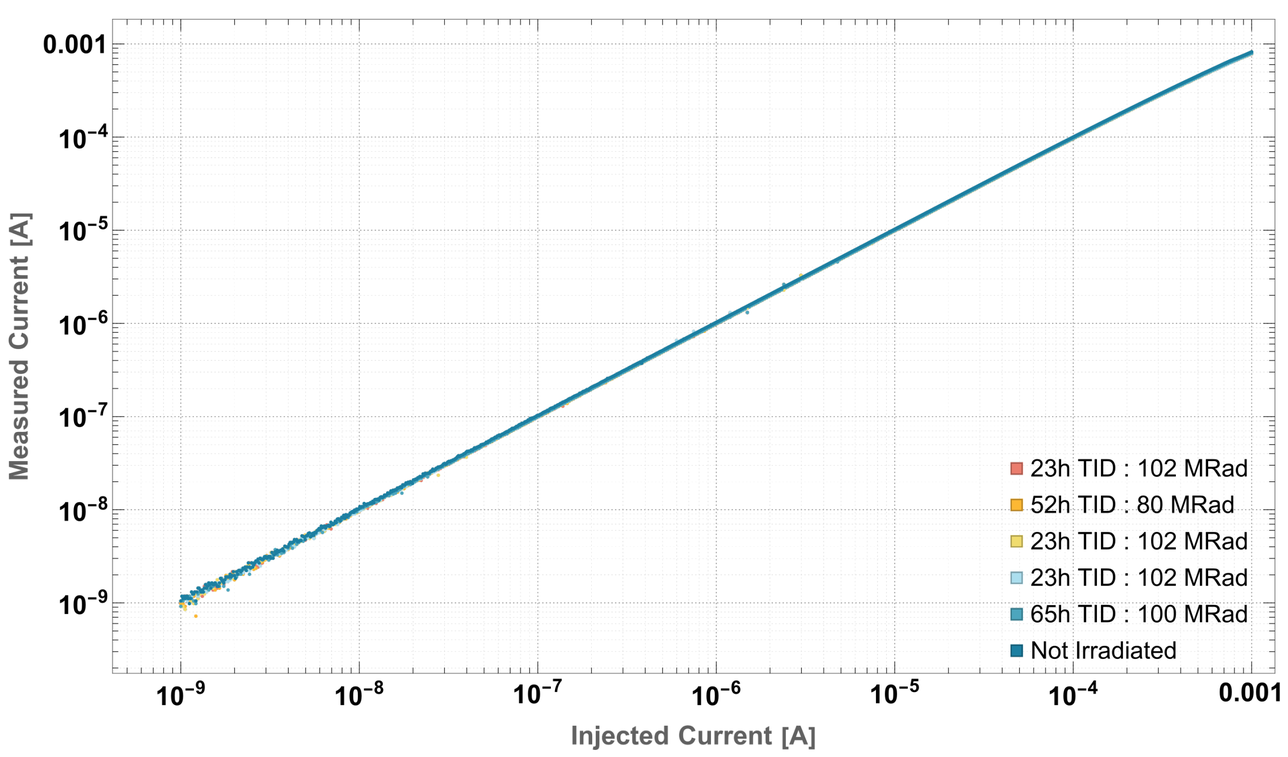


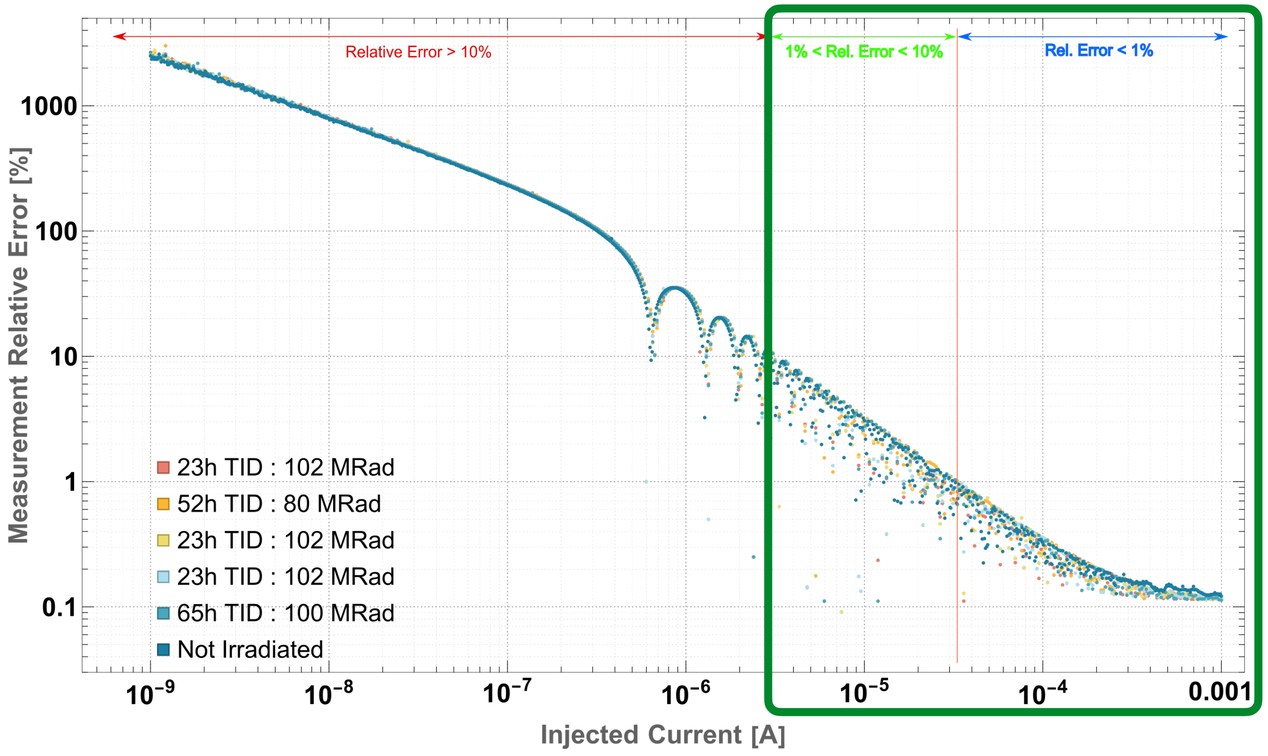
The installation prototype assembled within the new SPS Acquisition Crate and connected to the back-end





BLMASICv2 Post-Irradiation Results high currents





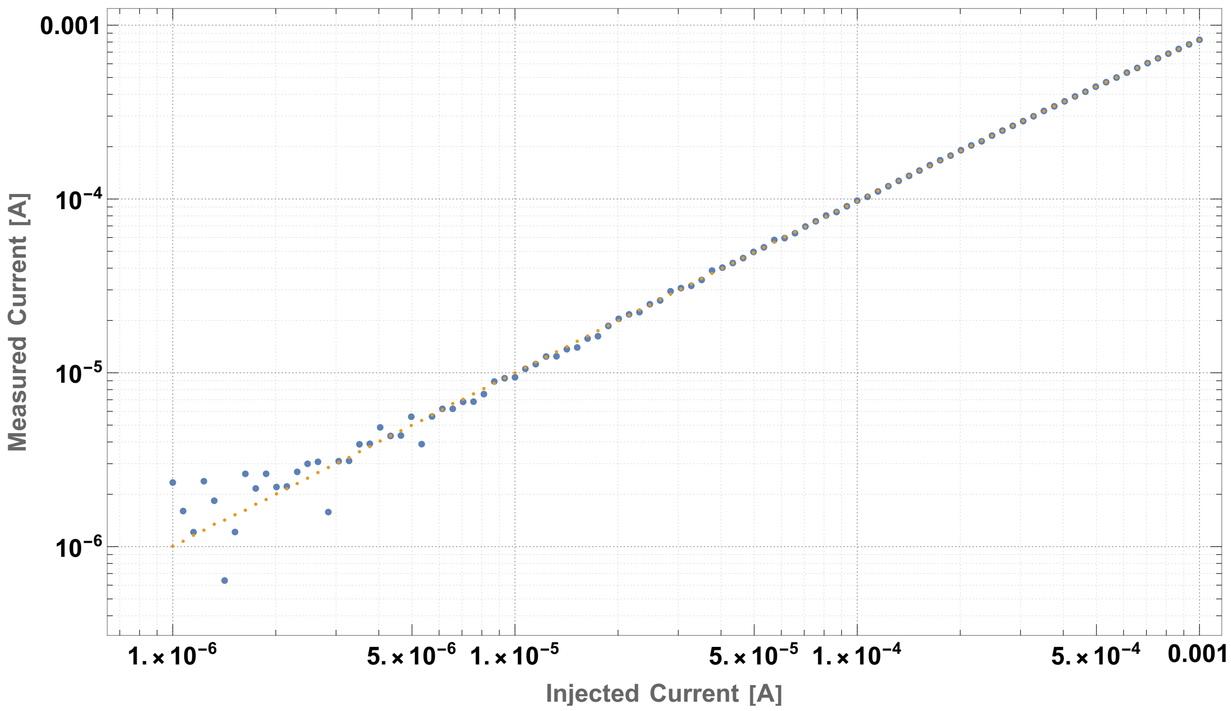
Conversion characteristic (left plot) and relative errors (right plot)
by a logarithmic current sweep of 500 values from 1 nA to 1 mA. The averaging time window is set to 100 μs.

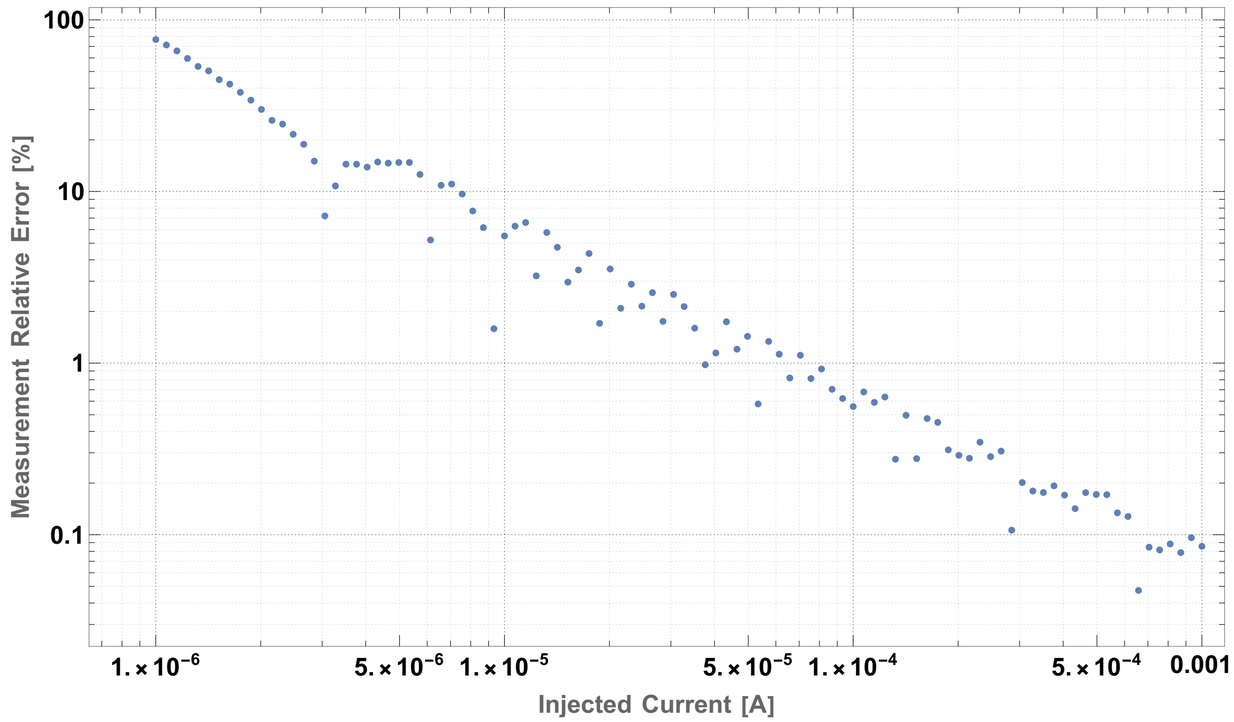
Relative Error :

- Below 10 % from currents greater than 3μA
- Below 1 % from 35μA to 1mA

Front-End Conversion Characteristic high currents

with BLMASICv3





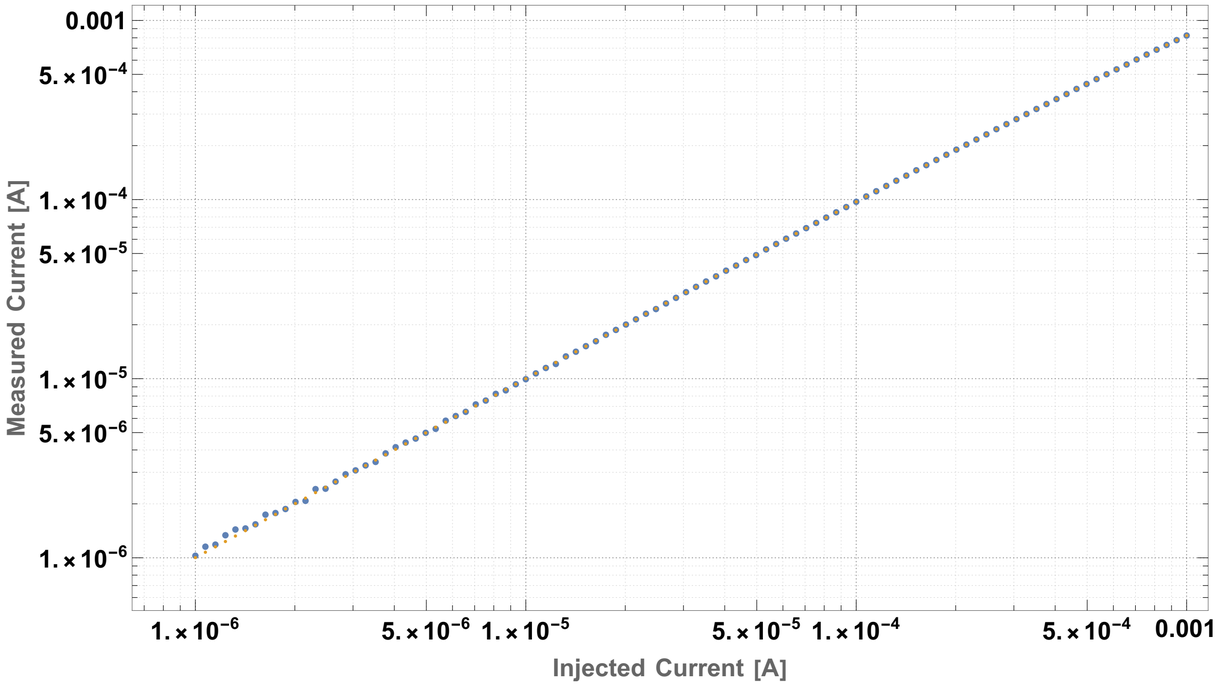
Results obtained by Double Precision IIR filtering of the CFC counter data.

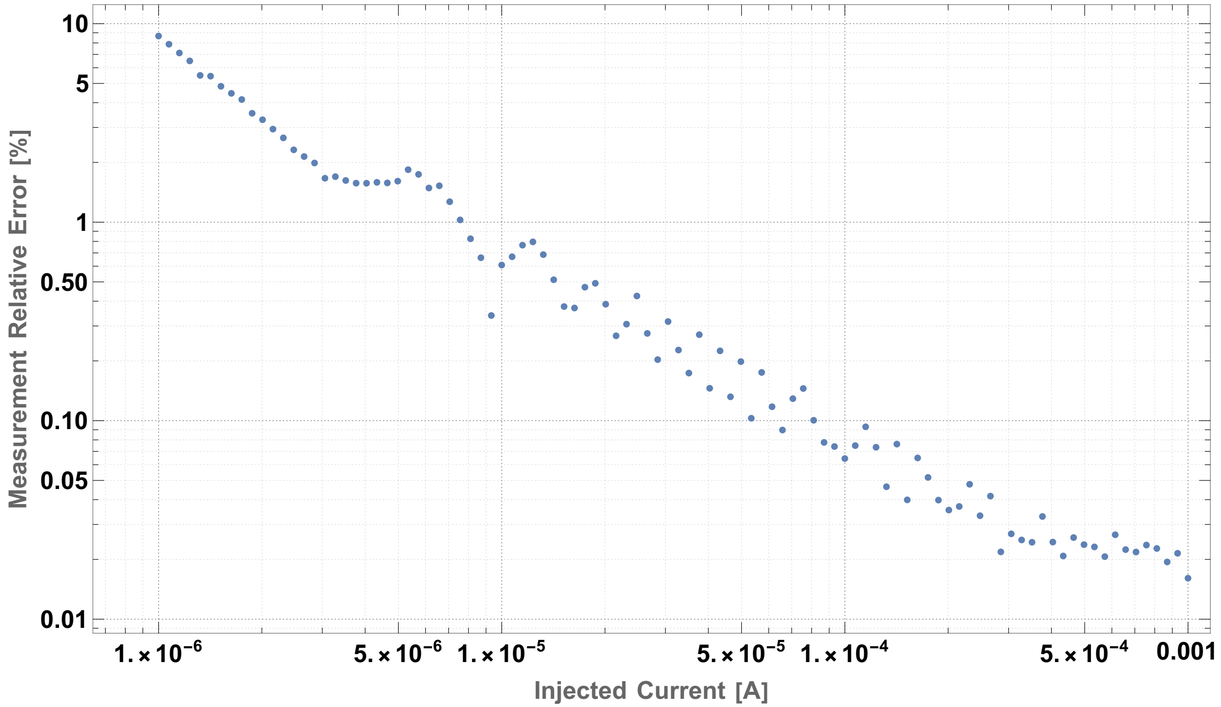
Cutting Frequency = 10 kHz *(Rise Time equivalent to that of a moving average FIR 43.8 μs wide)*

Error below 10% for currents greater than 7 μA

Front-End Conversion Characteristic high currents

with BLMASICv3





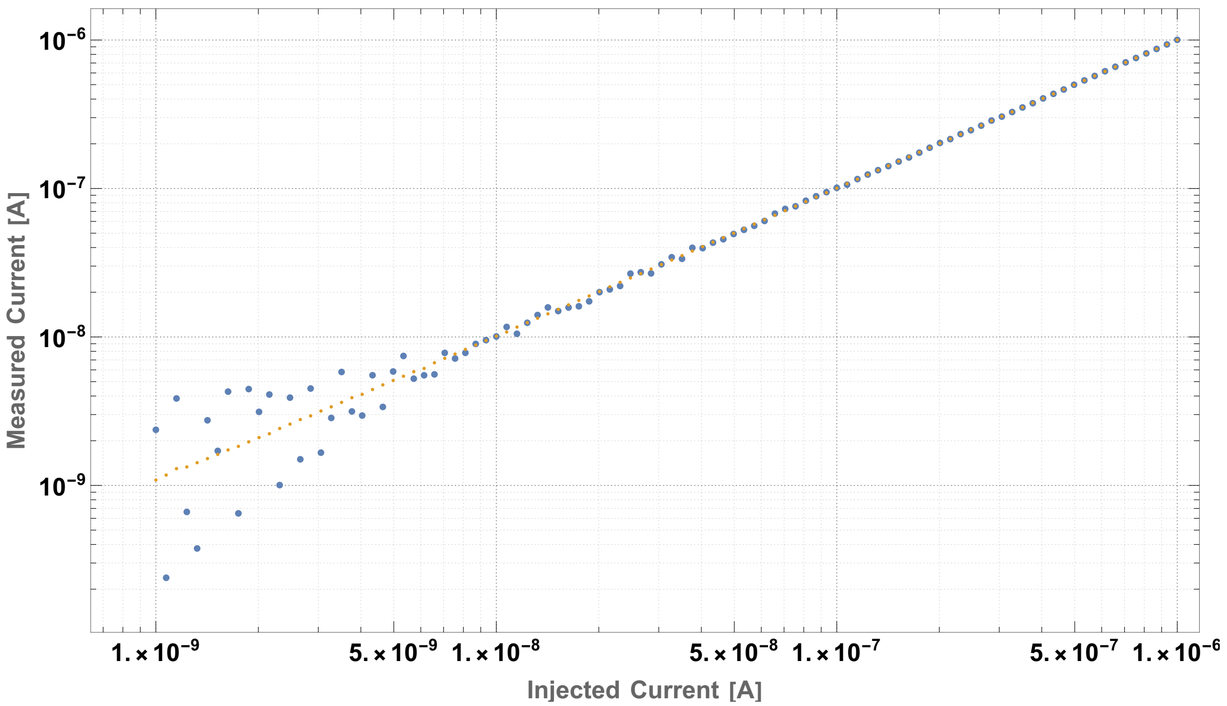
Results obtained by Double Precision IIR filtering of the CFC counter data.

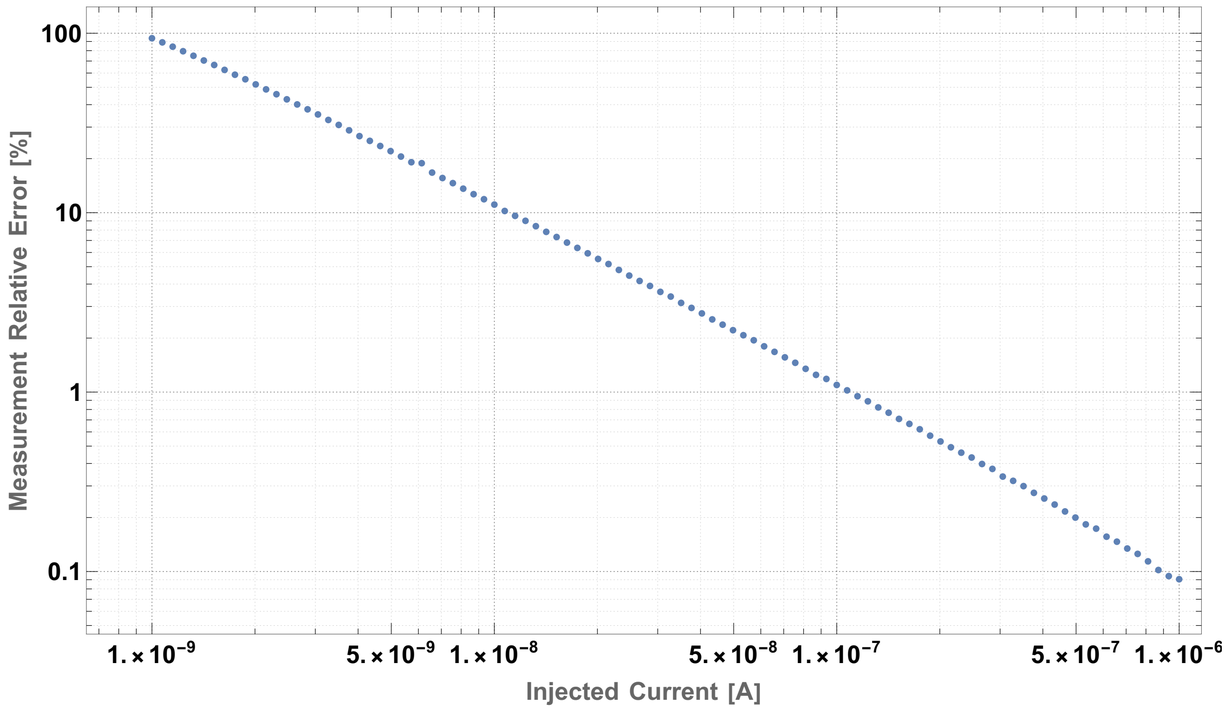
Cutting Frequency = 1 kHz *(Rise Time equivalent to that of a moving average FIR 438 μs wide)*

Error below 10% for currents greater than 1 μA

Front-End Conversion Characteristic low currents

with BLMASICv3





Results obtained by Double Precision IIR filtering of the CFC counter data.

Cutting Frequency = 10 Hz *(Rise Time equivalent to that of a moving average FIR 43.8 ms wide)*

Error below 10% for currents higher than 10 n*A*

Production Status and Costs Overview

BLMASIC Converter

- Three versions of the BLMASIC have been released so far.
- 200 × BLMASICv3 were delivered during 2021 Q4 (cost: 250$ each).
- The installation production will require a dedicated TSMC silicon mask of 200k$ non-recur. costs, several wafers of 5000 pieces each will be manufactured (~2023). *They are available to be used in other experiments / applications.*
- The final device cost (including package) will be less than 50$ / piece.

ASIC Based BLM Front-End (BLEIC)

- Several prototypes will be assembled soon for irradiation and beam test.
- It is uniquely based on CERN's ASICs and passive components.

  About 400 vs. > 2000 of the currently installed front-end
- The cost for the complete board is <1k$ vs. 3k$ of the installed front-end.

Roadmap and Targets

2021

Q1	Q2	Q3	Q4
Preliminary characterisation of the BLMASICv2 device and Front-End design review	Noise characterisation of the BLMASICv2 with the latest test-bed system. X-Rays irradiation sessions.	Submission of the BLMASICv3, Front-End card delivery and assembly	Acquisition Back-End firmware development and delivery of BLMASICv3 device

2022

Q1	Q2	Q3	Q4
Installation Front-End card conversion performance characterisation with BLMASICv3 and irradiation test	Beam test of the prototype system and reliability validations	Diagnostic features and availability validation	BLM system integration

Acknowledgements

ADC & other rad-hard ICs

- Kostas Kloukinas
- Alessandro Marchioro

BLMASIC

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- Pedro Vicente Leitao

LpGBT

- Daniel Hernandez Montesinos
- Paulo Moreira

SM-VTRx

- Jan Troska
- Carmelo Scarcella
- Leonardo Marcon
- Manoel Barros Marin

Rad-Tol COTS

- Rudy Ferraro
- Salvatore Danzeca

Fibre & Copper connections

- Jeremy Blanc
- Daniel Ricci

Thanks for the attention…

Questions?

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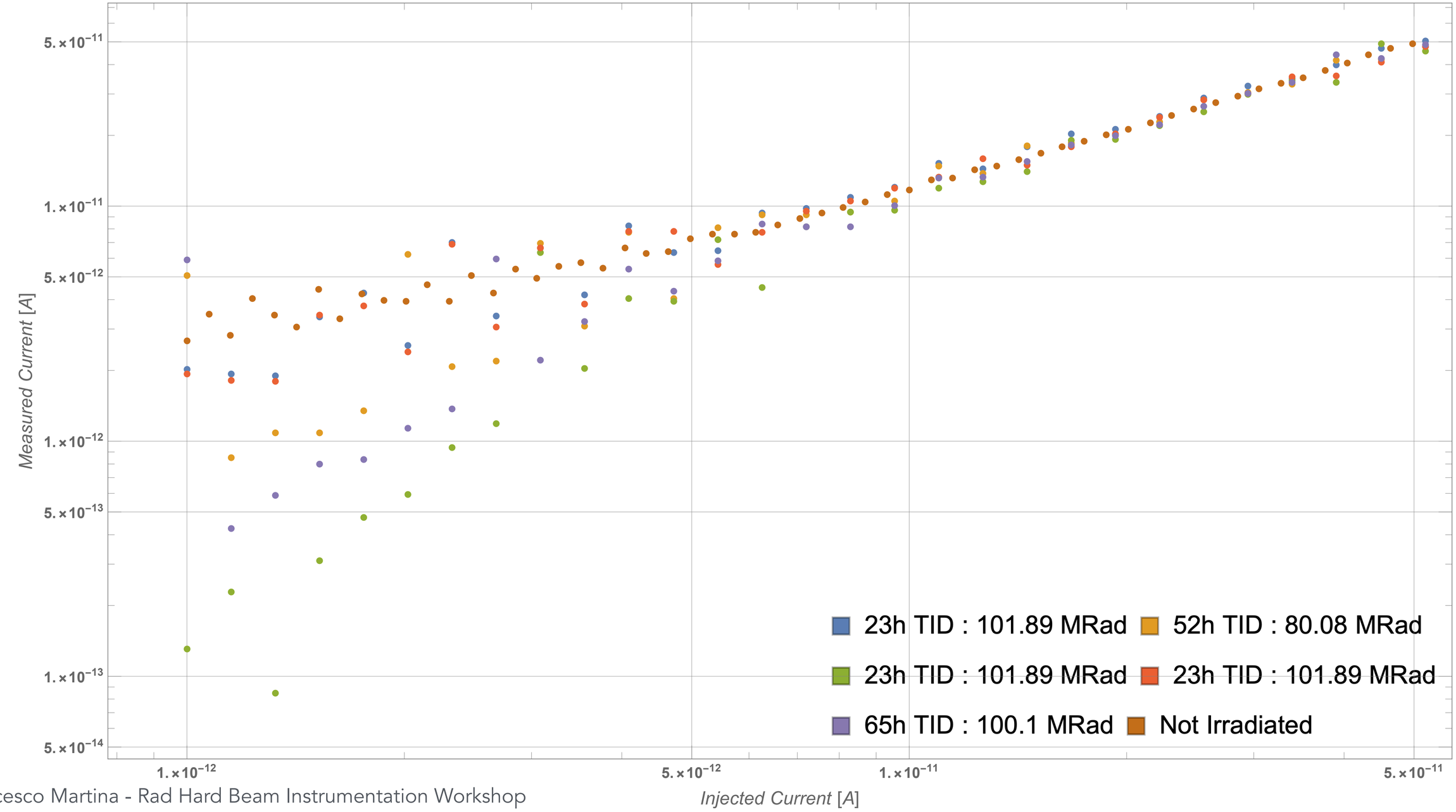
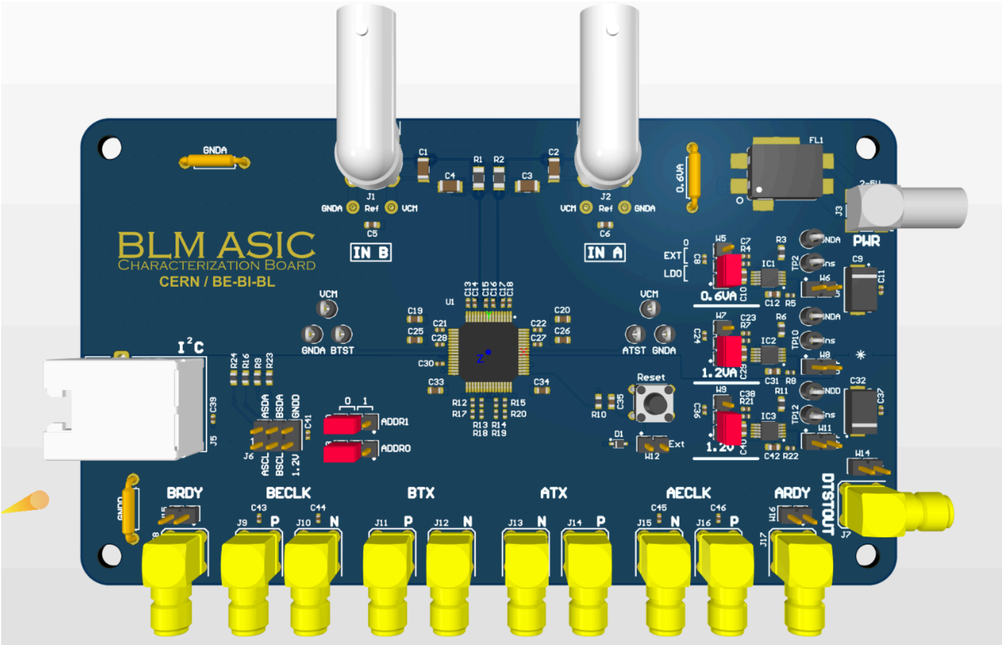
Backup Slides

Conversion Characteristic Results *low currents* *1 s Integration*

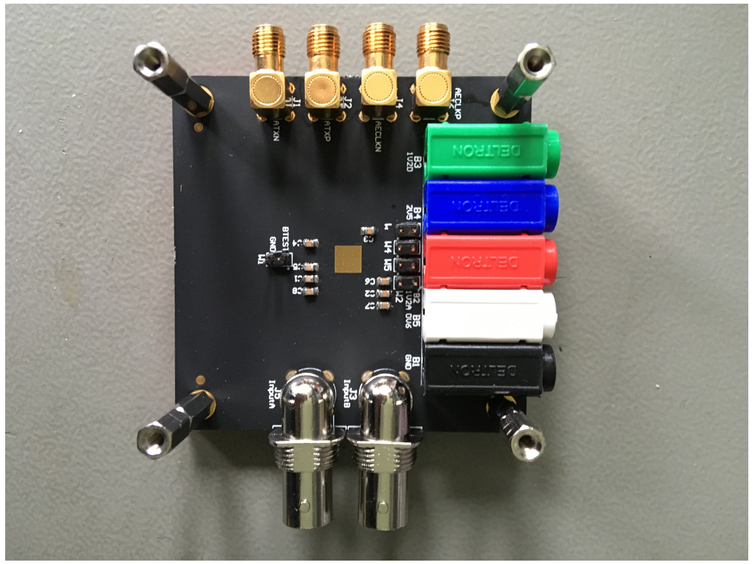


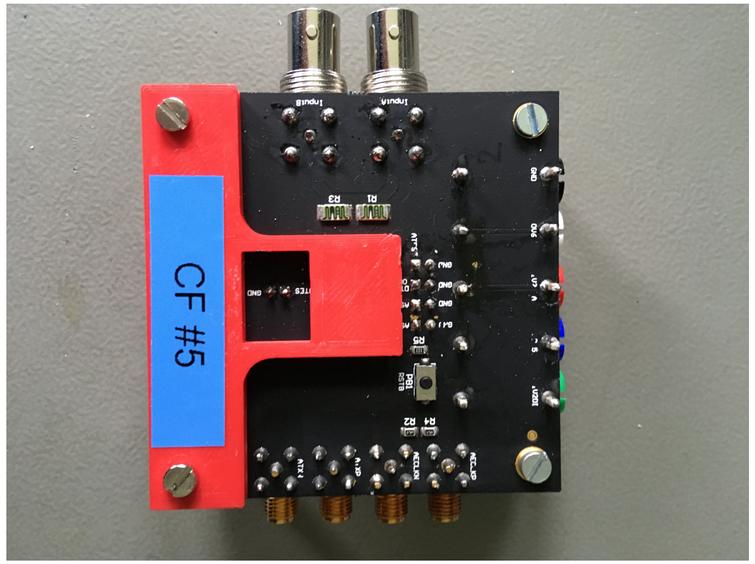
Irradiation details

XRAYs	Flux [MRad / h]	Time [h]	TID [MRad]
CFC#0	Not Irradiated	0	0
CFC#1	4.43	23	102
CFC#2	1.54	52	80
CFC#3	4.43	23	102
CFC#4	4.43	23	102
CFC#5	1.54	65	100



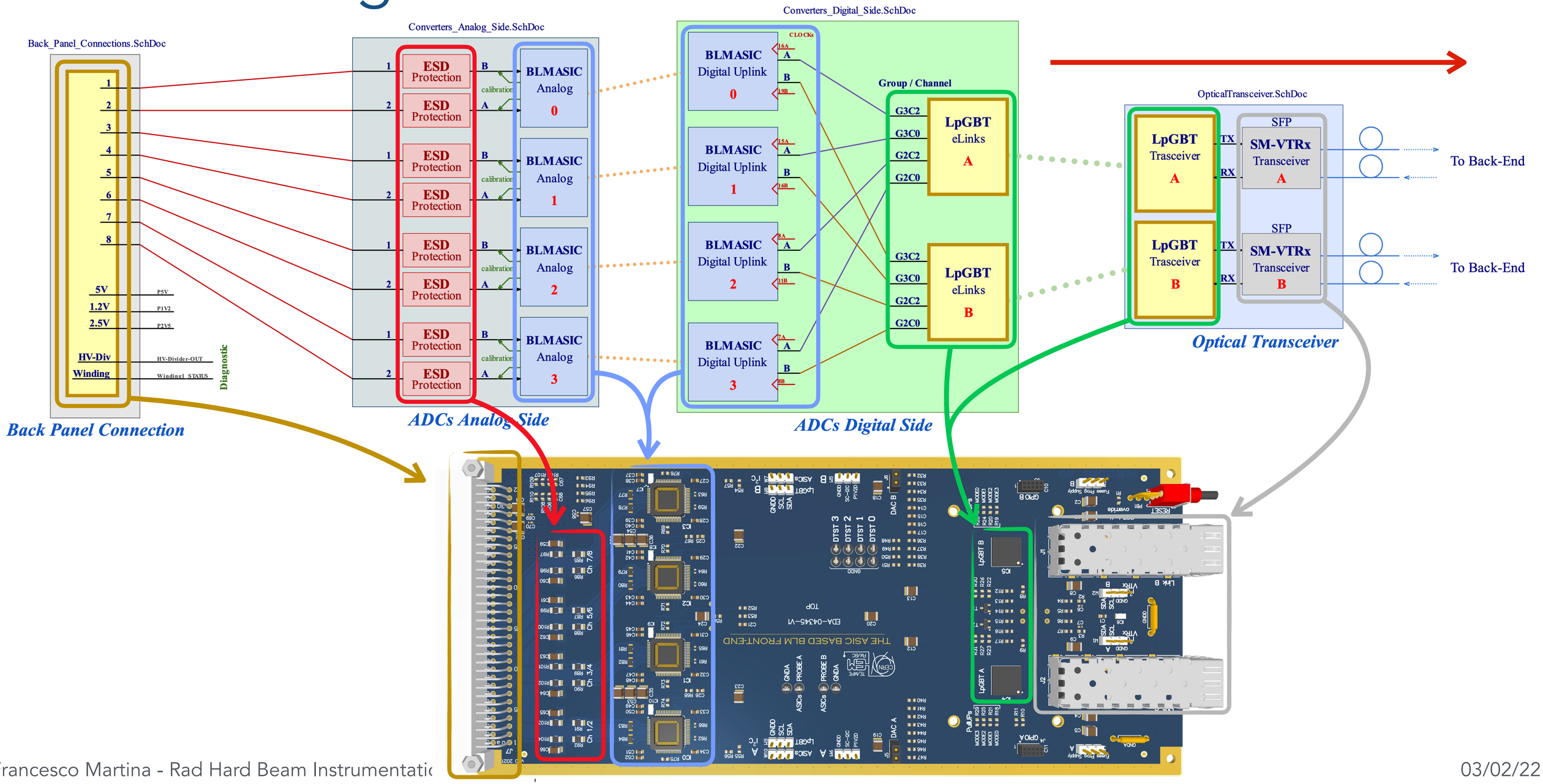
Mainstream Prototype board used for the electric characterisation





Breakout board used for the Irradiation Tests

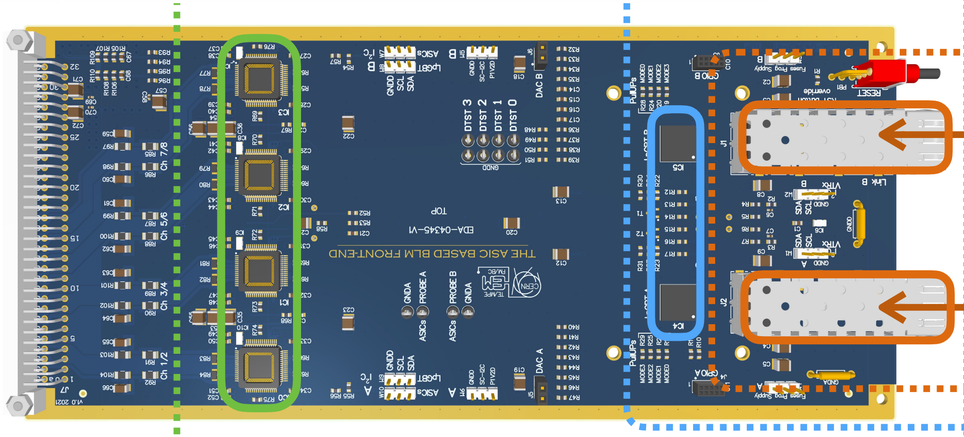
Front-End Signal Path



Overall acquisition system signal path

Open Systems Interconnection (OSI) Model

Host Layers	APPLICATION	Network process to Application, User end APIs, resource sharing, remote file access, etc.	DATA
	PRESENTATION	Translation of data like character encoding, encryption/decryption, data compression, etc.	DATA
	SESSION	Establish, maintain and gracefully shut down the session.	DATA
	TRANSPORT	Reliable end to end communication, segmentation, flow-control, acknowledgement, and multiplexing	SEGMENT
Media Layers	NETWORK	Path determination, logical addressing, routing, traffic control	PACKET
	DATA LINK	Reliable node to node transmission of frames, MAC and LLC sublayers, Physical addressing	FRAMES
	PHYSICAL	Transmission/Reception of binary bit streams over physical medium, encoding/decoding at bit level	BITS



Application

Presentation

Network to Session

PHY to Data Link

5.12Gb/s Transceivers

LpGBT IP-Core (x2)

LpGBT Slow Control

BLMASIC Data Retriever

Diagnostics

Measurements Processing

Thresholds / Interlock

Front-End | *Back-End*