DEEP UNDERGROUND NEUTRINO EXPERIMENT

Imperial College London

Firwmare design

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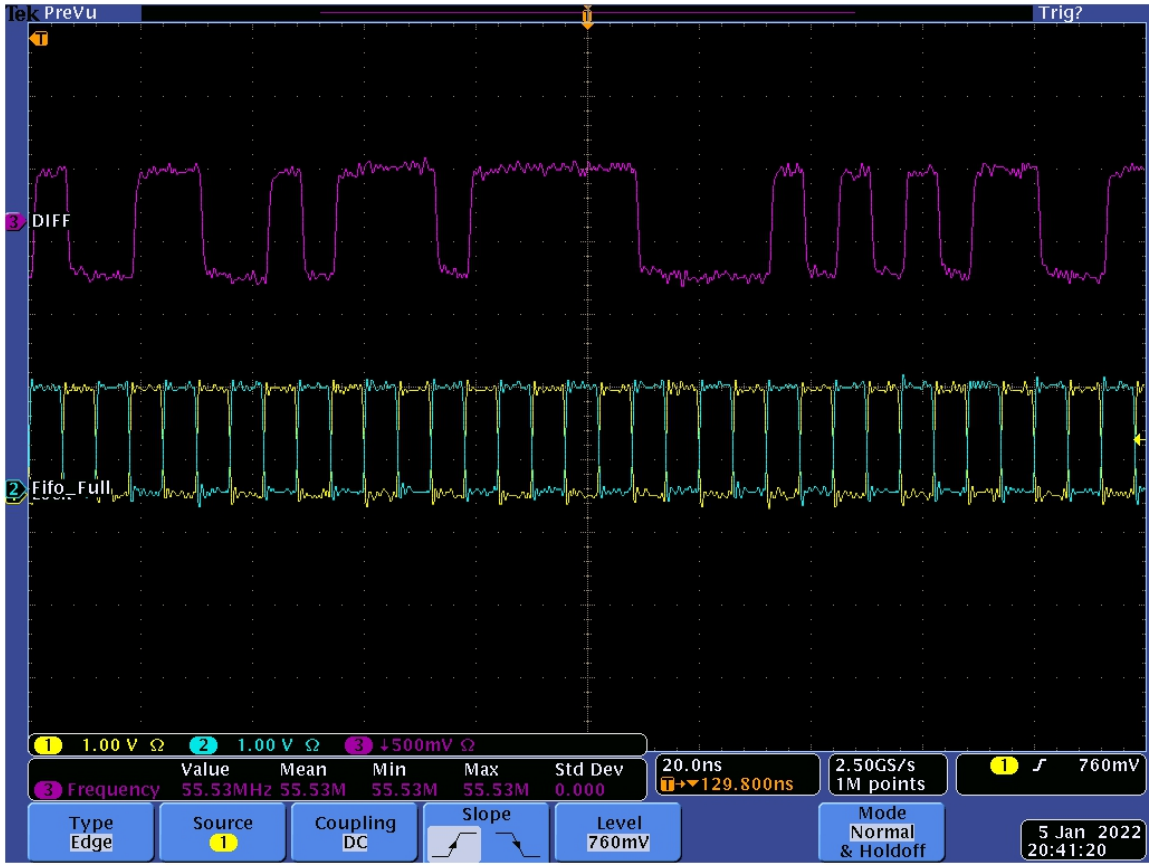
- Meeting: HPgTPC electronics meeting (Imperial)
- Date: 11/1/21

Current situation with hardware tests

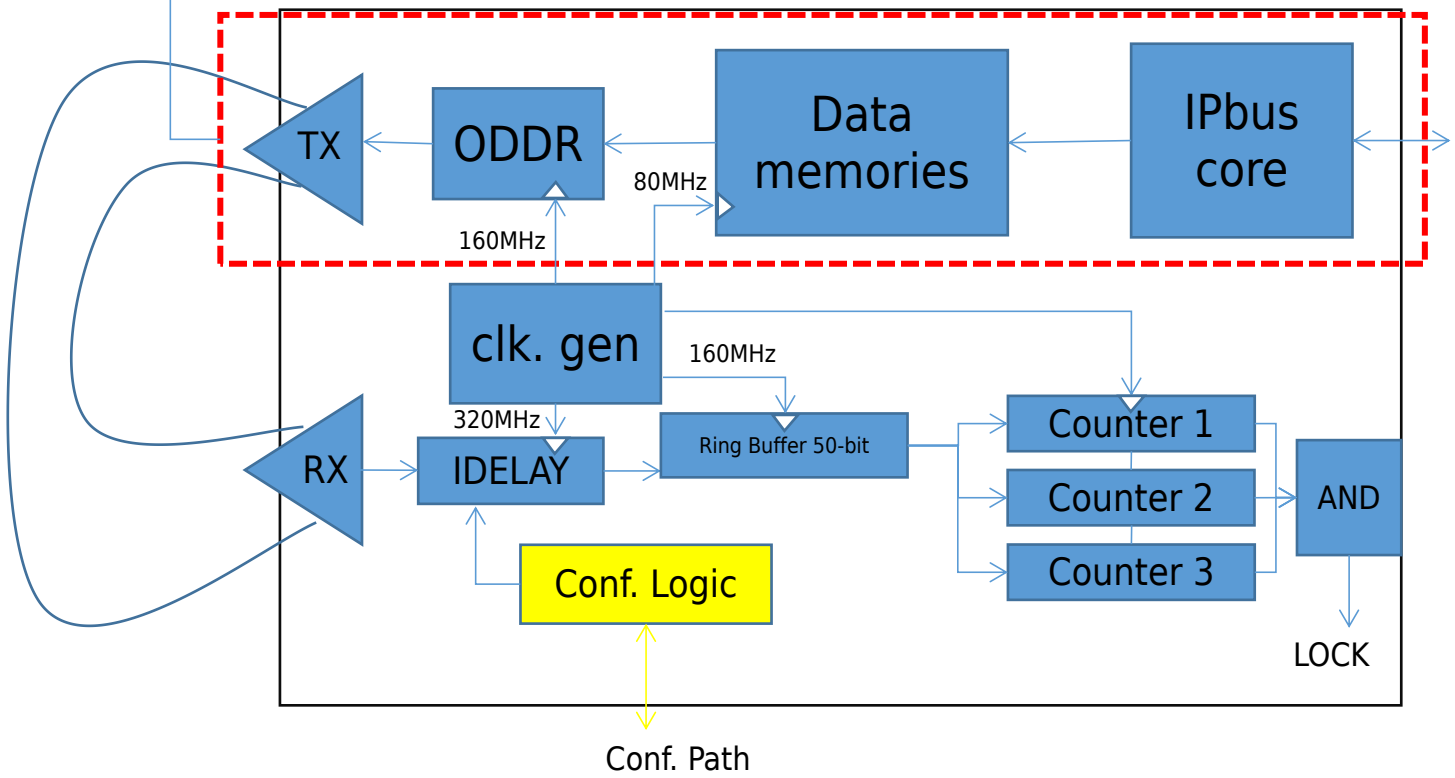
- AGGR <-> TIP links:
  - Eye-scans retrieved for all links with all possible configurations of old inductors
  - Eye-scans with new inductors in both RX,TX path and in RX/TX-only have been retrieved for 10m cable (baseline)
  - Analysis is needed to identify critical path
- FEC <-> AGGR
  - Transfering 160Mbit of data with 80MHz clock from 12x lines shows sharp and nice transistions
    - Line-0: Is sending 160MHz clock to “fake” SAMPA
    - Use also for trigger when probing the signals



Aggregator firmware status

- Interface blocks for ethernet and aurora in place
- On the front-end side the bit alignment logic has been implemented and tested with ribbon cable loopback
- Generation path connected to IPbus for simplicity but can be connected to SiTCP once software is available
  - Multiple operation modes available

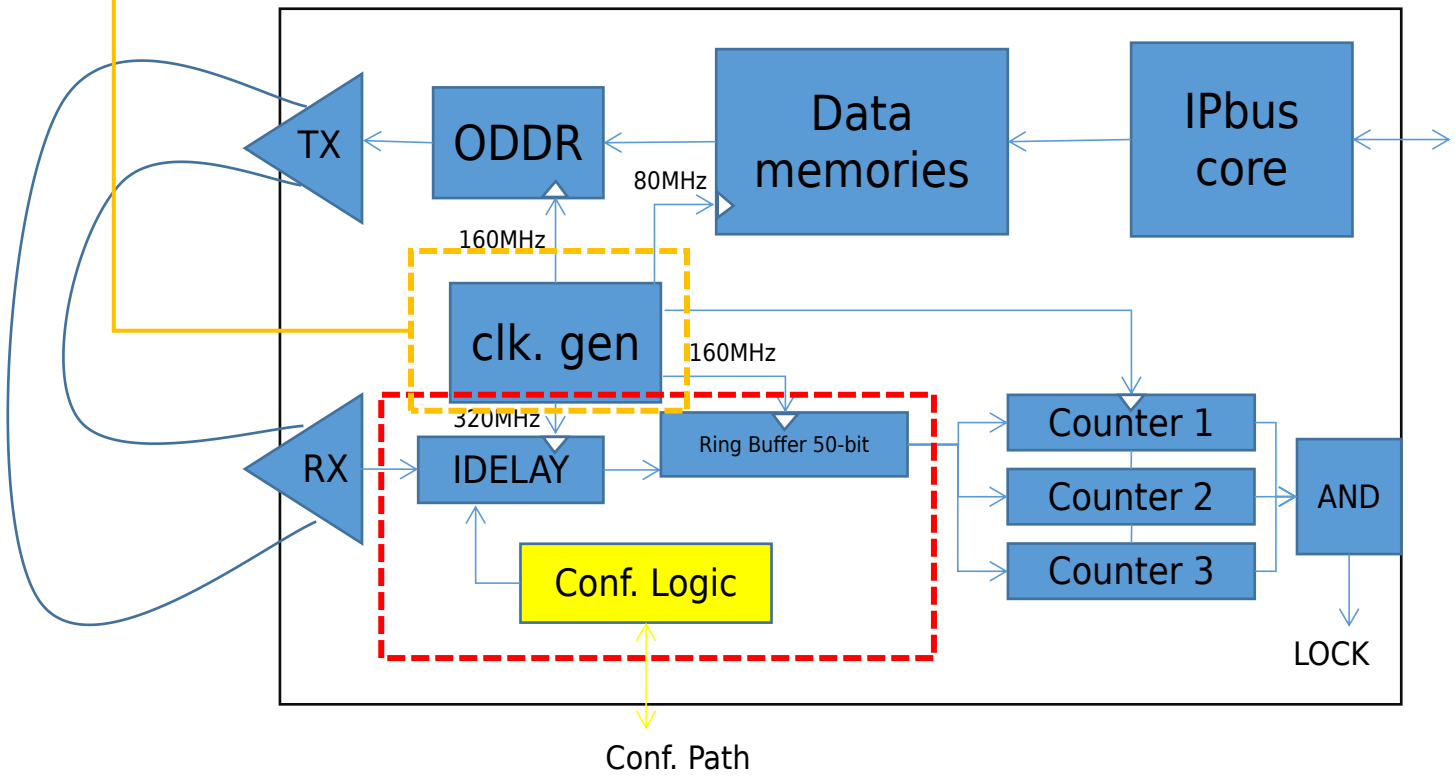
The generation part has the following capabilities and can be easily expanded:
1) Send SAMPA sync packets
2) Clock signals
3) Random patterns from software
All implemented in FSM further modes can be easily added (e.g. SAMPA like data streams)



Aggregator firmware status

- IDELAY: Xilinx specific primitive
  - Not callibrated (for temp, voltage, etc.)
  - Callibration can happen via software (e.g. CCM path)
  - Max dealy for KU FPGA's: 512 taps (min: 2.5-15ps, max: 1.2-7.9ns)
  - Sampling clock 320MHz: 3.125ns
- Output stream CDC to 160MHz clock falling edge to ensure being in the middle of the pulse eye (this will need to be evaluated)
- 50-bit wide ring buffer retrieves incoming bit stream to be compared with expected header value (stored in register, or adjustable from CCM)

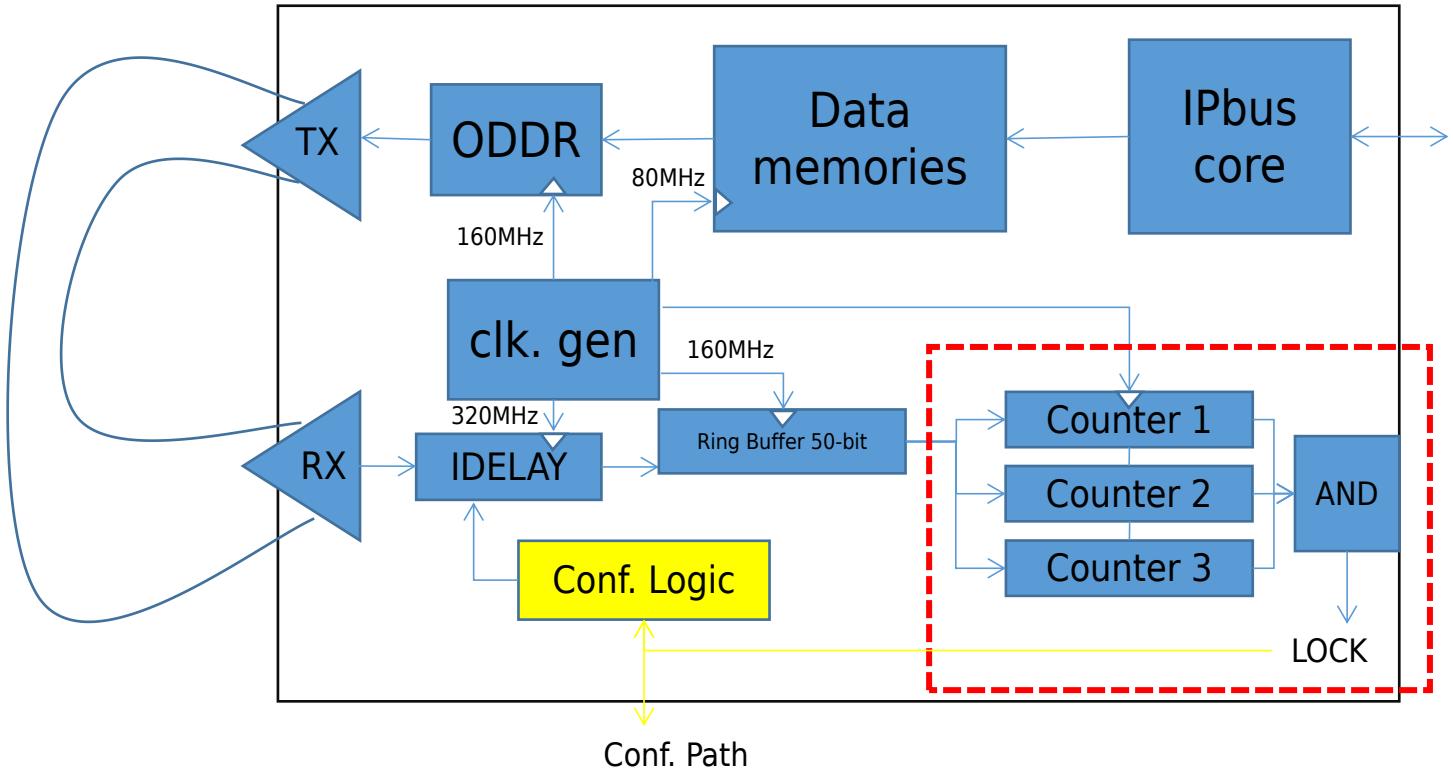
Clk: generation from recovered 62.5MHz clock
-> Ensures alignment with TIP clock
-> Till current design version 1x MMCM was sufficient



Aggregator firmware status

- If tap delay sufficient then 50-bit counter starts once sync. packet expectation same as ring buffer value
  - Cascade of 50-bit counters enabled when previous counter coincides with 50-ring buffer comparison
  - Once 3 counters (#Counters generic) succeed then lock signal indicated ends of calibration
  - Control packet to TIP for CCM path
- After callibration 10-bit counter provides parallel data to FIFO (size x1024 only if not sync_packet)
  - Based on format every 4x packets info if packet is sync or header (discussion on this next time)

* Memory usage estimate:
1x BRAM block = 36Kb (can split in 2x18Kb)
* 1x FIFO = 1024 x 12-bit (2'b: debug 10'b: data) = ~13Kb (1024 fits max. SAMPA payload)
* Every channel pair 1xBRAM block hence 28x BRAMS per aggregator (~5.2% utilization)



Proposal on timestamping

- SAMPA counter sync to ref. clk (160MHz)
  - 10-bit@20MHz, with max window = 5.1µs
    - Stamps: First cluster over threshold
    - Reset: Every time window (in continuous mode overflows after max value unless trigger or master reset)
  - 20-bit@40MHz, with max window = 2.6ms
    - Stamps: Time window begining (after reset if no signal over threshold should reset with 10-bit counter every ~5x clock periods)
    - Reset: Either with master reset or overflow after full window

- Beam spill ~1 sec but no beam spill clock available for the system
- Proposal: 26-bit counter in aggr. provides ~1.7s window (adding all spares allows window to 14mins max)@40MHz (sync. to 160MHz)
  - Shifter triggers beginning of run
  - 40MHz SAMPA exits reset and aggr. counter aligned with BX counter (max off by cable delay?)
  - When packet with clusters above threshold retrieved BX counter value and time stamp mark aggr. value added on aurora header (next time data-format discussion)
  - If aggr. counter overflows control packet will be send to TIP to mark new 1.7s window
- TIP will sync. aggregator counters with server unix clock

Next steps - Thoughts

- Do we have a better timestamping proposal?
- Data formatting for aurora and ethernet is finalised (will show next time details)
  - Roughly: 64-bit header/trailors (aligned with PACMAN firmware on far detector)
- Current developments:
  - Firmware for data capture tested with 0.5m cables and lock was succeed without having to change delay value (nominal 2.5ps tapping -> might work also with 0ps but good to have delay primitive in)
  - FSM developed for retrieving SAMPA header in 10-bits and payload and convert to 16-bit Aurora data stored in larger FIFO memories every 7x SAMPA front ends
    - If ~8k locations of 16-bit needed per group of 7x SAMPA then x4 BRAM per group = 36x BRAM. Grand total: 36+28 = 63x BRAM (11.5%) (if I add 30% contingency: ~15% usage)
    - Initially I will design with those values and then optimize to cover all BRAMs. Of course sim. from expected rates will be useful as well if BRAM usage becomes critical
  - Conf. FSM for alignment and configuring the SAMPA started to be developed with currently the enable FEC, align incoming data options (detailed FSM functionalities documented)
  - Discussions with CCM/Data format software groups to start installing DUNE sw to send streams of data from TCP (stop using IPbus)

Next steps - Thoughts

- Few thoughts before next step:
  - Most firmware blocks are designed with generic parameters about mem. size, specific components, etc.
  - All designs are tested also for timing given the current values to avoid future surprises
    - This doesn’t mean that extrapolating to full FPGA utilization will be straight forward
    - Differences expected when FPGA package changes to final version (once substantial firmware block ready, migration will happen for compiling with target chip)
  - Detailed documention for every firmware block is attempted to be maintained (have already an overleaf doc.)
    - Due to thesis viva imminent, some updates are needed
  - Small scale tests with firmware block easy to connect to IPbus and test on workbench setup
  - After ribbon cable tests and eye scans on ethernet much more confident for firmware operation
- Next steps:
  - Design 1x slice in the firmware with 7xFEC (2x SAMPA) to Aurora link, to check critical aspects on data rates
  - Start implementation of priority logic between 9x groups (can be also ported to TIP)
  - Main focus shifted to configuration and monitoring path to start finalising complete functionality list
  - Proto-fw version till easter (possible)