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Whitepaper 1: MPGDs: Recent advances and current R&D

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ABSTRACT

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1 Executive Summary

2 Development of the Micro-Pattern gaseous detector technologies: an overview of the CERN-RD51 collaboration

The modern photo-lithographic technology on flexible and standard PCB substrates favored the invention, in the last years of the 20^{th} century, of novel Micro-Pattern Gas Detectors (MPGD); among them: the Micro-Strip Gas Chamber (MSGC) [1], the Gas Electron Multiplier [2] (GEM) and the MicroMegas (MM) [3]. Since the very beginning, the goal was the development of novel detectors with very high spatial $\mathcal{O}(50\,\mu\text{m})$ and time (ns) resolution, large dynamic range, high-rate capability (up to 10^6 Hz/mm^2), large sensitive area and radiation hardness - making them an invaluable tool to confront future detector challenges at the frontiers of research. The dedication of several groups of MPGD developers has led to rapid progress, crowned by new inventions and understanding of the underlying operation mechanisms of the different detector concepts. MPGDs promised to fill a gap between the high-performance but expensive solid-state detectors, and cheap but rate-limited traditional wire chambers. Nevertheless, the integration of MPGDs in large experiments was not rapid, despite of the first large-scale application within the COMPASS experiment [4] at CERN SPS in the early days of the 21^{th} century. In COMPASS, telescopes of MMs and GEM trackers demonstrated reference performance at particle fluxes of 25 kHz/mm^2, with space resolution better than 100 μm and time resolution of $\mathcal{O}(10$ ns). Thus, the potentiality of MPGD technologies became evident and the interest in their applications has grown in the High Energy Physics (HEP) and Nuclear Physics domains, and beyond. Consequently, it became crucial to consolidate and enlarge the dedicated community to foster further developments and dissemination of MPGD applications in the HEP sector and other fields. The RD51 CERN-based technological collaboration, started in 2008, now has 90 institutions from 25 countries. Since its foundation, the RD51 collaboration has provided important stimulus, and has become a major focus, for the development of MPGDs. While a number of the MPGD technologies were introduced before RD51 was founded, with more techniques becoming available or affordable, new detection concepts are still being introduced, and existing ones are being substantially improved. The nature and extent of the collaboration activities is reflected in the seven Working Groups (WG), transversal to the RD51 activities, covering all relevant R&D topics: MPGD technologies and novel structures, detector characterization, study of the physical phenomena and detector simulations, dedicated electronics tools for read-out and laboratory studies, production and engineering aspects, common test facilities, and dissemination beyond the HEP community - including dedicated education and training. Important consolidation of the some better-established MPGD technologies has been reached within the RD51 collaboration, often driven by the working conditions of large collider experiments. One of the breakthroughs came with the development of MM with resistive anodes for discharge mitigation [5], in the context of the ATLAS New Small Wheel (NSW) project. This concept allows limiting the energy of occasional discharges and results in a protection of both the detector and its front-end electronics and, equally relevant, in a substantial dead-time reduction (time required to re-establish the operational voltage). The resistive anodes have been obtained by a variety of approaches: photo-lithography, screen-printing technologies and sputtering.
The construction of GEM-detectors centers on two main issues: GEM-foil production and

preservation of the correct spacing between successive GEMs in multilayer configurations. Initially GEM foils were produced using a double-mask approach with the chemical etching performed from both foil faces. The difficulty of aligning the two masks, limiting the achievable lateral size to 50 cm, led to the development of a single-mask production protocol. It was initially developed for the upgrade of the TOTEM experiment [6], further used to produce GEM foils for the KLOE2 cylindrical GEM-detector [7] and those of the CMS forward muon spectrometer [8]. The requirement to preserve the constant inter-foil spacing in multilayer GEM detectors of large-size was first fulfilled successfully, though with small dead-zones, by adequate spacers; e.g. in COMPASS [9] and TOTEM [10] trackers. Later, the INFN groups involved in the construction of the GEM-based trackers for LHCb experiment introduced an alternative approach: GEM-foil stretching prior to gluing on support frames [11]. This concept also paved the way to the construction of a cylindrical-GEM detector [7]. Further extension of the stretching technique has been introduced for the CMS forward muon spectrometer [8]: to save a relevant fraction of the assembly time the foils are mechanically fixed onto the frames, where they are mechanically stretched and kept at the correct tension without gluing. This NS2 technique, no-stretch no-spacer method, originally presented by R. de Olivera at MPGD2013 [12], has become the basis of the GEM-detector construction for the CMS upgrade. Nowadays, the single-mask GEM technology, together with the NS2 technique, simplifies the fabrication process, resulting in an important minimization of the production time – particularly relevant for large-volume production (Fig. 3). So far, the largest GEM foil production has been finalized and the GEMs are in place for the upgrade of the ALICE Time Projection Chamber (TPC) [13]. The demanding requirements of a TPC, where fine resolution tracking and good dE/dx accuracy are equally relevant, has imposed a detailed and stringent quality assessment protocol. Therefore, this construction effort represents the first fully-engineered large mass-production of MPGDs.

THick GEMs (THGEM), also referred to in the literature as Large Electron Multipliers (LEM), were introduced in parallel by several groups at the beginning of the 21^{st} century [14]. They are derived from the GEM design, scaling up 10-fold the geometrical parameters and changing the production technology. The Cu-coated polyimide foil of the GEM multipliers is replaced by that of standard PCBs (e.g. FR4) and mechanical drilling produces the holes.

The consolidation of the better-established technologies has been accompanied by the flourishing of novel technologies, often specific to well-defined applications. These technologies are derived from MM and GEM concepts, or they are hybrid approaches combining different MPGDs technologies and gaseous with non-gaseous detectors, or they are entirely new architectures. Novel technologies are illustrated by the following selected examples. The Gridpix counter [15] is obtained applying, by post-processing, a small-scale micromesh directly onto a Timepix chip [16], therefore obtaining a miniaturized MM with the fine granularity of the Timepix itself. The very fine space resolution has been confirmed using a set of Gridpix units as read-out sensors of the ILC TPC prototype [15]. GEM geometries where extra electrodes are added onto one of the two GEM-foil faces aim at improving the capability of multilayer GEM detectors to trap the ions flowing back from the multiplication region, a feature required for performing gaseous photon detectors and for TPC sensors: Micro Hole and Strip Plates [17] and Cobra [18] architectures have been designed and characterized.

A promising GEM-derived architecture is that of the μR-WELL [19], where the anode is directly placed at the hole bottom, forming the well structure, in order to maximize the collection of the avalanche electrons, and it is realized by a resistive layer for spark protection: in this architecture, a single multiplication layer is present.

Initially, GEMs had been introduced to act as a preamplifier stage in gaseous detectors [20] and, therefore, the concept of the hybrid approach has been present since the very beginning in the MPGD concepts. More recently, electron multipliers have been coupled to devices capable to detect the luminescent light produced in the amplification process: in GEM TPC with optical read-out [21] and THGEM-based read-out for double-phase liquid Ar detectors [22]. A final MM multiplication stage is added to GEM or THGEM multipliers in order to control the ion backflow making use of the intrinsic ion trapping capability of the MM principle; the GEMs and MM scheme has been proposed as read-out sensor of the ALICE TPC [13]*, while THGEMs and MM are the basis structure of novel gaseous photon detectors [23]. A GEM foil facing the Medipix chip [24], forming the GEMpix detectors [25], is in use for medical applications as well the treatment of radioactive waste [26]. The μPIC [27] is a fully industrially produced PCB including anode strips on one face and orthogonal cathode strips on the other face. A regular pattern of uncoated zones is present in the cathode strips; an electric conductor buried in the PCB brings the anode voltage to a dot at the center of each uncoated zones: the multiplication takes place there, thanks to the electric field established between the cathode strips and the anode dot. A resistive coating of the cathode strips ensures the spark tolerance of the detector.

A key development which facilitates and encourages the development and use of MPGDs is the realization of the Scalable Readout System (SRS) [28]. This is a multichannel readout solution for a wide range of detector types and detector complexities. The scalable architecture, achieved using multi-Gbps point-to-point links with no buses involved, allows the user to tailor the system size to his needs. The modular topology enables the integration of different front-end ASICs, giving the user the possibility to use the most appropriate front-end for his purpose or to build a heterogeneous experimental apparatus which integrates different front-ends into the same DAQ system. The SRS system is today available through the CERN store or via the CERN Knowledge Transfer office. More than fifty groups are today using SRS for their R&D or experiments. The new, extended SRS-e paradigm adds realtime trigger functionality, deep trigger pipelines and a generalized frontend link via the new eFEC concentrator card. Horizontal links synchronize clocks and realtime actions, and the vertical links can be connected as vertical or horizontal readout architectures. Trigger extensions for SRS-e are discussed in section 5 below.

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3 High precision timing with the PICOSEC Micromegas detector

New challenges in current and future accelerator facilities have set stricter requirements on the timing and rate capabilities of particle detectors. The PICOSEC Micromegas detector has proven to time the arrival of Minimum Ionizing Particles (MIPs) with a sub-25 ps precision. Model predictions and laser beam tests demonstrated that an optimized PICOSEC design can time single photons with an accuracy of 45 ps which indicates an improved resolution in timing MIPs of the order of 15 ps. We propose the implementation of the PICOSEC detector for timing the arrival of EM showers with very high precision as well as for Time-of-Flight measurements for particle identification applications.

3.1 The PICOSEC Micromegas concept

The PICOSEC detector [1] consists of a two-stage Micromegas [2] coupled to a front window that acts as a Cherenkov radiator coated with a photocathode. A sketch of the detector concept is shown in Fig. 1. The drift region is very thin ($< 200\mu m$) minimizing the probability of direct gas ionization as well as diffusion effects on the signal timing. Due to the high electric field, photoelectrons (pes) undergo pre-amplification in the drift region. The readout is a bulk [3] Micromegas, which consists of a woven mesh and an anode plane separated by a gap of about 128 mm, mechanically defined by pillars. A relativistic charged particle traversing the radiator produces UV photons, which are simultaneously (RMS less than 10 ps) converted into primary pes at the photocathode. These primary pes produce pre-amplification avalanches in the drift region. A fraction of the pre-amplification electrons (about 25%) traverse the mesh and are finally amplified in the amplification region. The arrival of the amplified electrons at the anode produces a fast signal (with a rise-time of about 0.5 ns) referred to as the electron-peak (e^-peak), while the movement of the ions produced in the amplification gap generates a slower component for the ion-tail (about 100 ns). This type of detector operated with Neon- or CF4-based gas mixtures can reach high enough gains to detect single pes.

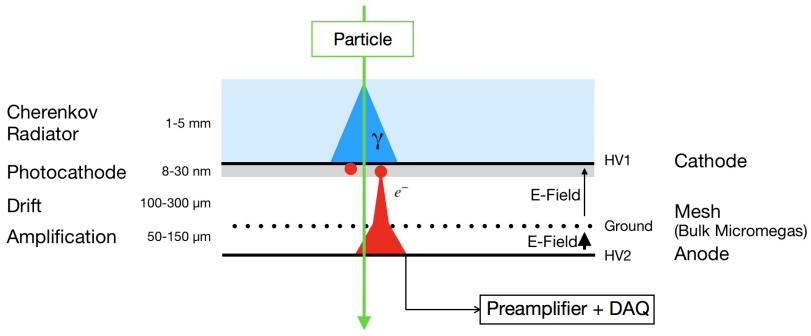

Figure 1: Sketch of the PICOSEC-Micromegas working principle,

3.2 Achievements in precise timing

The time response of a single-cell PICOSEC prototype detector (circular anode of 1 cm diameter) to single photons and to Minimum Ionizing Particles (MIPs) was extensively studied in laser and particle beams. The PICOSEC waveforms were fully digitized by a fast oscilloscope and analyzed offline to determine the e-peak charge and amplitude as well as the Signal Arrival Time (SAT), which is defined as the time measured at 20% of the signal amplitude. As reported in Ref. [1], the resolution for timing single photons was measured to be 76.0±0.4 ps, while the accuracy for timing the arrival of muons (MIPs) was measured to be 24.0±0.3 ps using CsI photocathodes (with an average value of about 11 pes induced per MIP). Several technologies concerning photocathodes and resistive anodes have been evaluated, which guarantee radiation hardness and stability in operation while preserving the precise timing capability (28-34 ps) of the detector.

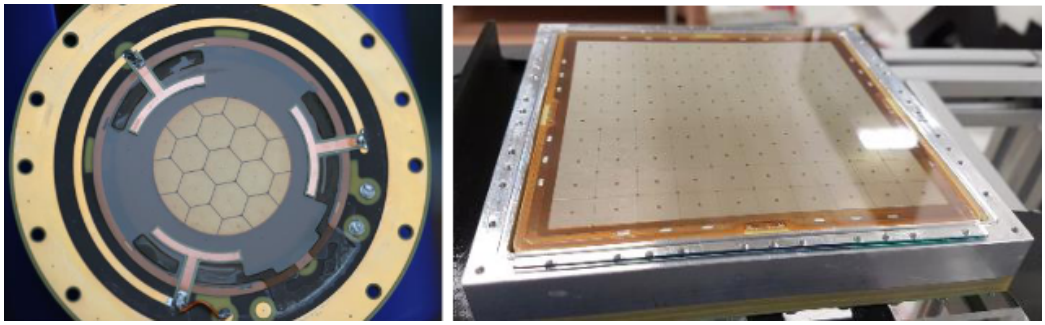

Figure 2: Multi-pad PICOSEC prototypes with active areas of about $10cm^2$ (left) and $100cm^2$ (right) respectively.

Aiming at large area detectors, multi-pad PICOSEC prototypes were developed, which comprise segmented anodes divided into either hexagonal or square pads (Fig. 2). Extensive tests in particle beams revealed that a detector with 19 hexagonal pads, each with 1 cm diameter, offers similar time resolution to the single-pad PICOSEC prototype. This remains true in the case that the incoming MIP induces signals in more than one of the neighboring pads (Fig. 3). Recently, particle-beam tests of an improved, larger prototype (comprising 100 $1cm \times 1cm$ pads) demonstrated even better timing capabilities [4, 5, 6]. Furthermore, a recent conceptual study [7], based on fully digitized PICOSEC waveforms, has shown that existing, cost-effective technologies [8] can be used for digitizing the signals of large, multi-pad detectors, while retaining the precise timing information. It has also been demonstrated [6, 7] that a trained Artificial Neural Network (ANN), fed with a partially digitized PICOSEC waveform (e.g. delivered by the SAMPIC [9] digitizer), provided extremely precise measurement of the signal arrival time. That indicates that PICOSEC detectors could offer timing information on real-time to be utilized for event selection. The Garfield++ simulation package [12], complemented with a custom made simulation of the electronics response, reproduces [13] very well the PICOSEC timing characteristics. In addition, a phenomenological model [14] was developed which describes stochastically the dynamics of the signal formation, in excellent agreement with the Garfield++ predictions and the

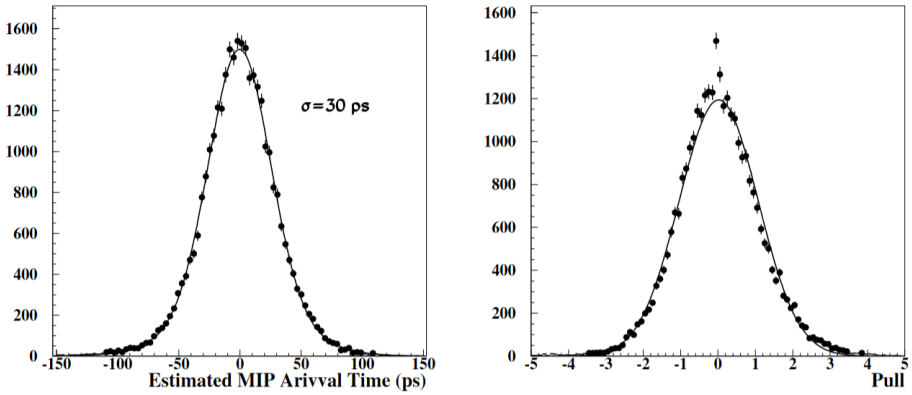

Figure 3: (left) Distribution of the arrival time of MIPs, passing within 3 mm of a common corner of four square pads estimated combining the individual single-pad measurements and their expected errors. The solid line represents a fit to the data points by a sum of two Gaussian functions corresponding to a σ of 30 ps. (right) Pull distribution of estimated arrival times. The solid line represents a Gaussian fit to the data points, consistent with mean and σ values equal to 0 and 1 respectively [10, 11].

experimental measurements. Recently, guided by the phenomenological model predictions, new PICOSEC designs were advanced that improve significantly the timing performance of the detector. As an example, PICOSEC prototypes with reduced drift gap size (about 120 μm) reached a resolution of 45 ps (in comparison to 76 ps of the standard PICOSEC prototype) in timing single photons in laser beam tests (Fig. 4).

It should be underlined that such a detector design maintains stable operation when irradiated with intense laser pulses, providing an excellent timing resolution of about 6.8 ps for about 70 pes. Optimized PICOSEC thin drift-gap design has been recently tested in particle beams and preliminary results [4, 5] confirm the observed performances during laser beam tests [15] with a resolution below 20 ps for MIPs.

3.3 Potential applications

The ongoing R&D in advancing scalable, radiation hard, resistive PICOSEC Micromegas detectors is focused in evaluating new thin-gap Micromegas designs, new photocathode materials, resistive-anode technologies as well as digitized electronics [16]. However, at this stage there are detector designs with proven operational virtues offering high timing precision. As an example, a PICOSEC detector embedded in an EM calorimeter could offer an excellent resolution in timing the arrival of EM showers. Indeed, the plethora of secondary relativistic electrons in the EM shower will induce a large number of pes even in the case that photocathodes (e.g. Al, Cr or Diamond Like Carbon-DLC) with very modest photon-yield are used. Moreover, metallic or DLC photocathodes are almost immune to radiation damage due to the ion back-flow in the Micromegas. According to simulations, a PICOSEC detector can offer a timing resolution of approximately 14 ps for

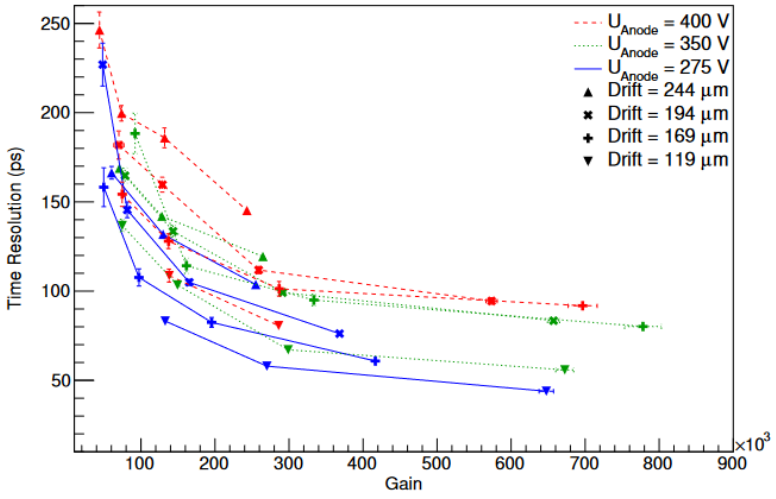

Figure 4: Time resolution as a function of the gain for different gap region thicknesses and anode bias voltages under single photo-electron conditions. The amplification gap is 128 μm deep [15].

5 GeV electrons, when the detector is embedded 2 radiation lengths inside the calorimeter. For higher energies, the expected resolution is much less than 10 ps. Tests in electron beams, scheduled for the Spring and Summer of 2022, will quantify the PICOSEC resolution to time high-energy electromagnetic showers. Recently, a dedicated R&D has started to design optimized PICOSEC prototypes for the ENUBET (Enhanced Neutrino Beams from Kaon Tagging) [17] project. These high-precision PICOSEC detectors aim at timing low energy (about 5 GeV) electron showers in the ENUBET decay tunnel or/and to time-tag electrons from Kaon decays or/and to time muons inside the hadron dump. Another possible application concerns the use of PICOSEC as a TOF detector to provide particle identification at low momenta. We have considered the case of using PICOSEC detectors, with 20 ps timing resolution, to separate e/π , π/K and K/p in the barrel and the forward region of a detector facility at the Electron Ion Collider [18]. Figure 5 shows the limits, in the momentum-pseudorapidity plane, in separating at a 3σ level (e.g. $3 \ \ x \ \sqrt{2} \ x \ 20ps$) between the above particles at the barrel and forward region. Although a better than 20 ps timing precision is needed in order to reach 3σ for e/π separation at 4 GeV/c, there is a wide momentum spectrum where the PICOSEC detector offers a good π/K and K/p separation.

3.4 Concluding Remarks

The RD51 PICOSEC collaboration focuses in advancing scalable, radiation hard, resistive PICOSEC Micromegas detectors for very precise timing, by evaluating new thin-gap Micromegas designs, new photocathode materials, resistive-anode technologies as well as digitization electronics. These activities motivates collaboration between groups with diverse expertise, something we are hoping to promote through this letter. However, even at

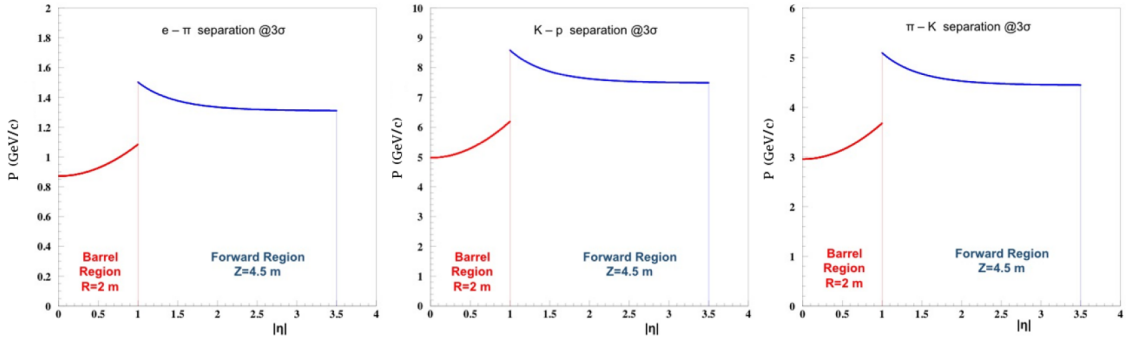

Figure 5: Estimated limits (at 3σ CL), in the momentum-pseudorapidity plane, for separating e/π (left), K/p (center) , and π/K (right) in the barrel and forward regions.

this stage of development, the currently designed detectors could offer valuable experimental information in physics projects.

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4 Pixelated resistive MicroMegas for high-rates environment

The new era of Particle Physics experiments is moving towards new upgrades of present accelerators (Large Hadron Collider at CERN) and the design of high energy (tens/hundreds TeV scale) and very high intensity new particle accelerators (FCC-ee/hh, EIC, Muon Collider). Cost effective, high efficiency particle detection in a high background and high radiation environment is fundamental to accomplish their physics program. We present a new High Granularity Resistive Micromegas detector capable to ensure full efficient and stable operation and a good tracking capabilities up to particle fluxes of 10 MHz/cm^2.

4.1 Introduction

Micro Patterns Gaseous Detectors (MPGDs) will play a crucial role in the next future of High Energy Physics, when the intensity frontier will be moved over. Resistive Micromegas (R-MM) are built with parallel plate electrodes structure, with the volume divided into two gaps (drift and amplification) by means of a metallic mesh. The anode plane hosts the read-out elements, usually strips, built using Printed Circuit techniques. To prevent discharges that could damage the detector and worsen its performances, a layer of resistive strips facing the amplification gap is added. [1]. This is, for example, the solution adopted by ATLAS for the New Small Wheel upgrade, for operations up to few kHz/cm^2 [2]. Since 2015, our research team is working to a further development of the MM technology to reach stable and efficient operation up to particle fluxes of tens of MHz/cm^2, with low occupancy and good stability and robustness, and ensuring good tracking capabilities. To achieve these performances we designed a higher granularity detector using few mm^2 large readout pads instead of strips. This choice significantly reduces the occupancy of the readout elements, but the resistive structure required for the spark protection needs to be optimized to avoid losing efficiency at very high rates. In this paper we are going to report the status of our R&D project and a summary of the performances measured along last years by mean of high intensity X-ray, muon and pion sources.

4.2 High granularity MicroMegas for high-rate environments

The main idea that underlies our detector design is to reduce its occupancy in order to fulfill the requirement on the rate capability: this can be achieved designing a resistive Micromegas with small enough readout electrodes. At the same time, the resistive scheme has to guarantee a time stable operation (spark suppression) and fast charge evacuation at high particle rate. We have built and tested many high granularity Resistive Micromegas using different resistive schemes, in order to try different technologies and exploit all the advantages of the different techniques that have been used. All detectors presented in this paper share the same anode plane, segmented with a matrix of 48×16 readout pads. Each pad has a rectangular shape (0.8×2.8 mm^2) with a pitch of 1 and 3 mm in the two coordinates. The active surface is 4.8×4.8 cm^2 with a total number of 768 channels and a density of about 33 readout elements per cm^2, routed off-detector for next signal processing

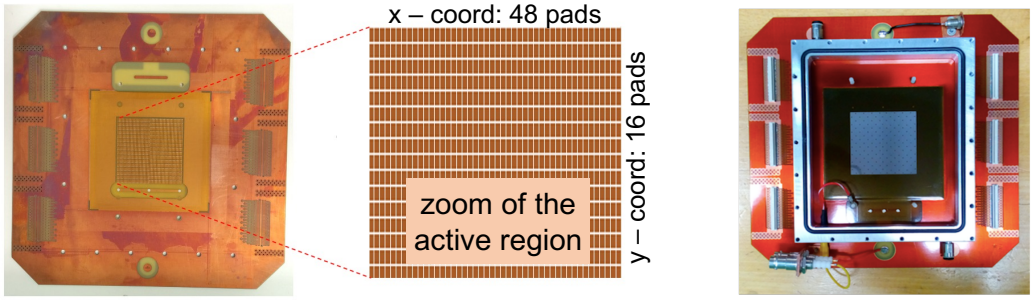

Figure 6: Picture of the detector anode plane (left) with an expanded view of the pad structure (center). Right: picture of the detector after the *bulk* process with the frame defining the gas enclosure; readout connectors are clearly visible at the border.

stages. The readout connectors are hosted on the border of the detectors where the front-end electronics is plugged-in. Figure 6 shows a picture of the anode plane. A resistive layers is put on top of this anode plane to act as a spark protection system. Different concepts of resistive layers have been implemented and will be discussed in this section. All MM detectors are assembled using the *bulk* Micromegas process [3], defining the 128 μm wide amplification gap with a metallic micro-mesh woven using stainless steel wires having a diameter of 18 μm and a pitch of 45 μm. The mesh is supported by cylindrical insulating pillars with a diameter of 300 μm and an height of 128 μm (unless differently stated), The detector is completed using a copper cathode to define the 5 mm wide conversion and drift gap.

4.3 Resistive protection layer: different approaches

The resistive layout is a crucial element of our Micromegas detectors. The detector performances have a strong dependence on its characteristics. We have implemented and studied several concepts of the spark protection resistive layers. Two main schemes can be defined, even if some hybrid solution have been exploited. In the following we describe all the resistive layouts that have been built and tested, sorting them from oldest to newest one.

Pad-Patterned embedded resistors layout (PAD-P)

The first proposed detector [8] presents a pad-patterned (PAD-P) resistive layer, where each readout pad is overlaid by a resistive pad, both interconnected by intermediate resistors embedded in the structure. It has been inspired by a similar development considered for the COMPASS experiment [4, 5]. A schematic view of the layout is reported in figure Figure 7 (left). It consists in stacking over each copper readout pad other two resistive pads (screen printed with a suitable resistive paste) interspersed with an insulating kapton layer; the outermost pad (facing the gas gap), the middle one and the innermost pad (the metallic one) are all electrically through staggered connection vias made by micro-holes

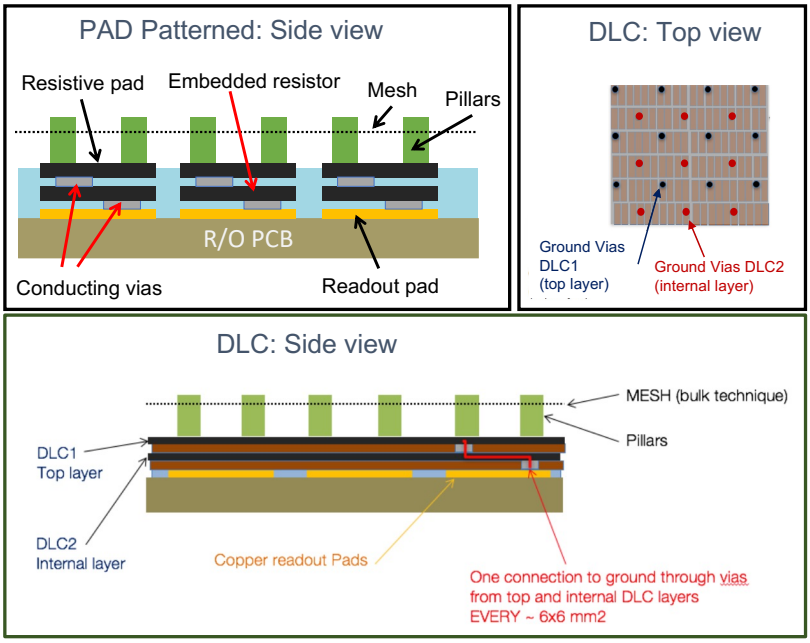

Figure 7: Sketch of the pad-patterned embedded resistor layout (top left) and of the Diamond-Like Carbon layout (top right and bottom).

filled with silver paste. With this solution middle pad acts as a resistor, totally separated from the neighbors, whose value ranges between 5-7 MΩ, depending on the paste resistivity; moreover an almost uniform resistance to the anode pads is guaranteed, independently from the impact position of the electron avalanche on the innermost layer.

Diamond-Like Carbon (DLC) layout

The second technique used to obtain the resistive coverage of the readout elements is referred in this paper as "DLC" and takes its name from the use of the Diamond Like Carbon surface treatment. It has been inspired to the technique used for the μ-RWELL detector [**?**]. This consists in sputtering carbon (evaporated from a graphite target) on a kapton foil, obtaining a uniform resistive layer. As shown in fig. 7 (right), two DLC foils are then interconnected through staggered conductive vias, providing the charge evacuation through their resistive surface. The pitch of the conductive vias network represents a relevant parameter of the detector, as long as the surface resistivity of the DLC foils. For this reason two prototypes have been built and tested with this technique using different resistivity: the first one with average resistivity of about 50 MΩ/□, and the other with foils with about 20 MΩ/□ referred to as DLC50 and DLC20, respectively. Moreover for both detectors, the active plane has been divided in two halves for testing purposes, with a different pitch of the conducting vias through the DLC layers: 6 mm and 12 mm respectively. In order to distinguish these two regions, the suffixes "$-6mm$" and "$-12mm$" are added to the corresponding name.

DLC with the sequential build-up technique (SBU)

In order to further improve the precision of the construction process, a new technological solution for the production of the resistive layers has been introduced making use of copper clad DLC foils. This technique has been named Sequential Build Up (SBU) [9] and it uses photolithography to precisely locate the conductive vias and align them below the pillars as shown in Figure 8 right in comparison with a misaligned via-pillar pair observed in one of the first standard DLC prototypes (Figure 8 left). Detectors produced with SBU technique are quite similar to standard double DLC detectors but they have a better stability because avoiding conducting surface exposed to amplification region can prevent discharges. Moreover this solution is much more convenient than the simple double DLC process described before because this building technique is is fully compatible with standard PCB processes, significantly facilitating the technological transfer of the production. Three prototypes have been built with the SBU technique, referred in the following sections as SBU1, SBU2 and SBU3. All of them, have been built using a configuration with the 6 mm pitch grounding vias is adopted in the full area. The first two detectors were built with a $\sim$5 M$\Omega/\square$ resistive layer facing the amplification region and an innermost layer with a resistivity of $\sim$35 M$\Omega/\square$. The third prototype, SBU3, has both DLC foils with a mean surface resistivity of about 30 M$\Omega/\square$.

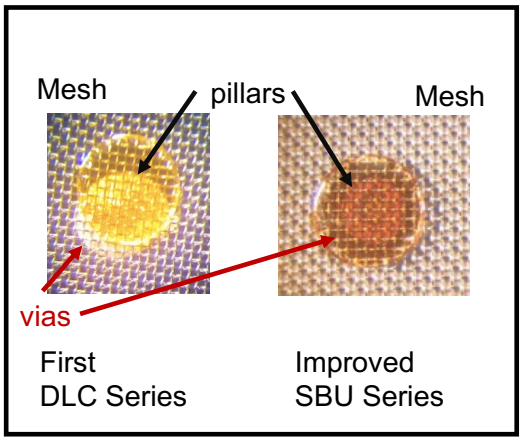

Figure 8: Left: example of pillar (uppermost yellow circle) in DLC20/50 prototypes, not well centered with the conductive vias. The mesh layer can also be seen. Right: example of good alignment between pillar and conduction vias in SBU prototypes.

Hybrid layout (PAD-H)

This fourth kind of detector can be considered a technological improvement of the Pad-Patterned embedded resistors layout. This configuration uses a uniform DLC layer for the inner layer and screen-printed resistive pads for the outer layer. Differently from the DLC and the SBU schemes, in the PAD-H configuration the carbon layer of the DLC foil is patterned in pads by means of a proper etching procedure. The schematic cross-section of the detector is shown in Figure 9 top, with the indication of the components of the stack. The size of the DLC pads can be equal to the one of the screen-printed pads to maximize the number of charge evacuation paths, or to a multiple of them to simplify the

construction at the cost of longer evacuation paths. In our prototype we opted for the first solution, leading to the same connection scheme, between the inner and the outer layers, of the PAD-P detectors.

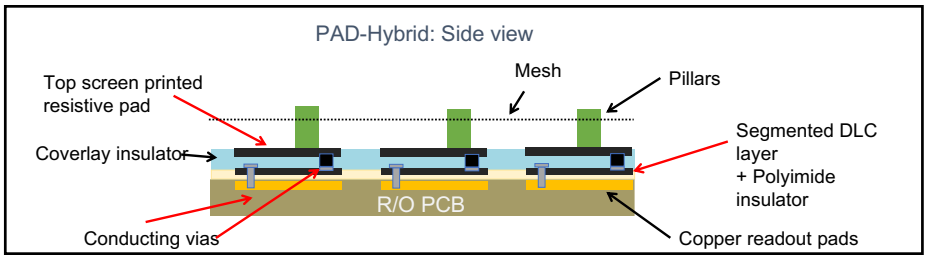

Figure 9: Schematic view of the PAD-H prototype.

DLC-Strip layout

The latest prototype that has been built is really quite different from the previous ones because of many changes in the design of both resistive protection and signal formation. The main feature of this detector is that the readout pads are located in-between the two resistive layers in order to improve the capacitive coupling for signal induction. As shown in Figure 10 bottom, the resistive layers are obtained using a uniform DLC foil at the outer part and a segmented DLC one at the innermost. The segmentation is obtained with a proper etching as for the inner layer of PAD-H detector. Another important change with respect to the former prototypes is that metal connection strips are used to connect each other the DLC layers, for this reason we will refer to this design scheme as DLC-Strip layout. The reason for this solution lies in the fact that metallic connections provide a much more reliable solution for charge evacuation than conductive vias obtained with a silver-loaded polymer. Also in this case, to avoid the development of intense discharges top surface of these metallic connections must be completely insulated by the gas gap, and that is obtained as usual by covering the exposed conductive material with pillars. Anyway in this case they need to be elongated to a length of 5 mm, as shown in Figure 9 bottom right, thus reducing the geometrical acceptance of the detector.

4.4 Detector characterization and performance studies with different gas mixtures

All the detectors have been characterized and extensively tested in order to measure their performance in terms of charge up behavior, gain, rate capability, energy resolution, efficiency and spatial resolution and detector stability. Measurements using radioactive sources (^{55}Fe), and 8 keV photons from a Cu X-rays gun have been performed at the GDD (Gas Detector Development) laboratory of the RD51 [13] Collaboration at CERN. Spatial resolution has been measured in dedicated test beam activities at CERN beam lines, using high energy muon and pions, looking at residuals distribution with respect an external tracking system. More irradiation tests have been performed at PSI using intense pion beams and

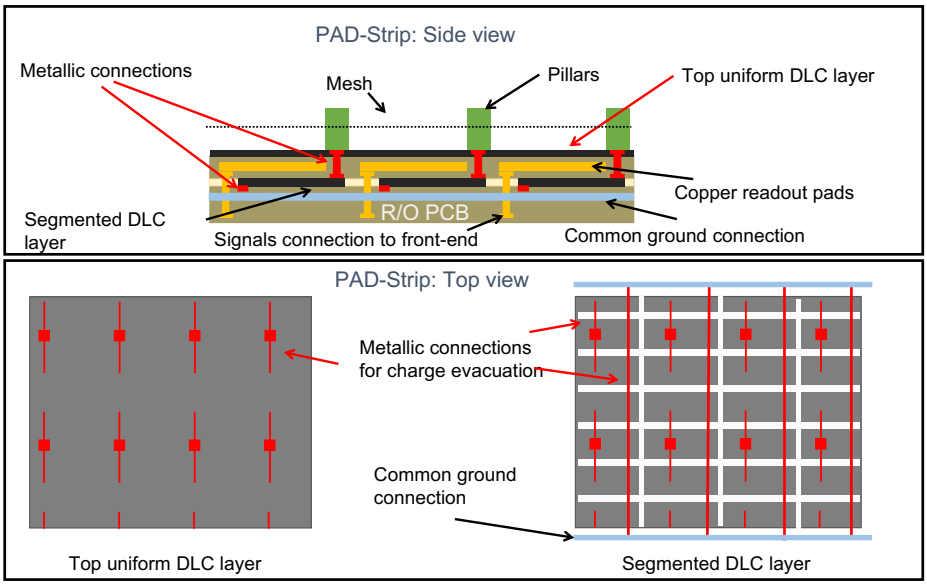

Figure 10: Schematic view DLC-Strip detector. The bottom plot shows the layout of the metallic connection on both resistive layers and the necessity to cover them with elongated pillars.

at CERN in GIF++ facility [15]. Two kind of gas mixtures have been tested: the binary Ar:CO_2 gas mixture (93:7) as a standard reference, and a ternary mixture Ar:CO_2:iC_4H_{10} (93:5:2), at a gas flow of few renewal per hour, for a typical gas volume of 0.2 l. A nominal electric field in the drift region of 60 V/mm has been used as a reference for all measurement, unless differently state, thus optimizing the mesh electron transparency.

In this section a summary of the most relevant results is reported: a complete and detailed review of them can be found in [8, 9, 11, 10].

4.5 Gain, Charging up effect and rate capability

Detector gain has been measured using different methods, depending on the range of the rate of incoming radiation seen by the detector. Al low rate (below few hundreds kHz, when detector is exposed to ^{55}Fe source or to 8 keV X-Rays) the detector current is measured from readout pads with a pico-ammeter and signal rate from the mesh is counted directly or through a MultiChannel Analyzer (MCA). Figure 11 right shows the gas gain as function of the amplification voltage of a PAD-P, a DLC and two SBU detectors. DLC and SBU, which both have an external uniform DLC resistive layer, show the same gain, thus demonstrating the high level of uniformity reached in the production process. The PAD-P detector shows a lower gain, by about a factor 2, only partially justified by the larger charge-up. The main difference is attributed to the different field configuration as consequence of the different layout of the external resistive layers. The same difference was observed comparing the

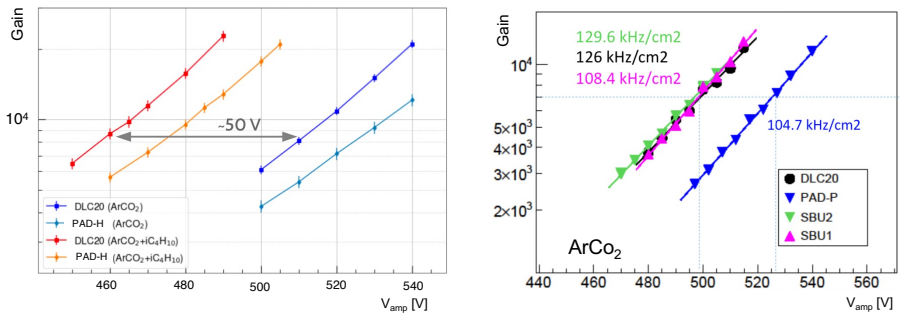

Figure 11: Gain vs amplification voltage for PAD-H and DLC detectors in Ar:CO_2 and Ar:CO_2:iC_4H_{10} (left) and for PAD-P, DLC and SBU detectors in Ar:CO_2 (right).

DLC20 detector with the PAD-H, as shown in Figure 11 left. In the same plot are also reported gain curves of the two detectors measured with the Ar:CO_2:iC_4H_{10} mixture in the fraction 93:5:2. The introduction of 2% of isobutane lead to a gain increase of a factor about 4 with respect to the Ar:CO_2 mixture, owing to the higher Penning transfer. It has been observed that adding isobutane drastically reduce the intensity of discharges, thus ensuring a much stable operation working point. The mixture with the addition of 2% of isobutane allows then to operate the detector at lower voltage to reach the same gain.

At higher rate values, which can be reached using the X-rays gun exploiting the full range of the current flowing in its filament, a direct measurement of the detector rate is no longer reliable due to events pile-up: then, for this reason, detector rate has been estimated using an extrapolation at higher current values in the linear relation between detector response and incoming flux of particles. This relation has been verified over two orders of magnitude and it's shown in figure 12: measured points have a relative uncertainty less than 2% with respect the extrapolation taken at very low value of incoming radiation and they are within the 95% CL prediction over the exploited range up to 200 kHz. At even higher values, up to several tens of MHz, any other deviation from this linear behavior is then attributed to a detector gain loss.

The variation of the gain in MPGD when exposed to intense radiation fluxes is a well known effect and has been observed by many authors [16, 17]. This phenomenon is due to to the charging up of the dielectric material in the detector structure and it can produce either an increase or a reduction of the gain, depending on the field configuration: both effects can be present in the same structure although with different time scales. We have measured a different behavior of the detectors with the upper resistive layer segmented in pads (like the PAD-P series) with respect to detectors with an uniform DLC layer. (as the DLC and SBU series).

As shown in Figure 13, the current as function of the time has been recorded for a PAD-P and a DLC detectors, when irradiated with X-rays, changing the irradiation rate in a range few MHz/cm^2 by discrete steps. The PAD-P detector shows a fast gain reduction of the order of 15-20% within a time scale of few seconds, and we can interpret this result

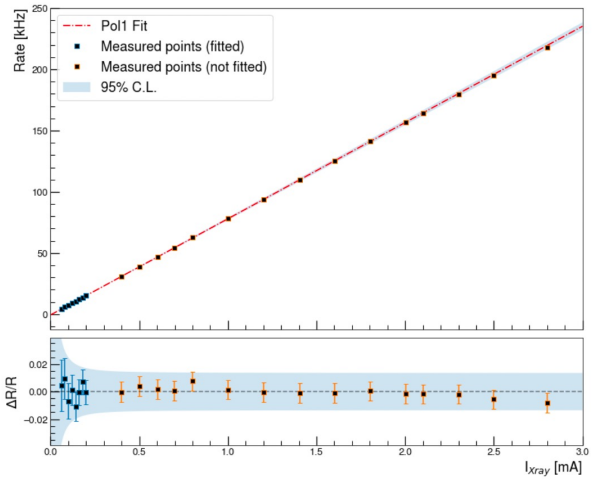

Figure 12: PAD-H detector response as function of the current of the X-ray gun: the detector shows an excellent linear behavior up to 200 kHz.

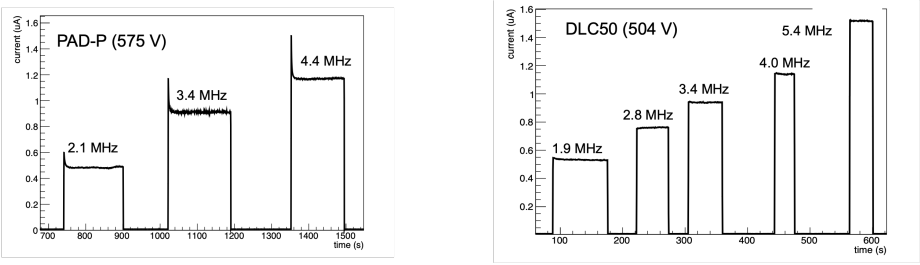

Figure 13: Charge up for the PAD-P (left) and the DLC (right) detectors irradiated with X-rays.

as an effect due to the charging-up of the exposed dielectric surface. This effect is almost negligible at the same short time scale for detectors presenting an uniform resistive DLC layer facing the gas amplification region (DLC and SBU series), with a gain reduction of less than few percent PAD-H detectors showed a charging up effect similar to the PAD-P series. The opposite effect was observed during long-term (about 10 h) irradiation with high intensity pion beam at PSI. Results are shown in Figure 14 left: after a short initial period when the PAD-P detector suffers a decrease of the current, differently from the others, all the detectors show an increase of the current in the long run. Figure 14 right illustrates the peculiar behavior of the DLC-Strip prototype: it presents no detectable gain drop at short time scale, as all the prototypes with a top uniform resistive layer (DLC and SBU series) but it shows a gain increase of $\sim 3\%$ in few minutes even at an hit rate of about few hundreds of kHz/cm^2 under X-ray irradiation.

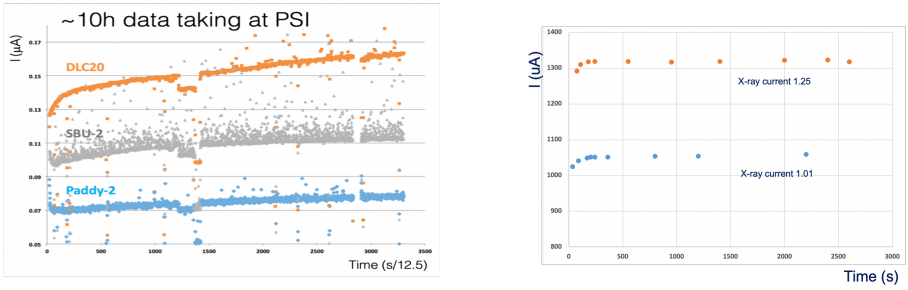

Figure 14: Charge up for the PAD-P, DLC and SBU at PSI pion beam (left) and of the DLC-Strip (right) irradiated with X-rays.

To assess the rate capability of the detectors, their gain has been measured over a wide range using Cu target X-rays. Figure 15 reports the gain of the PAD-P and DLC-20 detectors in the range from few kHz/cm^2 up to 30 MHz/cm^2 for different values of the amplification voltage. As already stated in the previous section, the pad patterned prototype shows a significant gain drop at lower rates (below 5 MHz/cm^2) dominated by charging up effect, up to about 20% at 10 MHz/cm^2 at 530 V, while it has a negligible ohmic voltage drop in range of rates from 10 to 30 MHz/cm^2. On the contrary, the DLC-20 detector shows an almost constant gain in the range below few MHz/cm^2 and than, at higher values, a significant ohmic voltage drop, with a relative drop of about 20% at 20 MHz/cm^2 at 510 V. This behavior is common to all the DLC series detectors, including the SBU type; moreover the detectors with uniform resistive layer have systematically a gain higher than PAD-P (at low/moderate rates) for the same value of the amplification voltage: this is due to a more uniform electric field in the amplification gap with respect to PAD-P. For this reason, we usually operated the two kind of detectors at a sligtly different voltage values, in order to keep them at the same gain values when comparing their performances.

Figure 16 left reports a comparison between the different types of detectors: relative gain loss of PAD-P, DLC and SBU prototypes has been measured as a function of the hit rates in the range 1-100 MHz/cm^2. As previously mentioned, the different behavior of the PAD-P prototype is evident: its gain drop is dominated by the charge up, increasing with

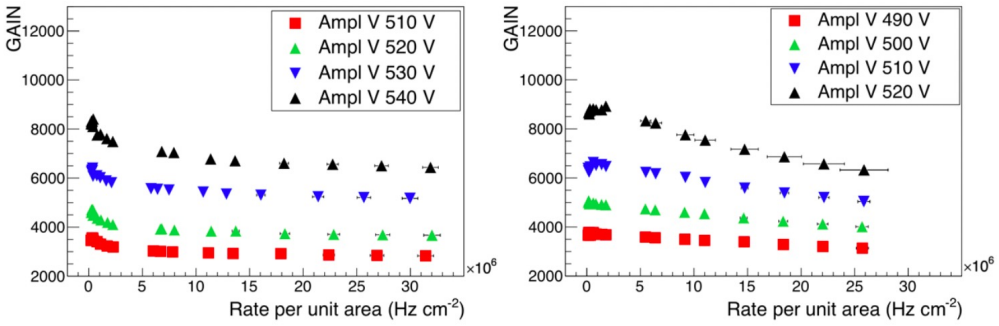

Figure 15: Gain of the PAD-P (left) and DLC20-6mm (right) in the range of rates up to 30 MHz/cm^2 for different values of the amplification voltage, measured with X-rays.

the rates and almost saturating at 20 MHz/cm^2, where the gain drops by about 20%. With a current larger than 0.5 μA per pad, the voltage ohmic drop is contributing only for very high rates, up to a total gain drop of about 30% at 100 MHz/cm^2. Instead, all the detectors belonging to DLC or SBU series have the same behavior at rates above few MHz/cm^2 , but it dramatically depends on the value of the surface resistivity: the DLC50 prototype is more severely affected by the ohmic voltage drop and the gain is significantly reduced, as expected because of its higher resistivity. Moreover the configuration with 6 mm pitch grounding vias has a more reduced gain loss with respect to the 12 mm configuration, because there the charge sees a much higher impedance to ground. The DLC20-6mm and SBU2 detectors, which share the same configuration and have a quite similar value of the DLC surface resistivity show a similar behavior at high rates, with a gain drop similar to PAD-P at about 20 MHz/cm^2, further reduced up to about 50% at 100 MHz/cm^2.

In the same picture, but on the right side, there is the gain drop of PAD-H and DLC20 detectors, reported as a function of the hit rates and normalized to their value at low rates, in the range from few kHz/cm^2 up to few tens of MHz/cm^2. Data have been taken irradiating detectors with X-Rays almost uniformly in a circular area of 0.79 cm^2 and operating them approximately at the same gain. Even in this case, the two detectors show a quite different response to the increase of the rate. PAD-H undergoes a rapid loss of gain even at few kHz, with an apparent exponential drop of $\sim$25% within two orders of magnitude. The behavior of this detector confirms what has been measured for other pad patterned detectors and seems to be largely dominated by the charging-up. Anyway it can operate with still significant gain even at very high rates. Instead, the prototype with the DLC uniform layer resistive scheme shows constant performances for an extended range of rates. It shows variations of the gain smaller than 10% up to few MHz/cm^2 of incident radiation.

The performances in rate capability can be enhanced operating the detector with isobutane enriched Ar:CO_2:iC_4H_{10} (93:5:2) gas mixture. As previously noted, (see figure 11) this ternary mixture leads to a gain increase of a factor about 4 with respect the binary Ar:CO_2 (93:7) gas mixture thus allowing to stable operate the detectors with gain above

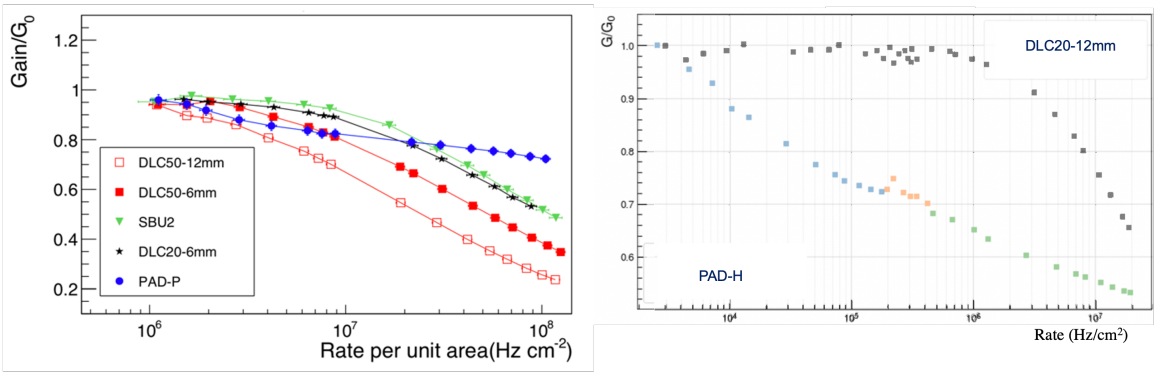

Figure 16: Left: Dependence of the gain of the PAD-P, DLC and SBU detectors, normalized to their value at low rates, as a function of the X-Rays hit rates. The amplification voltage was set to have a gain about 6500 at 100 kHz/cm^2 for all the detectors. Right: direct comparison between the PAD-H and DLC20 detectors operated at approximately the same initial gain.

10^4 up to extremely high rates of the order of 10MHz/cm^2 and more. Results are reported in figure 17.

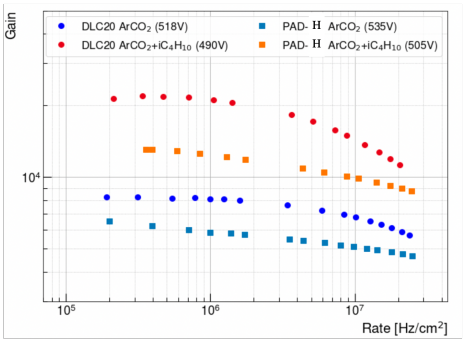

Figure 17: Gain as function of the hit rate for the DLC20 and PAD-H detectors operated with Ar:CO_2 (93:7) and Ar:CO_2:iC_4H_{10} (93:5:2) gas mixtures.

4.6 Energy resolution

The energy resolution (as measured by 5.9 keV ^{55}Fe X-rays) has been obtained by measuring the energy spectra of the detector response with a multi-channel analyser (MCA). Figure 18 shows a typical result obtained for PAD-P (left) and DLC (right) detectors. Energy resolution is in the range of 40-50% FWHM/mean for the PAD-P series, while has been significantly improved with the DLC scheme (FWHM/mean $< 30\%$), thanks to a more uniform electric field in the amplification region assured by the smooth surface of the carbon layer while the pad-patterned layout of the other detector produces strong variations of the

electric field along the border of the resistive pads, thus getting the energy resolution worse.

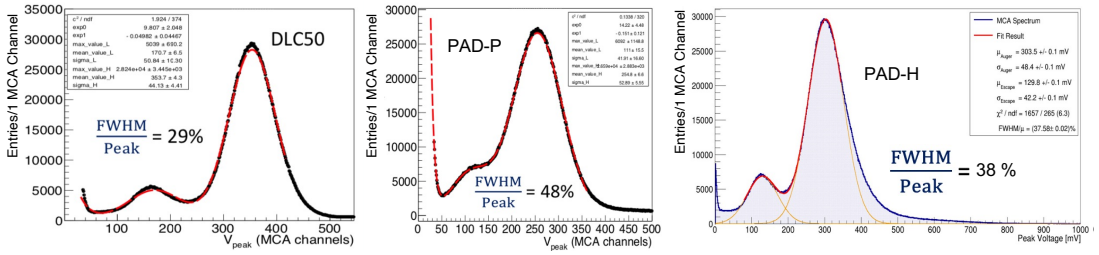

Figure 18: Energy spectra of γs from an ^{55}Fe source for the PAD-P (left) and the DLC (right) detectors. The main peak of each distribution is fitted with a gaussian and the energy resolution is computed as FWHM/peak value, as indicated in the figures.

4.7 Efficiency and spatial resolution

The spatial resolution and efficiency of the detectors have been measured during several test beam campaigns with particle beams at the CERN SPS H4 line and at PSI, and with muon at the CERN GIF++ facility [15] where a muon beam is available together with 662 keV photon background from a ^{137}Cs source of 16.6 TBq activity. Two resistive strips Micromegas with double coordinate readout have been used as tracking system with prototypes under test in between; events were triggered by two small scintillator counters. Detector signals have been acquired with APV25 hybrids read out with the SRS system [14]. All the presented results have been obtained with muon or pion beams perpendicular to the detector surface.

Figure 19 left shows the efficiency as function of the amplification voltage measured for the PAD-P detector. The efficiency is computed with three difference cuts when looking to the position of a reconstructed cluster with respect to the extrapolated muon track: cluster efficiency (the cluster is anywhere in the detector active area); software efficiency (the cluster is within 1.5 mm of the extrapolated reference track in the precision coordinate); 5σ efficiency (the cluster is within 5σ, about 1 mm, of the extrapolated reference track in the precision coordinate). In the right side of the same picture, the plateau efficiency of the PAD-P detector is measured as a function of the pion beam rate. Results confirm that even with the most stringent requirement, the detector efficiency is well above 98%. It is worth to note that for this chamber the pillars cover about 2.8 % of the active area surface.

Figure 20 shows the residual distribution of the reconstructed cluster position on the PAD-P detector under test and the extrapolated track position measured with an external tracker. The cluster position is obtained as the charge weighted centroid of the fired pads that pass minimal quality cuts, used to clean up the signals from front-end electronic noise. The spatial resolution measured with CERN pion beam in the precise coordinate (x, with pad size of 0.8 mm and a pitch of 1 mm) is 190 μm. In the second coordinate (y with a pad readout pitch of 3 mm) the residual quite uniformly distributed with a FWHM of about

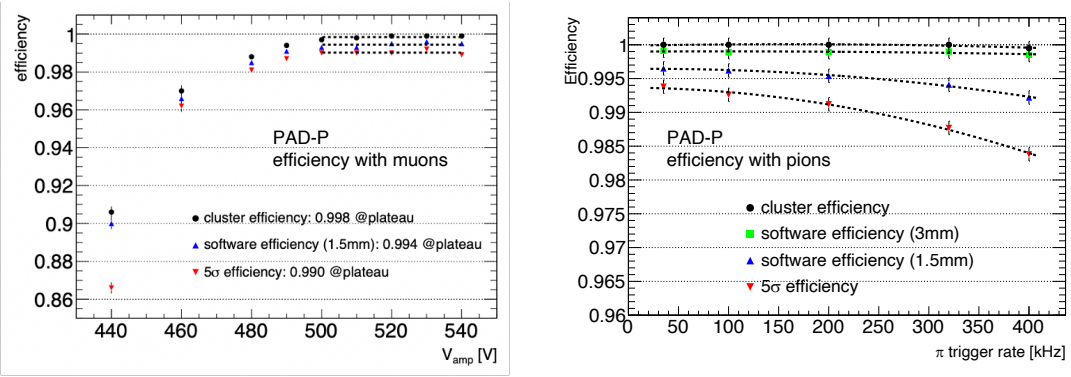

Figure 19: Left: PAD-P efficiency vs Amplification voltage, as measured with a high energy muon beam. Right: PAD-P efficiency vs pion beam rate.

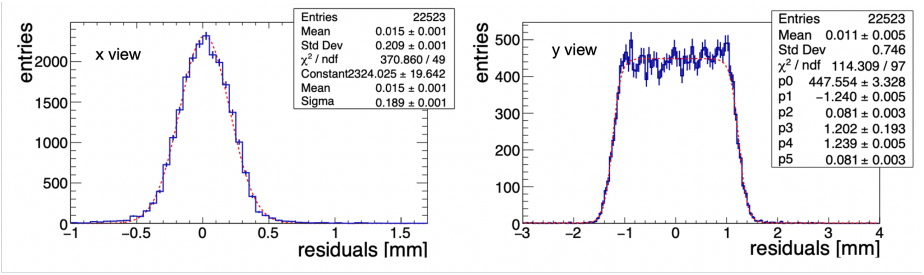

Figure 20: Distribution of the residuals between the reconstructed cluster position on the PAD-P detector and the extrapolated track position measured with an external tracker, for the x- (left) and y-coordinate (right).

2.4 mm, as expected from the large pad size which gives a reconstructed 2D cluster that is only one pad in y-coordinate wide.

The main parameters affecting the spatial resolution are the readout pad dimension, equal for all the detectors, and the configuration of the resistive layer. The latter affects the size of the induced signal. In detector with uniform layers (DLC, SBU) the induced signal spreads over more pads, leading to larger average dimension of the reconstructed cluster and a more precise centroid reconstruction. A lower resistivity of the external carbon layer goes in the same direction. All that is shown in Figure 21 where the cluster size (left) and the spatial resolution (right) are shown as function of the amplification voltage for the PAD-P, DLC20 and DLC50 detectors. As expected PAD-P, with segmented resistive pad in the external layer, has smaller cluster dimensions and correspondingly a slightly worst spatial resolution, while the DLC detectors show a larger cluster size and a spatial resolution better than 100 μm in the x-coordinate. In the comparison between the two DLC detectors, DLC20 behaves slightly better in terms of spatial resolution because of its smaller surface resistivity.

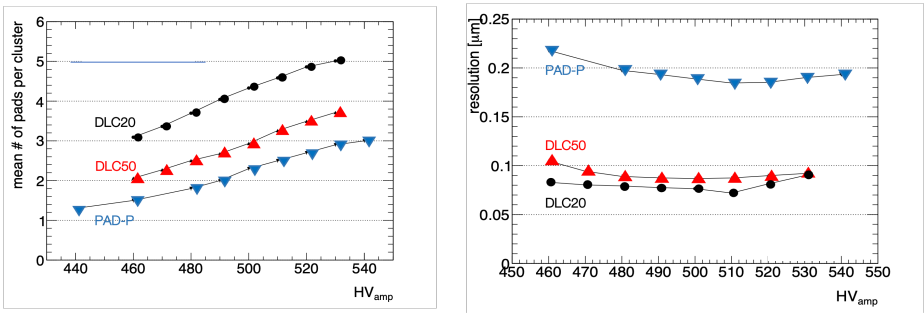

Figure 21: Cluster dimension (left) and spatial resolution (right) for the PAD-P, DLC20 and DLC50 detectors measured with pion beam at the CERN SPS.

Figure 22 reports preliminary results of the fall 2021 test beam campaign, showing the spatial resolution of PAD-H, the DLC-Strip, SBU3 and the DLC20 detectors. The top left plot shows the spatial resolution as function of the amplification voltage: as expected the DLC detector with uniform layer of lowest resistivity (DLC20) has a resolution of about 80 μm, in agreement with older measurements, while the pad-patterned device (PAD-H) shows a resolution of about 200 μm, that is compatible with PAD-P resolution. The spatial resolution was also measured with increasing photon background. Results are shown in Figure 22 top right where the x-axis reports the status of the GIF++ gamma source: Off means that during the measurement no photon flux was present; Attenuation=1 means full source, corresponding to approximately few tens of kHz/cm^2; Attenuation=22 means that the measurement was performed with a set of absorbers in front of the GIF++ source providing a total photon flux reduced by about a factor 22 with respect to Attenuation=1. No degradation of the tracking performance have been observed for any of the tested detectors for the full range of the GIF++ photon flux. This result confirms, once more, the suitability of these detector as tracking devices in conditions with high background. The bottom plot shows the same detectors tested few weeks later using muon beam in H4 experimental area @ CERN. Results are fully compatible with the previous ones, thus demonstrating the stability of detector performances in different experimental conditions.

4.8 Detector stability

Finally, with the high intensity pion beam of 350 MeV/c energy at the PSI, we have measured the spark probability of several of our detectors. Figure 23 left shows the detector current trend for particle rate of about 100 kHz/cm^2. Some discharges (seen as high current peaks) are visible, more frequently on one of the two SBU-type detectors. The right part of the plot shows the spark probability as function of the amplification HV for the PAD-P, DLC-20 and two SBU detectors. PAD-P shows a very high stability with a spark probability $<2\times10^{-9}$/pion/cm^2. DLC20 shows better stability of the two SBU, explained by the lower resistivity of the external resistive layer for the latter.

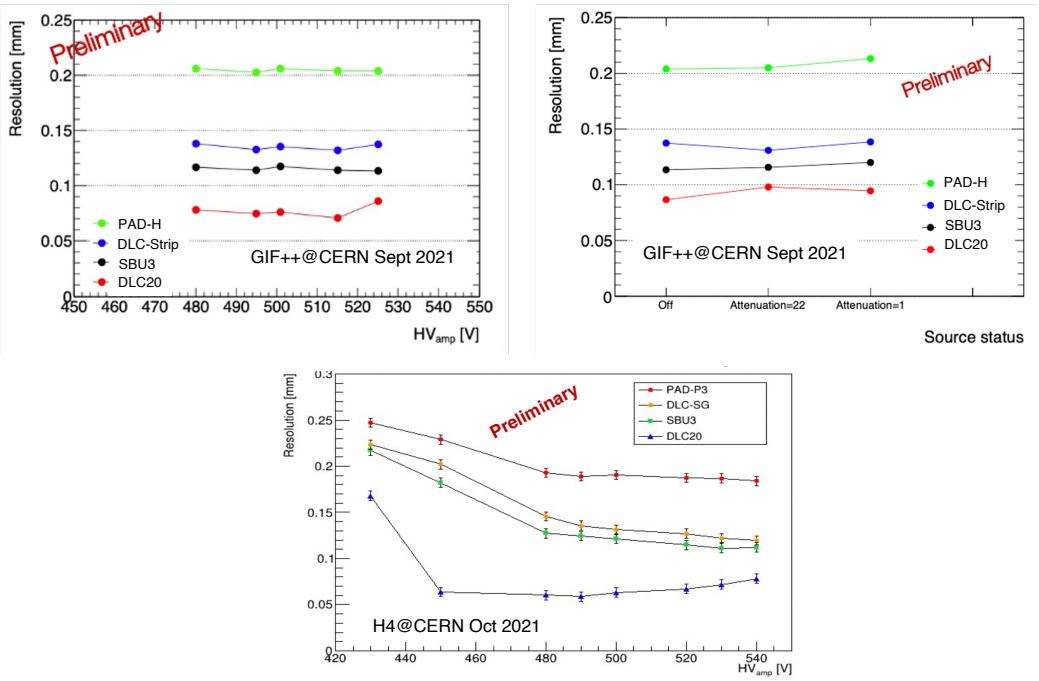

Figure 22: Top: Spatial resolution measured at the GIF++ facility at CERN as function of the amplification voltage (left) and of the ^{137}Cs source status (right), for the PAD-H, DLC20, DLC-Strip and SBU detectors. Bottom: Spatial resolution measured at H4 at CERN with muon beam as function of the amplification voltage.

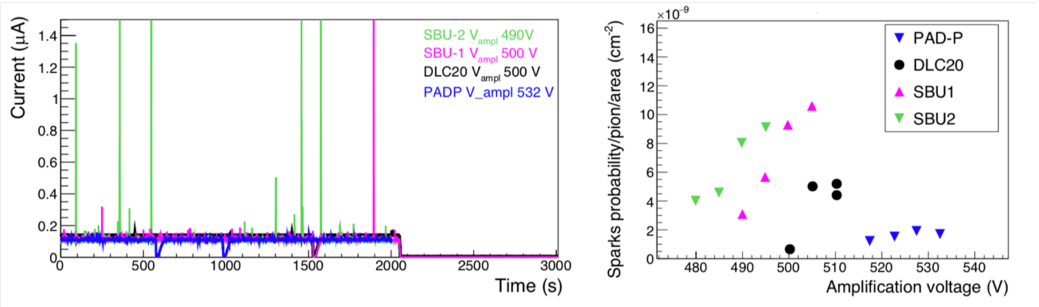

Figure 23: Detector stability with a pion beam of 350 MeV/c. Left: current as a function of time under a particle rate of about 100 kHz/cm^2. Right: spark probability density per pion.

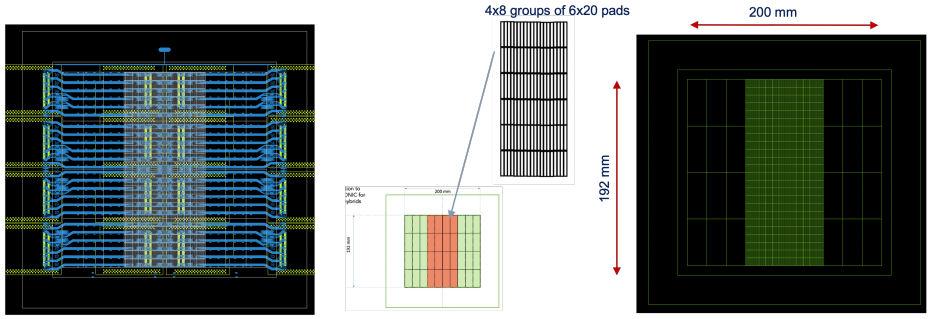

Figure 24: Schematic of the large-size demonstrator under construction. The figure includes the zoom showing the readout pad layout.

4.9 Towards large size detector: experience and future developments

The detectors that have been developed fulfil the requirements on rate capability needed by a gaseous detector in order to be employed in environments where high particle rates are expected and good tracking performance and reliable operations are needed. The performance have been studied so far on detectors with an active surface limited to 48×48 mm^2 but several possible applications of such devices will require larger detector surface. For these reasons we are building a demonstrator with an active area of 192×200 mm^2 with 4800 readout pads with a pitch of 1×8 mm^2 based on the SBU technology. The schematic layout of the large detector is shown in Figure 24.

While proceeding with the detector R&D (looking for the best resistive/readout pad patterns, pads resistivity, etc.) we are also exploring the possibility of integrate into the detector its readout electronics, embedding it on the back of the MicroMegas PCB. Since in our present prototype most of the PCB space is occupied by the pads routing, limiting the scalability of the board to larger sizes, this modification will allow to overcome this problem. A small prototype with APV25 chip for the readout has been produced at the CERN MPT workshop. It has been made of four regions having 128 pads each, matching the APV25 chip channels capability. Pads pitches will be 1x8 mm2 in three sections, and 1x3 mm2 in the fourth one, for comparison with the previous prototype. Fig. 25 shows front and back views of the PCB with the chips associated circuitry, We have performed first tests with APV chips, obtaining encouraging results. Anyway, the work on this direction is still in progress. The next step, after the electronics integration, will be the cooling integration if chips requiring continuous cooling has to be used. The idea here is to include a micro-channel cooling loop inside the base-plane material of the detector to have a compact and highly integrated detector system which includes the sensitive device and the electronics with its cooling.

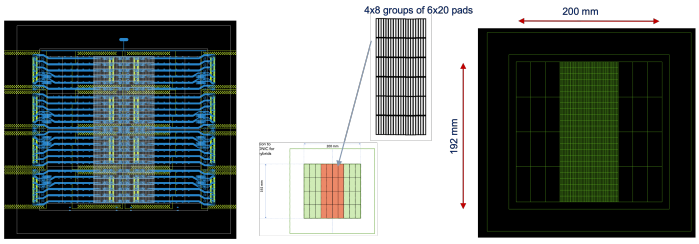

Figure 25: Top and bottom right: pictures of the first implementation of the PAD detector with integrated electronics. Bottom left: representation of a signal induced by a photon form a ^{55}Fe source acquired with the PAD detector with integrated electronics.

4.10 Conclusions and final remarks

This paper report the R&D activity, ongoing since several years, aiming to the development of a new generation of single amplification stage resistive Micromegas. Several detectors have been so far built with different construction techniques and fully characterised with test in laboratory and at beam lines. The developed device, with 3 mm^2 readout pads, can be efficiently operation up to particle fluxes of 10 MHz/cm^2, have an efficiency to charged particles above 98% and a spatial resolution ranging between 80 and 200 μm (depending on the technology) for readout pads with 1 mm wide pitch. The proposed detector can find a suitable application in many fields of particle detection in future experiments, as muon tracking or tagging detector, calorimeters, Time Projection Chamber, central tracker with low material budget, ad other. The R&D of this new technology is still ongoing to consolidate the construction of large-size detectors; to develop a fully integrated system that include the the front-end electronics and the cooling in a single structure; to optimise the performance and the operating conditions to the specific application.

4.11 Acknowledgements

We gratefully acknowledge the CERN MPT workshop (in particular R. de Oliveira and his group, for ideas, discussions and the construction of the detectors), E. Olivieri and the RD51 Collaboration for support with the tests at the Gas Detector Development (GDD) Laboratory and for the test-beam at CERN. The team of the piM1 Beam facility at PSI and GIF++ facility team also deserve our full and heartfelt gratitude for their support during our test beam and irradiation activities.

We would like to thank the organizers of Snowmass 2021 (US Community Study on the Future of Particle Physics) and in particular the conveners of the white paper 'Recent advances and Current R&D'.

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5 Trigger extensions for the scalable readout system SRS-e

5.1 SRS-e extended Scalable Readout System

SRS is a widely used readout system [citation1] for low- to high channel-count, gas or photon detectors of type MPGD [citation2] or SiPM [citation3]. "SRS classic" was designed for scalability from desktop systems to rack-sized readout systems running under the same Online DAQ and Control system [citation4]. The new, extended SRS-e paradigm adds realtime trigger functionality, deep trigger pipelines and a generalized frontend link via the new eFEC concentrator backend. Horizontal links synchronize clocks and realtime actions, and the vertical links can be connected within vertical or horizontal readout architectures. Compared to SRS classic, where crate-based FEC cards concentrate 8 frontend links each, the eFEC doubles the frontend links to 16, enhances the output bandwidth to 20 Gbps and includes an 80W subsystem to power for the frontend. A single eFEC concentrates 16 links to readout ASICs which are integrated on hybrid frontend carriers, generally named hybrids. Large SRSe systems are stacks of eFEC's powered in SRS crates connected to detector-resident hybrids. The default vertical link protocol is DTCC for Data, Trigger, Clock and Controls, implemented over physical HDMI cables for transmission of 32- or 64-channels per ASIC over 2 or 4 LVDS links. An Ultrascale+ FPGA in the eFEC decodes and stores up to 45 μs of event data in its embedded 18 kbit BRAM pipelines, allowing in parallel for realtime trigger algorithms to qualify event significances and to format events before transmission to two output links per eFEC. Firmware and DAQ software will get bootstrapped from the classic SRS system which is in full production and has been fully tested up to high rates and multichannel testbeam testups [citation VMM HR, VMM XR] with the default VMM3a [citation VMM] frontend hybrids. Open for integration of a wider variety of upcoming frontend technologies [citation RD51 Workshop 2021], the generalized eFEC frontend interface can be configured via firmware to operate with readout protocols at up to 3 Gbps over 4 $\times$ LVDS lines.

5.2 eFEC extended Frontend Concentrator

eFEC is an acronym for **e**xtended Front-End Concentrator. Apart from the SRS crates and optional CTF clock fanout, eFECs are the only modules required for an SRSe readout backend. The Online system gets connected via network fibers or cables with 2 10GBE uplinks per eFEC. The choice of the frontend ASICs is in principle open as long as the corresponding readout data is transmitted in digital format over LVDS links using a protocol like 8b10b. Adapter cards for different types of frontends are not required any more due to the configurable digital link interface. The main functional extension compared to the classic FEC is the realtime trigger functionality which can now get implemented in firmware on the Ultrascale+ FPGA, making use of a vast amount of DSP and programmable logic resources. The trigger algorithms can proceed in parallel to the data pipeline transit time with realtime access to event markers and delimitors. With the default VMM3a fronted [citation VMM frontend], 2k channels are transiting one eFEC pipeline before transmission to the Online system. Firmware will be bootstrapped from the production firmware de-

veloped for 'Assister cards' of ESS [citation FW], accessible in an open-source repository under the condition that newly developed user-firmware gets added to the same repository. The data-driven paradigm of VMM3a-based experiments will be enhanced by use of realtime ART flags (Address in Real Time) [citation ART] as event-framer. Experiments which require an externally generated trigger can connect prompt triggers in the same was as on the classic FEC via a NIM pulse. The eFEC however calls for additional detector-specific firmware algorithms to be developed for detection and selection of event signatures in time and space, or by generation of multiplane-track triggers from hit address combinations. Further examples for online triggers are total energy sums, or charge-over-threshold in space-time regions. Such triggers require extension of the classic SRS slow controls via dedicated Gbit ethernet links connecting to the Online and Control system. The addition of realtime-programmable trigger primitives is on the shelf for project-development by teams, making use of the FPGA-embedded dual-core realtime subunit, which may further get extended to a machine-learning, online trigger concept. Trigger boundaries (2k channels for VMM3a frontends) can be overcome via the horizontal X-link bus connected between eEFC panels connecting neighboring eFEC's in bidirectional, high-bandwidth ring topologies for common trigger regions. The second important extension of SRSe is a generalized frontend link interface, defaulting to the SRS-classic DTCC protocol [citation DTCC] for the VMM3a hybrids, or the SiPM frontend of the NEXT experiment. The new link interface offers 4 individually selectable link directions and firmware-defined protocols. SRSe maintains HDMI link ports on the eFEC rear side, each interfaced via 3Gbps LVDS Rx-TX macros with directional configuration.

5.3 SRS-e extended readout architectures

SRS classic was designed as scalable architecture via incremental addition of independent vertical readout slices, from frontend to backend allowing to bootstrap systems from a minimal number of test channels to final size. SRSe adds the cross-border X-link to the hierarchical architecture and offers the alternative hierarchical architecture. Due to parallelism in the vertical slice architecture, the total bandwidth can achieve very high levels, only limited by the network capabilities of a commercial switch which transmits the concentrated data from 16 frontend links of a single eFEC to online computer(s). Overload of the network can occur in a case of mismatch between the aggregate output data bandwidth and the capacity of the switch or the input bandwidth of the online system. Such overloads are mitigated using zero-suppressed frontend ASICs and by implementation of realtime triggers in the eFECs. Horizontally connected X-link trigger topologies further help to optimize such triggers. The horizontal S-bus serves for common, simultaneous actions at the 25ns level, like Busy, Xon/Xoff, or Reset. The common analogue lines of S-bus allow further to synchronize with external analogue conditions like spill structures or B-fields. The CTF-e common clock module is required for the use of multiple eFECs. It is an extended 'CTF classic' module, synchronizing the eFEC system clocks from either a common external clock source, or from one eFEC used as master clock generator. The clock can be either a local CTF-e clock or an external clock, like the master clock of an accelerator. The hierarchical architecture option of SRSe reproduces implementations like the ALICE EMCal hierarchical

trigger [citation EMCAL hierarchical Trigger] with trigger levels in successive FPGA layers at increasing trigger latencies, requiring additional data buffering at the higher levels. For this purpose, the eFEC can be equipped with DDR4 plugin memory plugin module of up to 64 Gbyte which is directly interfaced to the 64 bit bus of Ultrascale+ FPGA. The output bandwidth of the hierarchical architecture is limited to 2 x 10 Gbps. The X-link, S-bus and CTF clocks links are connected in the same way as for the vertical slice architecture.

5.4 eFEC control and test subsystem

eFECs cards can be equipped with a 32bit SoC plugin mezzanine, including USB and wireless connectivity to external computers. Though in principle the FPGA-embedded 4-core Cortex CPU of the eFEC has Monitoring access to all hardware resources, the external SoC card with its embedded uPython libraries and flash-resident memories offers much faster and user-friendly development environment via a terminal line to a Laptop, alt least for an initial test and debugging period. The SoC mezzanine is used in similar ways as on the VTC tester [citation VTC] for VMM production testing, where I/O control levels, I2C and SPI buses are routed to all programmable resources and a comfortable user-interface with parameter storage ta database on a Laptop. The eFEC is also connected to programmable resources on frontend hybrids. In the simplest case these are configurations mastered from the eFCE via I2C bus links to registers on the hybrids. Examples for local programmable resources on eFEC are its supply voltage settings, current monitoring and configuration of Flash devices. Connected resources on the frontend include ASIC configurations, baseline and pulser test monitoring and readout of sensors like geographical position, temperature, humidity, B-field or orientation. The target is a resource and configuration control via the FPGA embedded is the final target such that for a full production eFEC, the SoC plugin remains as option for test and development.

5.5 eFEC subsystem for frontend power

Digital ASICs integrated on frontend cards are specified between 10 and 20 mW per channel and require supply voltages between 0.8 to 1.2 Volt. This does however not include the power-loss over cables, dropoff in voltage regulators and power for additional integrated logic like FPGA's, Flash devices, link drivers, sensors and monitoring ADCs. The SRS default readout frontend, the VMM3a hybrid for SRS with 128 channels requires 2 supply Voltages for two ASICs and all support chips on the ASIC carrier card, totalling to : 3V@0.2A and 2V1.7A which is $\mathcal{O}$(4W) per 128 channels, or effectively 30mW/channel compared to the 12 mW specified for the VMM ASIC only. As a rule of thumb, the power budget for the readout frontend should be dimensioned with a factor of 2 of the power/channel-specification of the ASICs and a secondary supply voltage needs to be added for all service and monitoring logic. In order to provide a general-purpose power interface for the SRSe frontend, eFECs implement a programmable 80 Watt, 2 Voltage subsystem. The primary supply for ASICs requires a high-current programmable supply of $\mathcal{O}$(1.8 V) for frontend-resident LDO's and the service logic requires normal-level programmable supply of $\mathcal{O}$(3.3 V). These nominal voltages can be programmed in a $\pm$50% range with current monitoring and auto-fusing.

With 90% efficient DC-DC conversion, the maximal delivered 80 Watt produces $\mathcal{O}$(8 W) of losses for the crate cooling. The dual power panel connector on the eFEC frontpanel assumes the use of the PMX Voltage distributor box [citation PMX] with external Volt/Ampere monitoring per ASIC card and including a high-current, low impedance return GND path to the crates. This power distribution concept was validated in testbeams with a multi-FEC VMM frontend and is generally recommended to avoid ground lifts and/or redundant currents flowing across the detector Ground.

5.6 Crate environment

The eFEC card format is 6U x 220mm for insertion in rack-mountable subracks which comply to DIN 41494 and IEC 60297-3. Crates are mechanically compatible with the "SRS classic" format however may require upgrade of the ATX power supplies since eFEC get exclusively powered via SATA power cables delivering per eFEC up to 110W of which up to 80W are dedicated to the external frontend. Up to 4 eFECs can be powered from 600W ATX power supplies of type "80PLUS" which conform to more than 80% power conversion efficiency from universal AC inputs of 110-240V. The legacy ATX adapter [citation ATX] modules used in classic SRS crates are not required for powering eFECs. Minicrates of size 3U x 220 have one ATX power supply (500W recommended) for powering up to 2 horizontally inserted, eFEC cards and one CTF clock card. Connected to VMM frontends, up to 32 HMDI port links from 2 eFECs add up to a 4k channels for a fully loaded SRSe Minicrate with 4 uplinks of 10 Gbit each. Eurocrates of size 6U x 220 have two ATX power supplies (600W recommended) for up to 8 vertically mounted eFECs and one CTFe clock card. Connected to a VMM frontend, up to 128 HMDI link ports from up to 8 eFECs add up to a 16k channels for a fully loaded Eurocrate with 16 uplinks of 10 Gbit each. Readout backends beyond the channel- capacity of single crates can be incrementally increased, preferable in rack-mounted subracks with interleaved ventilators below each Eurocrate or below every 2 Minicrates. A total of more than 8 FECs requires addition of CTF cards driven from a common external clock source. A portable eCLK box, powered from the Crate 5V power outlet, will become available for driving multiple CTF cards with a common, jitter-free clock or an external clock. Any mixture of Eurocrates and Minicrates is equally possible. Due to the accumulation of the return currents (up to 17A per octal group of 8 VMM hybrids), a very low-impedance ground return copper braid fanout should be connected on the to the GND attachment plates on the rear side of the SRS crates. With 1 copper braid per group of 8 VMM equivalent carrier-cards, 4 copper braids are needed per Minicrate, or 16 per Eurocrate.

5.7 Status of SRSe with the VMM3a frontend

SRS is a very mature readout technology developed since 2009 with resources of the RD51 collaboration and using CERN infrastructure and resources [citation RD51]. Many RD51 collaborators have contributed to its progress with wide acceptance within the MPGD user community. Following a very successful early period with the analogue APV frontend, newer frontend technologies, like SAMPA [citation SAMPA], Timepix [citation TIMEPIX]

and in particular, VMM, have been interfaced to SRS. Based on the latest VMM3a ASIC version developed by BNL for the ATLAS NSW detector, SRS was fully redesigned on all levels for commercial SRS production. By 2021, 250k VMM channels are either in use or are on order for new installations. The SRSe extension represents the next generation of SRS, based on many lessons- learnt from deployed SRS classic systems and adding new functionalities and higher performance. At the time of writing the eFCE module is fully specified from the system level down to the schematics and 3D levels, with delays due to the general ASIC shortage in 2021 the first 2 prototype cards are now expected for Q2 2022 whilst firmware developments on the similar Kintex family with the VMM 3a frontend are already in production.

5.8 Work plan

This LoI represents also a call for competences to implement FPGA-based, trigger functionality with GUI-based user control on the new eFEC platform. As soon as eFEC hardware will become available, the default firmware developed for the VMM frontend on classic FECs (Virtex-6) and Assister cards (Kintex-7) will be adapted to the eEFC Ultrascale+ Zync FPGA as baseline for standard readout firmware already existing in the SRS classic systems. The implementing of the new trigger features will be gradually and driven by requirements of the associated experiments The initial phase consists in bootstrapping of firmware and software on eFEC prototypes in order to establish a baseline readout system, ready for testing and commissioning with user-defined frontends. A template work plan includes the following points

- Use existing frontends (VMM3a, SiPM) as well-known frontend as baseline
- Establish a common user forum modelled after RD51 WG5.1 user group to identify priorities and agree on code exchange rules and practices
- With first eFEC prototypes, establish a full set of uPython procedures to access FPGA resources via I2C, SPI and JTAG
- Establish a Linux-based control and monitoring environment on the embedded multicore system
- Afer initial production of 2 pilot eFECs, launch a first batch production
- If required, develop a MAC and/or Windows-based GUI for embedded use of uPython procedures
- Identify an experiment platform to implement a basic set of triggers (fast-or, veto, coincidence)
- Identify experiments requiring different frontend ASICs for implementing other kinds of link interfaces
- Call for experiments to work on implementation of region and topology triggers

- Establish rules for parameterization of trigger primitives
- Deploy first stand-alone eFEC readout systems with VMM in testbeam -like environment
- Establish a standard user guide for shifters

5.9 Additional Material

In the following one can find pictures (Figures 26 to 33) of the items discussed in the previous sections.

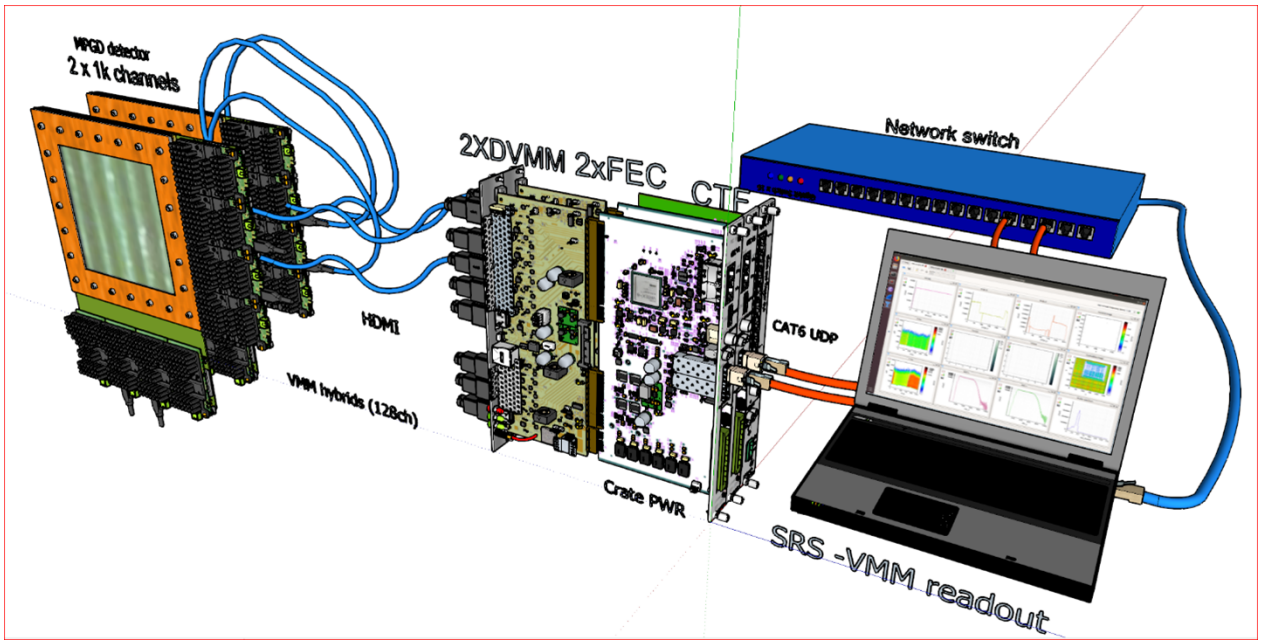

Figure 26: SRS classic small readout systems with FEC, CTF, DVMM adapter, frontend links (HDMI) and VMM3a fronted hybrids attached to 2 GEM planes.

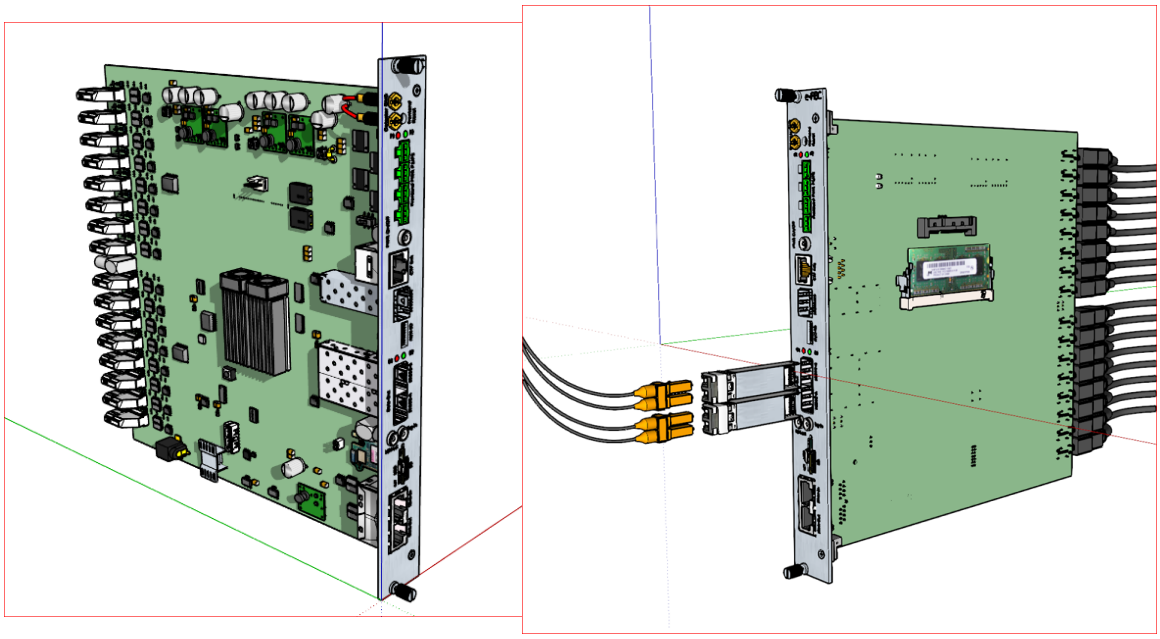

Figure 27: Left: New eFEC module 6U for SRS crates with cooled Ultrascale+ FPGA and 16 generalized HMI link ports. DCDC converters provide programmable power to the frontend. Right: eFEC with rear-side generalized frontend links and two SFP optical output links. The DDR4 data buffer is an optional plugin.

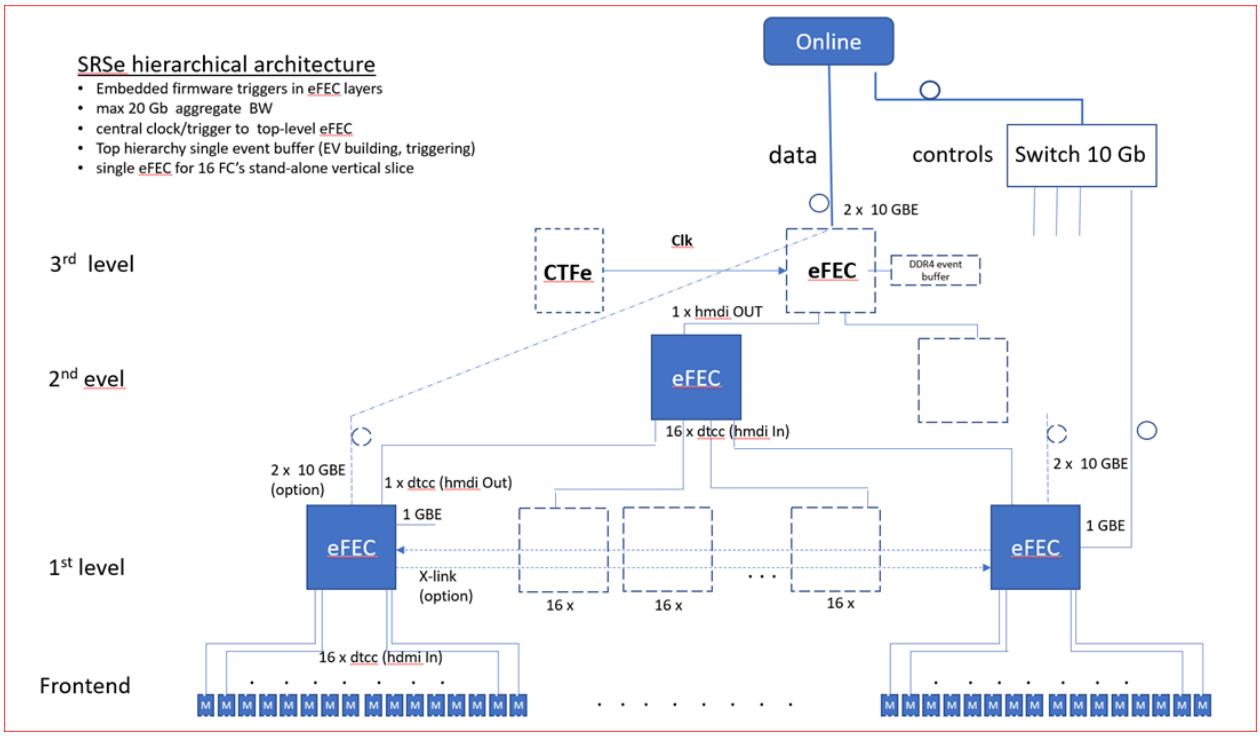

Figure 28: SRSe hierarchical architecture.

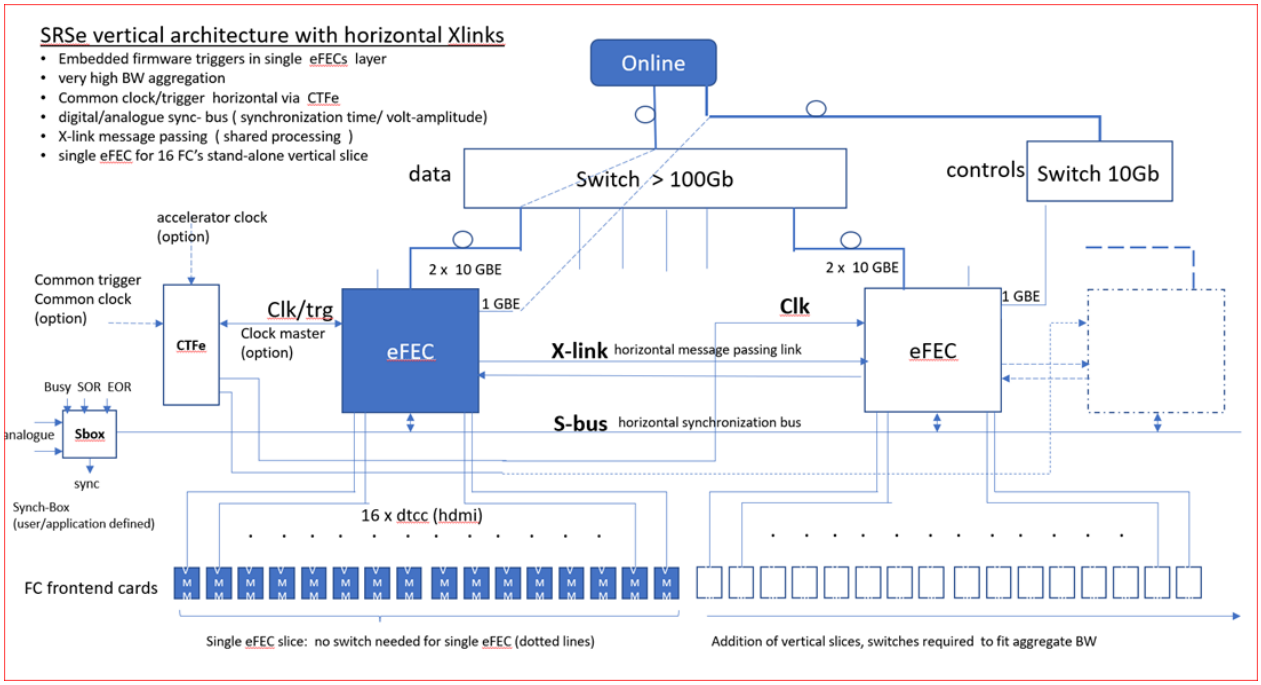

Figure 29: SRSe vertical slice architecture.

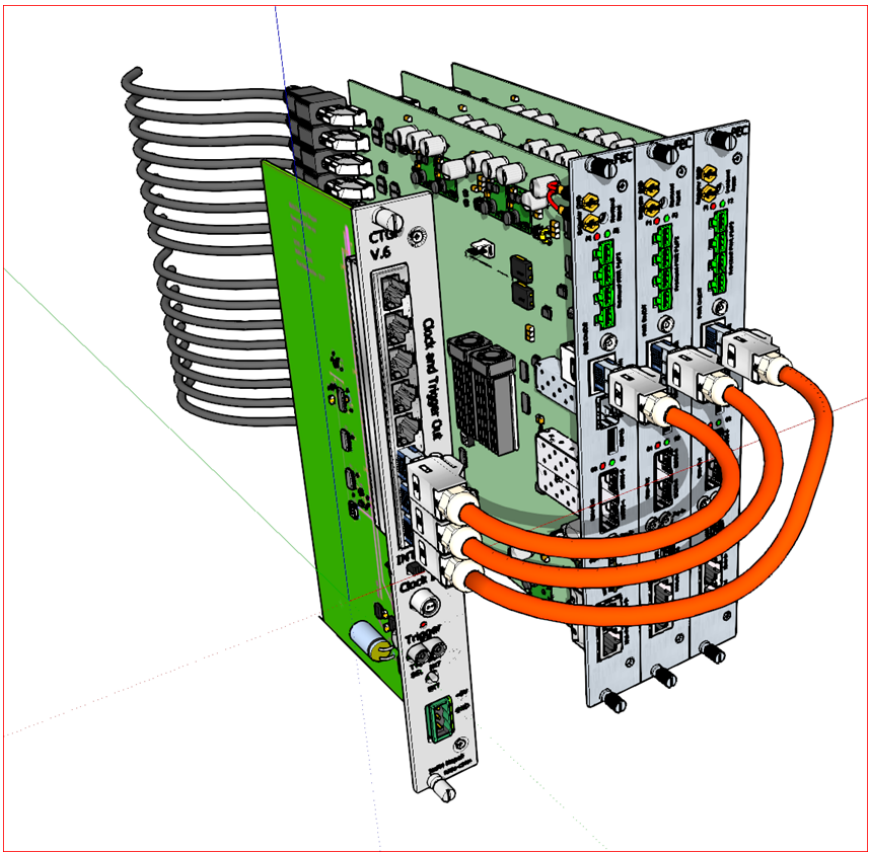

Figure 30: Common clock and trigger for stack of eFECs.

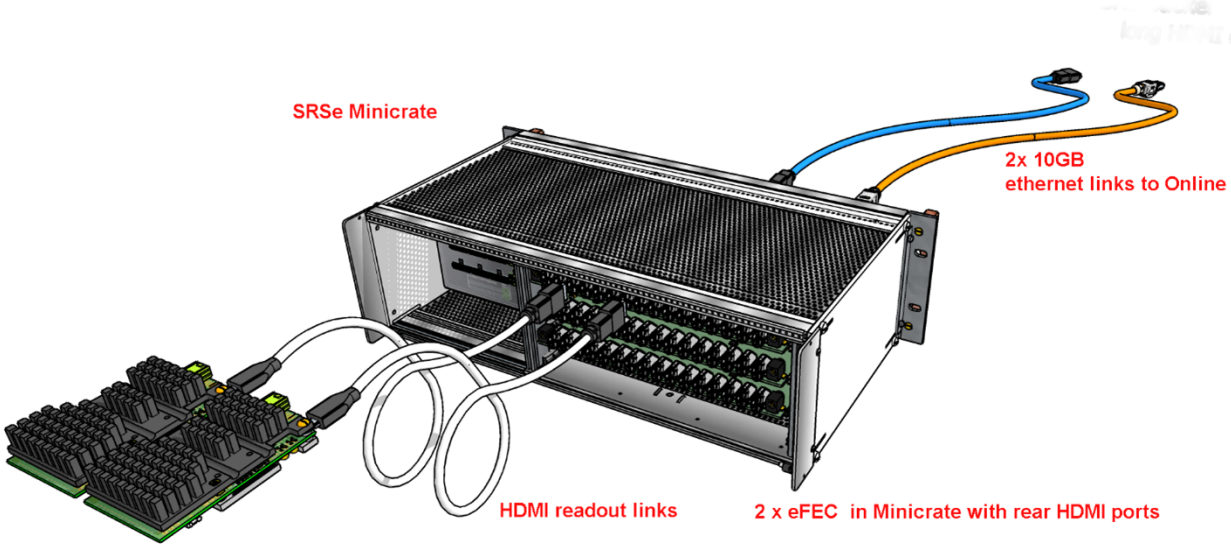

Figure 31: 2 × eFECs with two HDMI readout links for 2 VMM3a hybrids. eFECs housed in a simplified 3U Minicrate (SATA power only).

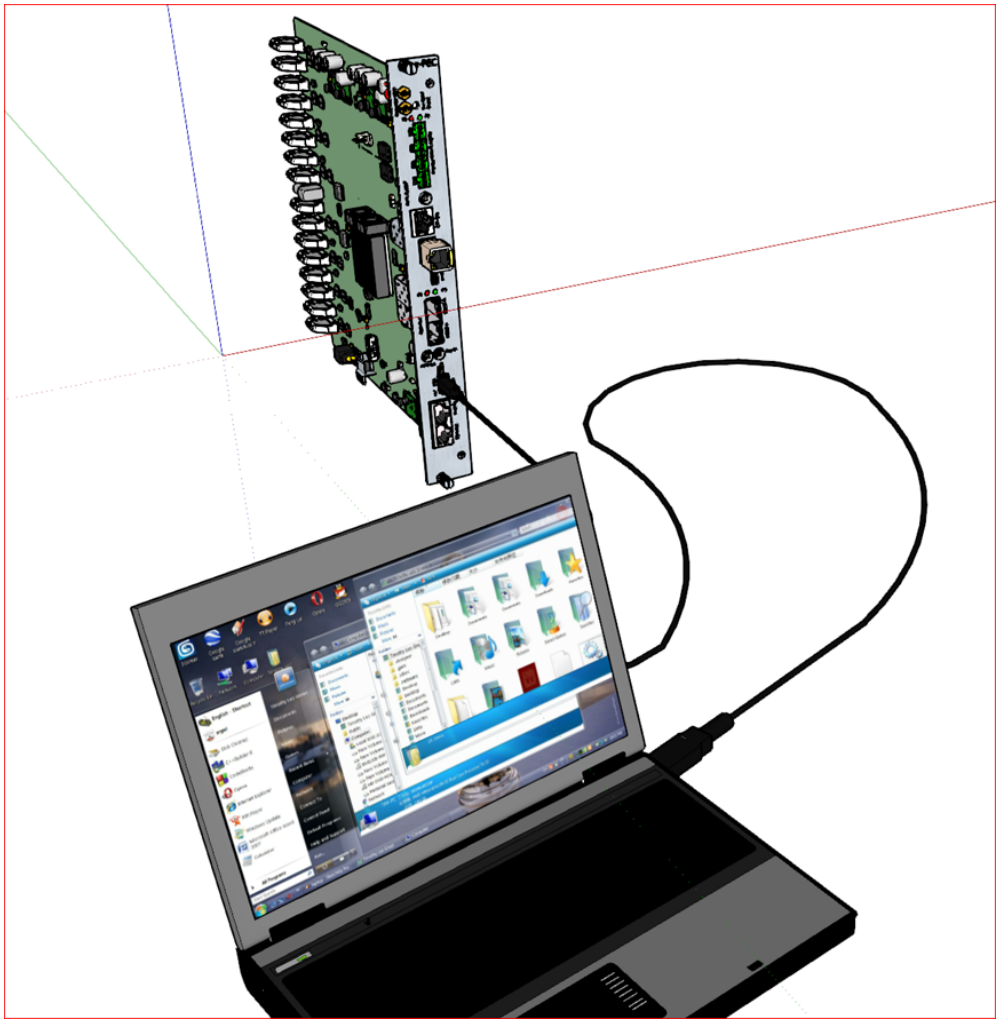

Figure 32: Local eFEC configuration and tests via USB link.

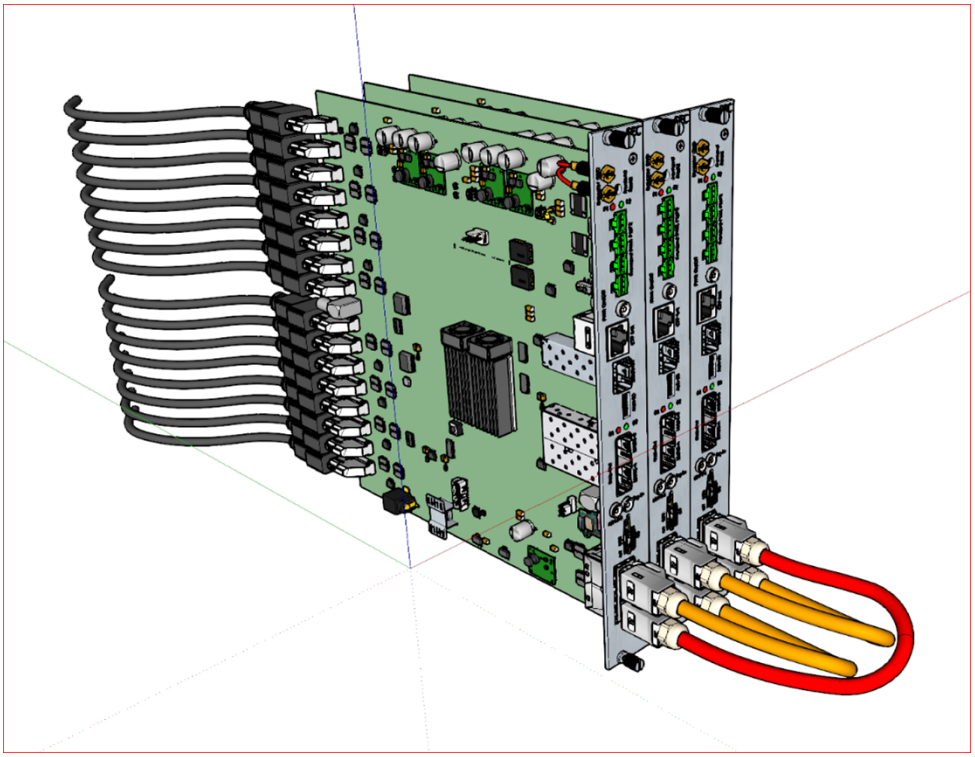

Figure 33: Example of a regional ring topology connected via Xbus network cables.

6 High-gain, low ion-backflow double and triple micro-mesh gaseous structures

6.1 Motivation

Positive Ions produced by electron-molecule collisions during the avalanche process can flow back to the drift region and affect the detector performance in many ways. In gas photon detectors, the ion bombardment can reduce the quantum efficiency of the photocathode or even render it completely ineffective. In the high-rate time projection chambers (TPC), large number of ions flowing back from the amplification region will cause significant non-uniformity of the local electric field in the drift volume and eventually lead to a distortion of the charged particle tracks. Micro-pattern gaseous detectors with high gain and very low ion-backflow (IBF) provide cost-effective solutions to large-area and position-sensitive photon detection and readouts of high-rate TPCs. The backflow fraction of Micro Pattern Gaseous Detectors (MPGD) is smaller than that of the more classical configuration. For example, in the Micromegas detector, a large fraction of the secondary positive ions created in the avalanche can be stopped at the micro-mesh depending on the field ratio, detector geometry, etc.

6.1.1 High rate TPC in future Colliders

It is worth mentioning that the upgrade of the large TPC of the ALICE detector at the CERN LHC provides a successful example of high rate TPC in the real experiment. In the ALICE TPC, The requirement to keep the ion-induced space-charge distortions at a tolerable level leads to an upper limit of 2% for the fractional ion backflow at the operational gas gain of 2000 [1, 2, 3], which was achieved by using stacks of four GEMs, as shown in Fig. 34, GEM foils with standard (S, 140 μm) and large (LP, 280 μm) hole pitch are combined to an S-LP-LP-S configuration. As well as the electric field was also highly optimized with a very low transfer field E_{T3} between GEM 3 and GEM 4 of only 100 V/cm, whereas the other transfer fields and the induction field E_{ind} are kept at typical values around 3500 V/cm. However, the method of the ALICE TPC with four GEMs may be difficult to apply in future large colliders with higher event rate. The International Linear Collider (ILC) is a proposed electron-positron collider for Higgs precision measurements and discovery. The TPC scheme is conceived to be central tracker of the International Large Detector (ILD) concept for the ILC, in which, the IBF ratio should be smaller than 0.1% at an expected gain of $\sim$ 5000. It is like the Circular Electron Positron Collider (CEPC), its TPC solution also requires very IBF ratio at 0.1% level [4, 5].

6.1.2 Gaseous photon detection

Gaseous photon detector (GPD) using micro-pattern gas detectors (MPGDs) have been widely studied owing to their potential advantages, such as large effective area with low cost, high spatial and time resolutions, and high magnetic field resistance. The most com-

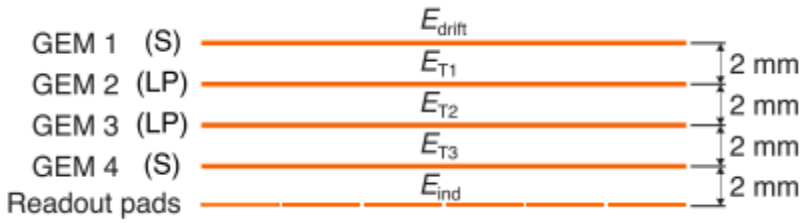

Figure 34: Schematic setup with four GEMs for ALICE TPC [1].

mon examples are photon detectors for ring-imaging Cherenkov counters (RICH) [6, 7] and gas photomultiplier tubes (gas-PMTs) [8, 9, 10]. However, the typical gas-PMT gain is $\sim 10^4$ whereas regular vacuum PMTs have a gain of $\sim 10^6$. Another big challenge in application of gas-PMTs is for IBF suppression. The effect of ion-backflow may cause aging of the photocathodes of GPDs. The quantum efficiency of a GPD will degrade when its photocathode is bombarded by ions [11, 12], which are produced during the gas multiplication process. Some detector structures, based on micro-pattern gaseous detectors (MPGD), have been studied [13] to suppress the IBF ratio, such as the multiple gas electron multiplier structures (multi-GEMs) [14], hybrid structure [5], cascaded GEM to micro-mesh gaseous structure (Micromegas) [15], and micro-hole and strip plates (MHSP) [10, 16].The studies mentioned suggest that mesh-type MPGDs have a better IBF suppression capability than hole-type ones. This therefore provides motivation to fully explore the mesh-type structure for gaseous photon detection.

6.2 Concepts and R&D status

6.2.1 Double micro-mesh gaseous structure (DMM)

For the purpose of high gain and low IBF, a double micro-mesh gaseous structure (DMM) [17, 18, 19] with two avalanche stages, was developed using a thermal bonding method [20]. The structure of a DMM is illustrated in Fig. 35. It has a 3-5 mm gas gap for particle primary ionization and electron drift, followed by a $\sim$ 0.2 mm PA gas gap and a $\sim$ 0.1 mm SA gas gap that are defined by two meshes and an anode. The structure is quite similar to that of a typical Micromegas except that it has two layers of meshes to provide cascading avalanche amplification. A typical Micromegas has only one layer, hence giving single avalanche amplification. The double cascading avalanche gaps ensure a very high gain for a single electron and, with the proper configuration of electric field, a low IBF ratio. It also preserves the advantages inherited from the typical Micromegas in terms of high-rate capability, good time resolution, and excellent spatial resolution. The DMM prototypes were fabricated and studied with X-ray and UV lights at first step, its features of high gain of $> 10^6$ and low IBF ratio of $\sim 0.05\%$ was validated [17]. Then the DMM structure was optimized to further suppress its IBF by changing the size of gas gaps and the density of the wire mesh, and more significantly, by aligning the two mesh layers with a crossing angle. A series of DMM prototypes with differing crossing angles, PA gaps, and mesh types were fabricated and investigated using X-rays (5.9 keV from ^{55}Fe source and 8.0

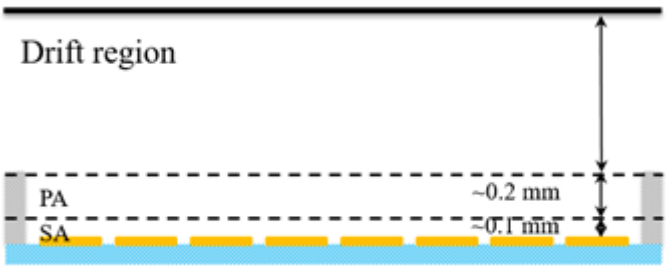

Figure 35: Schematic design of the DMM.

keV from an X-ray gun). The results (as shown in Fig. 36) of this investigation indicate that a low PA voltage, large PA gap, high mesh density, and crossed mesh setting improves IBF suppression at the same total gain. A low IBF ratio, as low as 0.025%, was obtained with the prototype, which was made of 650 LPI mesh and had a PA gap of 240 μm and a cross angle of 45deg. In addition, the measurement method for the gas gains and currents was validated. The ion space charge effect was studied and verified to be negligible in the case of very low IBF ratio in a DMM. The stability of the DMM prototype was also measured with a low sparking probability, smaller than 10^9, in a test done over 20 hrs [18, 19].

6.2.2 Triple micro-mesh gaseous structure (TMM)

A triple micro-mesh gaseous structure (TMM) is a natural extension to further suppress the IBF that comes from the SA stage of the DMM. Following the idea of multi-mesh, a triple micro-mesh gaseous structure (TMM) is a natural extension to further suppress the IBF that comes from the SA stage of the DMM. Fig. 37 shows the schematic design of the TMM, it has one more mesh above the DMM. A TMM prototype was also fabricated with the thermal bonding method [20] and studied to explore the limit for IBF suppression. As shown in Fig. 38 very excellent high gain and ultra-low IBF of $\sim 0.003\%$ is achieved, which reaches one order of magnitude lower than that of the DMM, the lowest IBF value ever obtained with gaseous detector.

6.3 Plans and objectives

Following the R&D works mentioned above, more simulations and tests should be carried out to comprehend the mechanisms and influence factors on the main features of gain, IBF suppression, resolution, etc., to provide guidance for further optimization of the DMM/TMM. We also must notice that the IBF is not the only parameter that decides the choice of the detector, in the previous study, the IBF was optimized while maintaining the others acceptable. Trade-off optimization in different parameters is required for the specific applications.

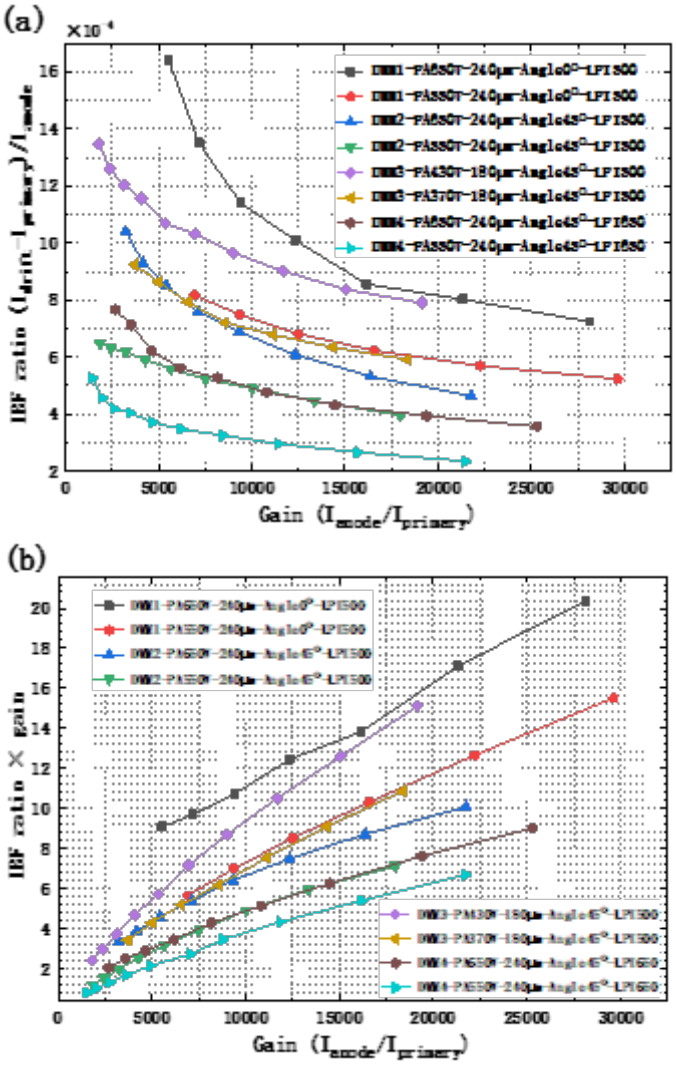

Figure 36: (a) IBF ratio versus total gain with a fixed PA voltage, for all detectors; (b) the product of the IBF ratio and gain versus the total gain.

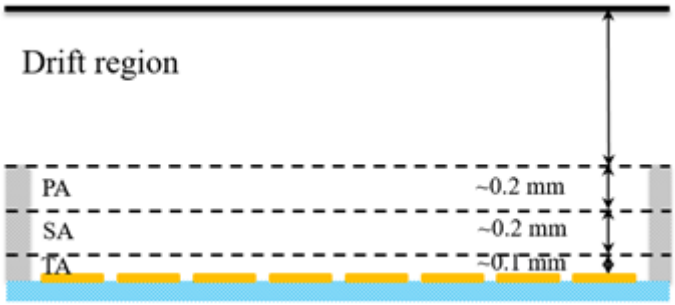

Figure 37: Schematic design of the TMM.

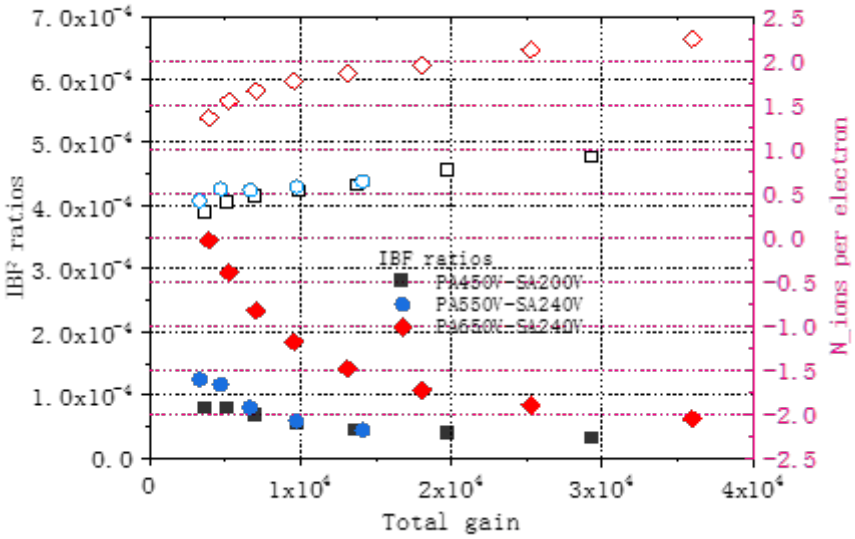

Figure 38: IBF ratio (solid dots) and the product of the IBF ratio and gain (hollow dots) versus total gain with fixed PA and SA voltages.

6.3.1 Optimization and improvement

6.3.2 Toward large area detector

However, the current results were tested with small area (25 mm×25 mm) prototypes, it is a crucial issue to produce the DMM/TMM with proper sensitive area (i.e., 100 mm×100 mm and larger), which is one of the biggest challenges for its application in a real experiment. A dedicated fabrication process using thermal bonding method was designed and a larger DMM prototype with an active area of 160 mm×160 mm was successfully fabricated.

6.3.3 Studies on specific application

The demand of real experiments is the greatest motivation for detector R&D, our studies will focus on the potential applications of the high-rate TPCs and Gas-PMTs, where the absolute backflow ion number (gain × IBF) of ~ 1 at a gain of higher than 1000 and low IBF ratio of 0.01% at a high gain of 105 are expected individually.

6.4 Summary

We have developed and optimized a double micro-mesh gaseous structure (DMM) with two avalanche stages, which has a low IBF ratio and high gain. An IBF ratio as low as 0.025% was obtained and a gain of up to 3×10^6 was reached for single electrons for the DMM.

A triple micro-mesh gaseous structure (TMM) was also developed to further explore the potential of the multi-mesh method, excellent high gain and ultra-low IBF of $\sim 0.003\%$ is achieved, which is the lowest IBF value ever obtained in gaseous detectors. These features of the DMM and TMM present their strong potential for Gas-PMTs, RICH photoelectric readout, and high-rate TPCs.

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