# Large area CMOS monolithic active pixel sensors for future colliders

Martin Breidenbach, Angelo Dragone, Norman Graf, Tim K. Nelson, Lorenzo Rota, Julie Segal, Christopher J. Kenney, Ryan Herbst, Gunther Haller, Thomas Markiewicz, Caterina Vernieri, Charles Young

*SLAC National Accelerator Laboratory*

James Brau, Nikolai Sinev, David Strom

*University of Oregon, Eugene*

Marcel Demarteau

*Oak Ridge National Laboratory*

## Contents

# 1 Introduction

Collider detectors have taken advantage of the resolution and accuracy of silicon detectors for at least four decades [1]. Future colliders will need large areas of silicon (Si) sensors, several hundred $m^2$, for low mass trackers and sampling calorimetry [2]. Trackers will require multiple layers, large radii, and micron scale resolution. Sampling calorimeters will also have very large areas and are improved by very thin overall packages which reduces the Moliere radius. A promising technique is CMOS Monolithic Active Pixels (MAPs), in which Si diodes and their readout are combined in the same pixels, and fabricated in a standard CMOS process [3, 4]. CMOS MAPs sensors have several advantages over traditional hybrid technologies with sensors bonded to readout ASICs. Integrating sensors and front-end electronics on the same die removes the need of interconnections, thus reducing complexity and mass. The close connection of sensor and front-end amplifier reduces input capacitance which reduces the achievable noise floor and thus for the same S/N ratio allows for a reduction in signal and therefore sensor thickness, which also reduces mass. CMOS devices are made in standard commercial technologies with small feature size allowing fine readout pitch. Furthermore designs in standard commercial technologies can be produced quickly and inexpensively, because of an active industrial market, potentially enabling large area detectors. Nevertheless challenges are present. Full depletion of the device is required for the charge to be collected by drift and not by diffusion, allowing a fast time response and radiation hardness. This adds design complexity and might require access to process customization. CMOS chip dimensions are typically limited to a reticle of about 2 cm by 2 cm. This scale is difficult unless they can be stitched together on large area wafers, and their digital readout area limited to one or two edges MAPs are being used in the STAR Heavy Flavor Tracker at BNL RHIC [5] and will be deployed in the ALICE ITS system for heavy ions at the LHC [6]. ALICE will have 10 $m^2$ of sensor with about 24,000 MAPs chips. We want to go to the next generation of MAPs, emphasizing both the pixel development for speed and resolution, and the system approaches needed for large scale use at reasonable cost. We propose to develop two types of fully depleted MAP sensors with characteristics suitable for Trackers and Electromagnetic Calorimeters. With an outlook to a broader range of future applications we will use the requirements of the SiD detector for ILC [7]. This work will directly address the issues of making large surfaces by developing the intermediate stage of tens of $m^2$, including powering and readout of large numbers of MAP sensors. It will enable detectors with far more pixels per

unit area, and thus higher resolution, with substantially lower mass budget and significantly lower cost.

# 2 MAPS developments

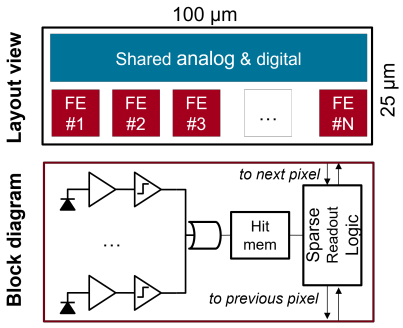
## 2.1 Pixel architecture

A large part of the international research efforts on MAPS are focused on the development of detectors for circular colliders with a continuous-time pixel front-end architecture [**?**, **?**]. Such architectures are not compatible with the requirements of low duty cycle lepton colliders, particularly in terms of timing resolution and power consumption.

The novel TowerJazz 65 nm imaging process is the current state-of-the-art process for HEP MAPS detectors. We will evaluate the performance of the TowerJazz 65 nm process by designing and fabricating a small MAPS prototype, with a target size of approximately 5x5 $mm^2$. The readout circuitry of this first prototype will be optimized for low-duty cycle machines, leveraging the beam timing structure of linear colliders. In particular, we will adopt two techniques. The readout electronics will have to be optimized for operation with power pulsing: the analog front-end circuitry will be powered off during the dead-time between different bunch trains. With low duty cycle machines like $C^3$ and ILC, this technique enables a power reduction by more than two orders of magnitude. We will leverage power pulsing techniques which were developed at SLAC for the KPix project [**?**]. Second, the pixel front-end circuitry will be based on a synchronous readout architecture, where the operation of the circuitry is timed with the accelerator bunch train. In this way, the noise and timing performance of the circuitry can be optimized while reducing power consumption. During the last decade, SLAC has developed several ASICs for the Linear Coherent Light Source (LCLS), gaining world-wide expertise in synchronous readout architectures operating with fast integration times [8]. By combining all these techniques, we aim to achieve the target specifications described in in Table 1, which are the results of a preliminary design carried out with previous funding. A concept of pixel architecture is shown in Fig. 2.1. The pixel sensing nodes and front-end (FE) circuitry will be segmented in $N$ channels to minimise the charge collection time. Each FE analog channel consists of a Charge Sensitive Amplifier (CSA) and a discriminator. The outputs of the discriminators will be connected to a shared digital logic block, which will store the hit information. Due to the low occupancy, each pixel will need to store only one hit for each bunch train, thus in turn enabling a smaller

| Parameter | Value |
|---|---|
| Min. Threshold | 140 $e^-$ |
| Spatial resolution | 7 $\mu$m |
| Pixel size | 25 x 100 $\mu m^2$ |
| Chip size | 10 x 10 $cm^2$ |
| Chip thickness | 300 $\mu$m |
| Timing resolution (pixel) | ~ns |
| Total Ionizing Dose | 100 kRads |
| Hit density / train | 1000 hits / $cm^2$ |
| Hits spatial distribution | Clusters |
| Power density | 20 mW / $cm^2$ |

Table 1: Target specifications for 65 nm prototype.




figurePreliminary architecture of the pixel front-end. Top: layout view of a 100x25 µm pixel. The Bottom: block diagram of a pixel circuit.

pixel size. We will implement a sparse read-out mechanism, so that only pixels containing a hit will transmit hit information to the circuits located in the periphery (here referred as balcony). The distribution of a clock signal across such a large area would result in power consumption which exceeds the requirements. For this reason we will develop an asynchronous read-out logic, which will minimise the digital power as well as make the circuitry more robust to local variations of the transistors performance.

### 2.2 Wafer-scale design

Once the design of the small-scale prototype has been completed, we will move to the design of a wafer-scale MAPS based on a stitching process. We will adopts a top-down approach, where the challenges of wafer-scale design are addressed from the early development phases. This will help to identify the risks that wafer-scale MAPS pose at system-level, such as yield, power distribution and fill factor and will help to investigate risk-mitigation techniques. The plan is to fabricate a first prototype of a wafer-scale device, which will be used to evaluate essential aspects of the integration of such devices into a detector system: *i.e.*, cooling, assembly procedures, wafer thinning and handling and power delivery. This would also minimise risks while reducing the costs.

The development of wafer-scale MAPS will allow us to investigate the following challenges:

- Power pulsing: to take full advantage of the power pulsing technique,

the current drawn from the supply needs to reach the peak value in the shortest time possible, minimizing the duty cycle and thus decreasing the average power consumption. However, the current consumption of a matrix of $10^6$ pixels increases by several Amperes in a matter of microseconds. At the same time, the supply voltage needs to reach a stable value to not inject noise in the analog circuitry of the pixel.

- Power distribution: the distribution of the power supply over a large area is challenging because of the non-negligible voltage drop over long metal distribution lines. We will evaluate local voltage regulators distributed across the die. An alternative approach could be postprocessing the CMOS wafers with wafer-level packaging techniques (such as a Re-Distribution Layer) to deposit additional metal layers on top of the existing ones, thus reducing the interconnection resistance.

- Yield: the probability of fabrication defects scales with the area of the device. For reticle-size MAPS, a defect in one reticle would result in a lower number of usable dies per wafer. However, a defect on a wafer-scale device is almost inevitable and could result in the loss of a full wafer. Therefore, it is essential to develop techniques to mitigate the effects of fabrication defects, such as shorts between supply and ground lines. We will study ways to segment the sensor into independent sections, as well as the trade-offs between circuit and interconnections density, stitching design rules, and yield.

- Stitching techniques: the design of integrated circuits with reticle stitching introduces additional layout design rules which improve fabrication yield and which are not traditionally encountered during reticle-scale designs. Exposing IC designers to such design rules is an essential goal of this proposal and it is the first step towards the development of wafer-scale devices.

- Assembly and power delivery: while preliminary mechanical and assembly tests will be carried out at SLAC on mock devices, a functional sensor will be used to study the techniques to deliver power to such sensors while also reducing the cross section of the cables, thus further reducing the dead material of the detector.

## 3 Performance for the ECal at future e+e-

The finely granular, digital readout of the SiD ECal offered by application of CMOS MAPs sensors provides the potential for significantly enhanced performance over that envisioned in the ILC Technical Design Report (TDR). [2] One advantage of this digital approach over the TDR analog approach is the reduction of the effects due to variations in energy deposition, such as Landau fluctuations. Fluctuations in the development of the shower remain as the main contribution to resolution. The fine granularity also reduces the likelihood of overlapping particles per pixel and improves the separation of nearby distinct showers, such as from high energy pi zeros or jets, and contributes to improved particle flow pattern recognition. Quantifying the nature of these effects is being investigated with GEANT4 simulations.

The pixel configuration of $2500\,\mu m^2$, segmented as $25\,\mu m$ x $100\,\mu m$, is designed for the tracking performance derived from the precision of the $25\,\mu m$ size. Excellent performance with a purely digital ECal based on this fine granularity is expected. Previous studies [9, 10, 11] have even indicated potential energy resolution advantages for a digital ECal solution (see Figure 1).

New simulation studies, based on this fine, digital configuration, have confirmed the previous studies referred to in Figure 1 and demonstrated additional details on the performance [12]. These studies indicate the electromagnetic energy resolution based on counting clusters of hits in the MAPs sensors should provide better performance than the SiD original design based on $13\,mm^2$ analog pixels. This is shown in Figure 2.

GEANT4 simulations of the performance of digital MAPs applied in the electromagnetic calorimeter has been under development and study throughout 2021, and are continuing. [12] These studies are aimed at understanding the ultimate performance and limitations, and to inform the ASIC designers on the requirements for the sensor chips. The expected performance has been found to exceed the requirements and performance of the SiD TDR ECal design. Pixel structures of 25x100 $\mu m^2$ achieve equivalent performance to a 50x50 $\mu m^2$ design. The 5 T magnetic field has been found to have a minor effect and to degrade the resolution by a few per cent due to the impact on the lower energy electrons and positrons in a shower.

Two shower separation is excellent, as shown in Figure 3 for two 10 GeV electron showers separated by one centimeter and Figure 4 of two 20 GeV gamma showers from a 40 GeV $\pi^0$ decay. The fine granularity of pixels provides excellent separation. The performance for two electron showers versus

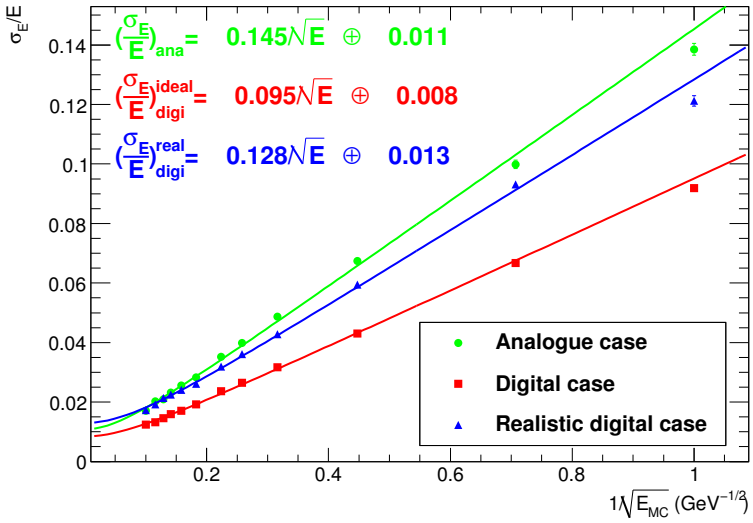



Figure 1: The energy resolution as a function of the incident energy for single electrons for both analog and digital readout using a GEANT4 simulation. The realistic digital cases includes effects of saturation and charge sharing, leading to a degradation of 35% [9].

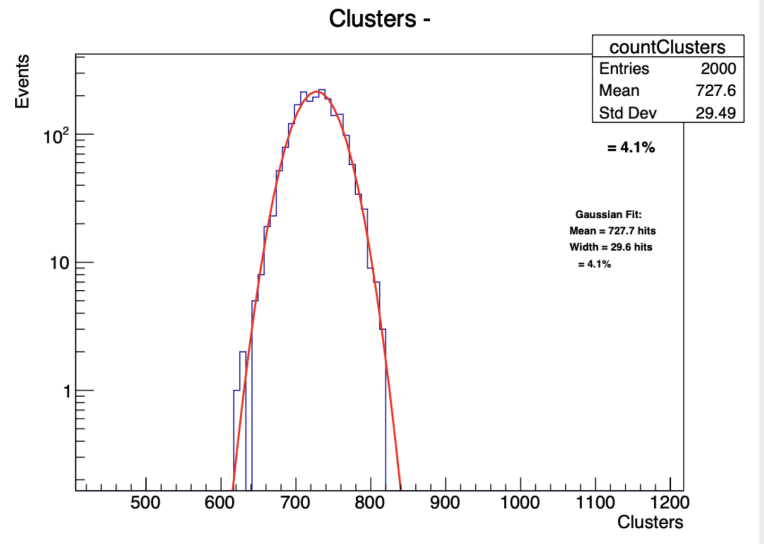



Figure 2: The distribution of cluster counts for a 10 GeV electron shower in the new SiD digital MAPs design based on a GEANT4 simulation. [12]

their separation is summarized by Figure 5. The fine granularity allows for identification of two showers down to the millimeter scale of separation, and the energy resolution of each of the showers does not degrade significantly for the millimeter scale of shower separation.

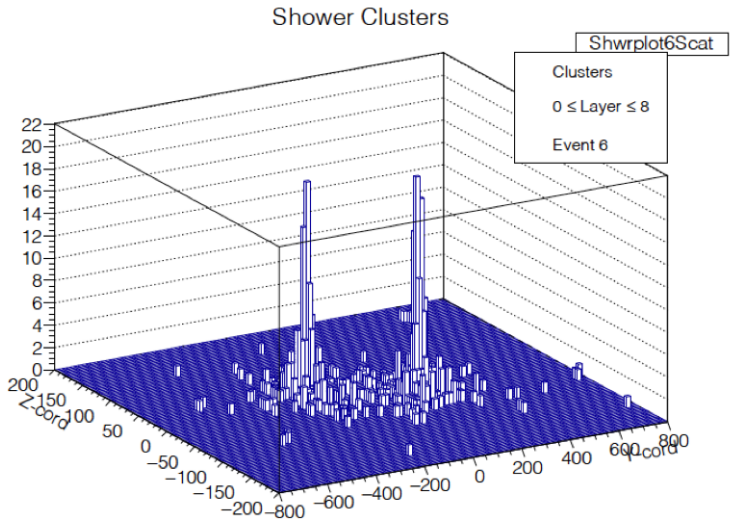



Figure 3: Transverse distribution of clusters in the first 5.4 radiation lengths for two 10 GeV electron showers with a separation of one centimeter in the new SiD digital MAPs design based on a GEANT4 simulation. [13]

Figure 6 shows the gamma energy resolution performance for the range of measurements from the basic mip counting (dark blue, an idealized, best possible resolution) to that achieved by analyzing hits in clusters (light blue). These simulations are now mature and are well positioned to guide the design and production of the sensors. (Note- gamma resolution is somewhat worse than electron resolution due to the different nature of the shower development.) Future planned studies include the reconstruction of showers and $\pi^0$s within jets, and their impact on jet energy resolution, and the measurements of the Higgs branching ratios.

Future studies include:

- Optimal Pixel size for a MAPs sensor-based ECal;
- Comparison of analog and digital ECal performance;
- Optimization of the overall ECal design;

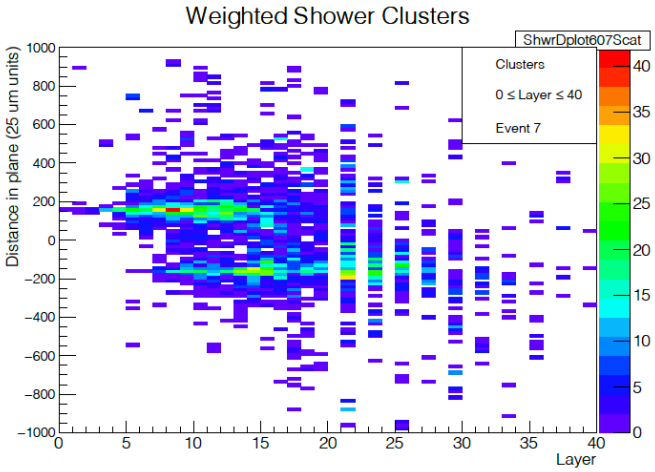



Figure 4: Projection in z-layer plane of the pixel clusters in two 20 GeV gamma showers emerging from a 40 GeV pi zero decay. The z direction is the 100 $\mu$m pixel direction and the layers shown are 20 thin (0.64 $X_0$) followed by 10 thick tungsten layers. Each vertical bin is 400 $\mu$m wide. The two showers are separated by less than one centimeter. [12]

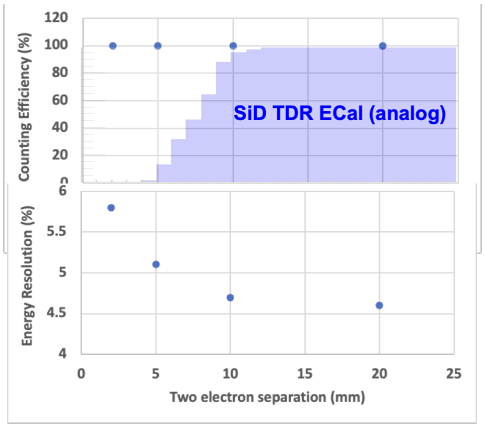



Figure 5: Efficiency for distinguishing two 10 GeV electron showers as a function of shower separation (upper curve) and the degradation of energy resolution as a function of separation due to overlap of cluster hits (lower curve) in the new SiD digital MAPs design based on a GEANT4 simulation. [12]

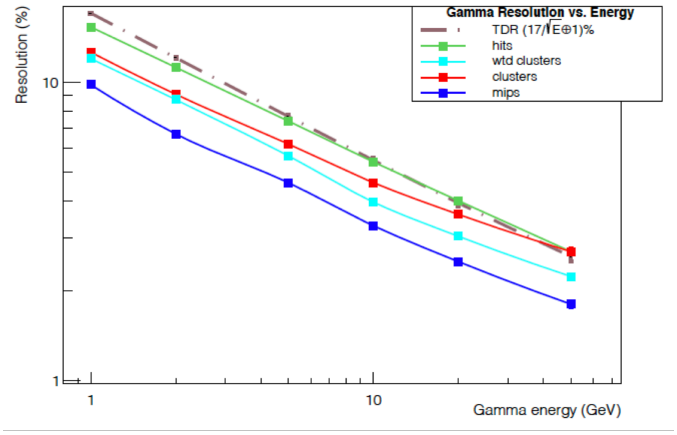



Figure 6: Energy resolution for gamma showers as a function of energy. The curves show (from lower up) the resolution based on a.) counting minimum ionizing particles (dark blue, mips), b.) modified cluster counting (light blue), c.) pure simple cluster counting (red), d.) active pixels (green, hits), and e.) the required performance from the ILC TDR (brown dash-dot). [12]

- Optimization of the design for manufacturabilty, possibly with robots.

The large volume of data provided by a MAPs sensor-based ECal reveals details of particle showers. The extraction of the most pertinent information, for example particle energy, particle type, and the separation of nearby and overlapping showers, provides an opportunity to apply Machine Learning techniques. We propose to apply such deep learning methods to particle and jet reconstruction in the SiD collider detector ECal based on MAPs sensor technology.

## 4 Performance for the ECal at EIC

## 5 Performance for the Tracker

## 6 Large area MAPs: next steps

## References


[1] P. Allport, *Applications of silicon strip and pixel-based particle tracking detectors*, Nature Reviews Physics **1** (2019) 567–576.

[2] Ties Behnke and James E. Brau and Philip N. Burrows and Juan Fuster and Michael Peskin and Marcel Stanitzki and Yasuhiro Sugimoto and Sakue Yamada and Hitoshi Yamamoto, *The International Linear Collider Technical Design Report - Volume 4: Detectors*, arXiv:1306.6329 [physics.ins-det].

[3] I. Perić, *A novel monolithic pixel detector implemented in high-voltage CMOS technology*, in *2007 IEEE Nuclear Science Symposium and Medical Imaging Conference*, vol. 2, pp. 1033–1039. 2007.

[4] D. L. Pohl et al., *Radiation hard pixel sensors using high-resistive wafers in a 150 nm CMOS processing line*, JINST **12** (2017) no. 06, P06020, arXiv:1702.04953 [physics.ins-det].

[5] Contin, Giacomo, *The MAPS-based vertex detector for the STAR experiment: Lessons learned and performance*, Nuclear Instruments and Methods in Physics Research Section A: Accelerators, Spectrometers, Detectors and Associated Equipment **831** (2015) .

[6] ALICE Collaboration, *The MAPS-based ITS Upgrade for ALICE*, PoS **Vertex2019** (2020) 003, arXiv:2001.03042 [physics.ins-det].

[7] SiD Consortium Collaboration, A. P. White, *The SiD Detector for the International Linear Collider*, in *Meeting of the APS Division of Particles and Fields*. 10, 2015. arXiv:1511.00134 [physics.ins-det].

[8] A. Dragone, P. Caragiulo, B. Markovic, et al., *ePix: A class of front-end ASICs for second generation LCLS integrating hybrid pixel detectors*, in *2013 IEEE Nuclear Science Symposium and Medical Imaging Conference (2013 NSS/MIC)*, pp. 1–5. 2013.

[9] J. Ballin, P. Dauncey, A.-M. Magnan, M. Noy, Y. Mikami, et al., *A Digital ECAL based on MAPS*, (2009) , arXiv:0901.4457 [physics.ins-det].

[10] SPiDeR Collaboration Collaboration, *Advanced monolithic active pixel sensors for tracking, vertexing and calorimetry with full CMOS capability*, Nucl.Instrum.Meth. **A650** (2011) 178–183.

[11] SPiDeR Collaboration Collaboration, *Performance of CMOS sensors for a digital electromagnetic calorimeter*, PoS **ICHEP2010** (2010) 502.

[12] J. Brau, *private communication*, tech. rep., 2021.

[13] J. Brau, *The SiD Digital ECal based on Monolithic Active Pixel Sensors*, .