Integration and Packaging

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1 Introduction

Simone Mazza, Ron Lipton Design of modern silicon-based detector systems used for tracking and calorimetry are, to a large extent, dominated by limitations imposed by system packaging. Issues include device cooling and thermal interfaces, power dissipation, inter-device and off-detector communication, and low mass mechanical supports. There have been major advances in these areas that have enabled the large-scale trackers in CMS and ATLAS and the silicon-based calorimetry in CMS. These include liquid CO_2-based cooling, extensive use of carbon fiber, and increasingly complex hybrid and PC board technology. However state-of-the art packaging and integration technologies now available can significantly extend the reach and effectiveness of future detectors, enabling lower mass, finer pitch, and lower noise systems.

Recent HEP experiments have been mostly relying on bump bonding for high density pixel to ASIC connection. This connection technology was proven to be reliable however it is know to have several limitations, both electrical and mechanical. It works down to the 50 μm scale but with issue of yield arising at lower scale. However, if the sensor technology reaches very high granularity it is necessary to develop a high density interconnect process with the readout electronics. The 3D integration technology is common in communication, computing and medical industries, however the option of 3D integration is currently not available in the international HEP community. This technology for high density interconnect would be of extreme interest for future HEP experiments. It will allow for finer pitch detectors with increased performance and mechanical stability, allowing a high density interconnect between sensor and electronics with a readout pitch that can be lower than 10 μm. This is crucial in many fields, for example for particle detection very close to the interaction point.

2 Advantages of advanced packaging

Robert Patty (Nhanched document summary), Simone Mazza, Ron Lipton

2.1 Footprint

Devices that share a package take up less space than if they were packaged separately. A multi-layer 3D chip may be no larger than a single traditional 2D chip, thus offering appreciable size reduction. Furthermore the single components do not need a support wafer after integration, allowing for very thin layers of detectors and readout.

2.2 Speed

Devices assembled in 3D are much closer together than chips on a circuit board. The vertical 3D connections in the device stack are only a fraction of the length of circuit board wires. Shorter distances allow electronic signals to travel more quickly from one component to another, so a 3D assembly can demonstrate higher performance than an equivalent circuit board. Past work has shown 3-5x improvement in latency or speed.

2.3 Performance

3D integration drastically lowers the parasitics of the interconnect wiring. NHanced's TSVs typically have only 2-3fF of capacitance and less than 3 ohms of resistance. In sensor applications, using DBI rather than micro-bumps has been shown to reduce noise and improve signal gain by 30% or more.

2.4 Power

The shorter connections in 3D assemblies also save significant power. Today, most of the power expended in systems is consumed by driving signals in wire, whether on-chip or across circuit boards. Additionally, when signals are external to a packaged device, the devices must have protection on the signal drivers and receivers to avoid ESD (electrostatic discharge) damage. ESD protection adds capacitance, and thus consumes more energy, when signals are driven in the interconnect wiring. 3D integration eliminates the need for ESD protection on the wiring between chips. Past work has shown 90% or more power reduction in the energy consumed by the interconnect.

2.5 Heterogeneous Integration

The devices in a 3D assembly are manufactured separately, so they can vary widely. Each device may come from a different supplier, be built in a different process, incorporate different materials, etc. The components may differ in scale, voltage, dimensions, and any number of requirements. Best of class technology options can be applied to each functional layer separately.

2.6 Robustness

3D assembled layers will interface with one another through DBI connections, which have very few mechanical weaknesses. In fact, 3D devices display robustness similar to a counterpart monolithic 2D part before packaging. However, 2D devices need to interface through wire bonding or solder bumped connections, package to circuit board soldering, and the circuit board itself, all of which have mechanical weaknesses. Because 3D technology greatly reduces the number of packages involved in a system, it better suited to withstand harsh environments than traditional circuit board collections of packaged 2D counterparts.

2.7 Security

An additional benefit of 3D is improved security. 3D devices integrated with DBI are inseparable after assembly. Attempting to separate the layers of a device would destroy them. Further, the outermost layers are assembled facing inward, thus obscuring their active surfaces and making reverse engineering much more difficult.

3 Commercial Availability

Variants of the 3D integration technology originally developed by Ziptronix as Direct Bond Interconnect (DBI) has now been adopted by an number of foundries under the generic term ”Hybrid Bonding”. This technology is now almost universally used for cell phone image sensors, most notably by Sony who licensed the process in 2015. Hybrid bonding is the process of bonding pairs of devices (wafer to wafer or chip-to-wafer) to achieve very fine pitch, robust interconnects. In addition to the hybrid bonding connections must be extracted from the device layers, which are buried after the bonding. This is usually done using Through-Silicon-Vias (TSVs) which can be inserted as part of the foundry process. Currently, TSVs are available to HEP from a few foundries [1] with several others providing TSV insertion after the CMOS wafer is fully processed. Hybrid bonding itself has wider availability[2].

3.1 Industry Partners

3.1.1 NHanced

Robert Patty (Nhanced document summary)

NHanced Semiconductors has assembled 2.5/3D integrated circuits for more than a decade. We have shown active circuits stacked to a height of 8 layers. 3D assembly of test wafers has been demonstrated to a 3D stack height of 16 layers. NHanced has successfully assembled many heterogeneous 3D devices with elements such as memory, FPGAs, microprocessors, ROICs, and sensors. NHanced has produced dozens of different 3D devices and several Focal Plane Array (FPA) and Logic on Memory (LoM) parts for customers. To date, NHanced has worked with more than 100 groups to produce 3D integrated circuits. NHanced performs the 2.5/3D assembly process in its own facility in North Carolina. NHanced 2.5D and 3D assembly technology covers several techniques including copper to copper diffusion bonding and covalent oxide bonding. NHanced can practice these and other assembly techniques in both wafer-to-wafer and die-to-wafer assembly. Correct operation and reliability of previously 3D assembled devices has been verified at temperatures down to 77°K. The Direct Bonding Interconnect (DBI) process has been demonstrated with maximum processing temperature as low as 125°C.

NHanced DBI Processing A key step in the DBI process is the direct bonding of two surfaces (dies or wafers) using Van der Waals forces. The direct bond process is a two-stage kinetic reaction. At room temperature, the wafers are aligned and brought into contact. The wafers have a natural dipole layer of moisture (water) adsorbed onto the surface that initially repels the opposite surface. The wafers “float” above each other until a gentle force, usually a mechanical pin, presses lightly at the wafer edge. This overcomes the electrostatic repulsion so that the water molecules bond through Van der Waals forces. Subsequent heating to high temperatures is necessary to achieve high bond strength through the formation of covalent Si-O-Si bonds. This reaction requires a high

[1]Global Foundries, Skywater, Tower/Jazz, and MIT-LL

[2]NHanced, Cactus, Teledyne/Dalsa, IZM Dresden, MIT-LL, Sandia Labs are some examples

thermal budget that is not suitable for the fabrication of many devices. However, modifying the surface chemistry allows the formation of chemical bonds at much lower temperatures. Such surface modification technology has been reported and patented.

One version simply requires a plasma treatment followed by an aqueous ammonium hydroxide rinse. A second method first prepares a metal structure(s) interconnecting to a surface (via) or backside (TSV) metal, then deposits oxide, followed by Chemical-mechanical polishing (CMP) to expose the metal/SiO_2 co-planar surface. This method is a single mask level process if the seed layer used for electroplating is blanket-etched following electroplating. These unit process steps are similar to those used in volume foundry interconnect stack fabrication manufacturing. This method forms the basis of the DBI process.

In the case of copper, special CMP techniques must be used to eliminate the dishing that normally occurs in the soft copper metal in the presence of the hard oxide during CMP. Subsequent heating of the bonded structures in a standard clean room oven forms a monolithic, low resistance metal-metal interface. Typically, a 300°C anneal is used for formation of a low resistance Cu-Cu interface. Since the activated and terminated oxide layers are bonded together with high strength, the M-M interface is subject to sufficient internal pressure so that when the copper expands at elevated temperatures, a reliable metallic bond results, even when the anneal temperature is lower than a standard anneal for Cu. NHanced has produced commercial devices using a maximum processing temperature of 150°C.

NHanced Vertical Interconnect Size and Pitch NHanced's 3D technology stands out from other 3D integration technologies because of its very fine-grained (down to a few micrometers) small pitch vertical interconnect capability. NHanced has assembled devices with more than 10 million vertical interconnects per layer and has demonstrated 3D assemblies with up to 8 device layers. NHanced has developed and fabricated a number of different functional devices using this process. The fabricated devices have passed preliminary qualification, including –65 to +150°C temperature cycling. Most sensor development has been on 180 nm and 130 nm processes, with some work on 65 nm and 55 nm technologies.

3.1.2 Cactus Materials

Rafi, to fix/expand

Cactus Materials is located in Tempe AZ within Macro-Technology Works (MTW) at Arizona State University Research Park. It has office and lab facilities including class 100 cleanroom located in one of the best semiconductor facilities in Arizona originally built by Motorola.

Capabilities Cactus Materials, Inc. has in-house lab for surface activation, wet processing and chemistry, wafer bonding and alignment equipment, and characterization tools. Solvent wet processing, in-situ surface activation in vacuum environment, wafer bonding and alignment, IR interface void characterization will be performed at Cactus.

Cactus Materials, Inc. is 10 mins away from ASU Nanofab where Cactus has direct access to state-of-the-art semiconductor equipment with discounted rate/hr. PI and engineers from Cactus Materials are trained and qualified to run those equipment and process.

ASU Nanofab have STS AGE for plasma system, PECVD, resist coater/spinner/developer, lithography, thickness measurement profilometer and electrical testing and C-V measurement. Cactus Materials. Inc. have access to SEM, TEM, Ion Beam Analysis, Auger Electron Spectroscopy (AES) which will be used to characterize bonding interface at ASU Eyring Materials Center. Cactus

Materials, Inc. has a long term agreement (five years) with ASU Eyring Materials Center (http://le-csss.asu.edu). An agreement can be provided upon request. PI has experience in running TEM. Engineer at Cactus Materials will run SEM at ASU.

4 Foreseen applications for 3D integration

There are a number of currently active 3D R&D projects for High Energy Physics and related fields. These include single-photon avalanche diode 3D integration on CMOS [1] [2], 3D integration of Medipix and Timepix [3], TSV insertion into existing chips, X-Ray imaging [4]. and several others [5] [6]. The Timepix 4 collaboration has recently demonstrated a 4-side buttable chip utilizing TSVs to achieve >99.5% active area in a bump-bonded array [7]. In the following sections we comment a few potential applications in HEP.

4.1 High granularity LGADS

The recent development of silicon diode Low Gain Avalanche Detectors (LGADs) [8,9] has enabled the design of granular (∼1x1 mm^2) fast-timing layers for the ATLAS and CMS tracking systems at the HL-LHC. These systems will allow the determination of the time-of-passage of minimum ionizing particles to a precision of better than 50 ps [10].

The essential design aspects of the LGAD can be described as: a region "p++" with a dopant concentration significantly greater than that of the bulk "p" region. This leads, after depletion, to an electric field large enough to provide amplification (by as much as a factor of 70) through multiplication of the signal. Because of this amplification, the "p" region can be made very thin (50 μm or less), leading to a fast signal and, in turn, precise timing. Several new technologies are being studied to overcome the LGAD granularity limitation. These technologies, when refined, will allow to produce finely segmented LGADs down to less than 50 μm scale maintaining the exceptional time resolution.

The ultimate goal is to provide readout to LGAD sensors with the ability to reach 10um of position resolution and 10ps of time resolution.

4.2 3DIC SIPM

The Silicon Photomultiplier (SIPM) has become a staple phtotodetector for high energy physics, replacing the photomultiplier in many applications. Although inherently a digital device, the current generation of SIPMs rely on analog summing of the micropixels and resistive quenching of the avalanche. A 3DIC version of the SIPM can incorporate much more sophisticated processing including active quenching for each pixel, digital timing and windowing, intermicropixel communication and digital pattern recognition and readout. Such a device can be tailored to the application and can be more selective and much more powerful that the usual analog SIPM. Prototypes are under development by the Pratte group at Sherbrooke University [2].

4.3 Edgeless Tile Arrays

Silicon based sensors can be wafer scale, such as the 8" sensors for the CMS High Granularity Calorimeter but electronic integrated circuits are generally limited by the size of the photomask reticule, typically 2×3 cm or less. This mismatch forces us to engineer complex multi-chip modules where the geometry and functionality of the pixel array is limited by the availability and routing of the external interconnects. The combination of 3D electronics, which provides dense interconnects

and vertical through-silicon readout, with active edge sensors that limit dead regions normally associated with silicon detectors, allow us to build fully active tiles. Tiles would be assembled into an array only after they have been fully tested. The only external interconnect are the backside readout bump bonds that are bonded to the detector motherboard. Tiles can populate complex shapes with near-optimal tiling and low dead area. All fabrication processes are wafer-scale, which lowers the processing costs. An active edge sensor array with dummy readout has been fabricated to demonstrate the concept.

4.4 Small Pixel Induced Current Detectors

3D integration allows for small pixels with minimal capacitance associated with the inter- connect and electronic processing in complex, multi-tier readout integrated circuits. The resulting signal/noise can exceed that provided by LGADs, which typically have much higher load capacitance. The induced current pulse is prompt, with very fast rise time, and, combined with low capacitance, has the potential to provide excellent time resolution [5]. A fast transimpedance amplifier coupled to the small pixel should provide both excellent time and spatial resolution. In addition to the time resolution provided by the central pixel the detector can also utilize the transient currents determined by weighting field coupling to nearby pixels. Shapes of these output signals depend on the geometry of charge motion within the silicon with respect to the electrode location. The signals shapes can be used to provide track angle information and remove off-angle background tracks. The design of such a device can be flexible, a thin detector to optimize radiation hardness, or a thicker detector to provide information on track angle or charge deposition pattern.

4.5 Double Sided and Small Pixel LGADs

The basic concept of the double sided LGAD consists of a double-sided silicon detector with a gain layer on the electron-collecting side and an array of small (3D-integrated) electrodes on the hole-collecting (anode) side [3]. We assume that the detector is thick compared to the anode pitch. The electron-collecting cathode will observe a fast rise-time signal due to the avalanche in the nearby gain layer while the anodes can provide information on the depth and location of the charge deposition. This complementary approach allows us to measure timing with coarse segmentation in the cathodes and therefore lower the total power and complexity for the timing layer. The anode signal shapes reflect an initial peak due to the primary ionization and a secondary peak a few nanoseconds later due to holes generated in the gain layer. We can use the anode signals to either measure total collected charge for position resolution or the current pulse shape to measure the depth of the charge deposition at the pixel position.

4.6 3DIC for high performance Pattern Recognition

High performance pattern recognition capability will become more important in the future. Traditionally, pattern recognition capability has been implemented in either FPGAs or conventional ASIC. Adding a “third” dimension opens up the possibility for new architectures that could significantly enhance pattern recognition capability. The 3DIC based architectures allow massive three dimensional network for data communication with much shorter traces and very low parasitic capacitance, with flexible algorithm cells distributed throughout the network. With this kind of data communication network, pattern recognition become much easier and one could even mimic the detector structure for pattern recognition, such as track finding or particle flow over multiple detector layers using both position information and time of arrival information. The basic algorithm cells could be as simple as Content Address Memory cell for simple matching, or could be as

sophisticated as NN cells to form a high performance NN network. One simple example [4] is using 3DIC as a way to implement associative memory structures for fast track finding applications.

4.7 Zero mass tracker

3D integration of thin sensors with lightweight readout chips would allow to build low (or zero) mass trackers. A zero mass tracker would be extremely useful in many detectors where the preservation of the energy of the particles escaping from the interaction point is very important. The thin layers of detectors/readout, after thinning is foreseeable to have a 50 um sensor (or less) plus a 10 um of electronics per layer. Several thin layers would give a very precise estimation of the interaction point without affecting the energy reading of subsequent sub-detector systems.

4.8 2D Interconnects and Interposers

The size and complexity of substrates (flex, PC board, ceramic) for HEP applications has become a significant limitation on detector design. We often use multi-chip modules to extract signals from front-end sensors, process them and send the resulting signals to the readout [11]. Replacing conventional hybrid circuits with silicon-based ”2.5D” substrates can improve the bandwidth, density and power efficiency of these systems. A silicon-based substrate or interposer (with TSVs), combined with microbump technology connecting the substrate to component ”chiplets” can improve performance by an order of magnitude or more [12]. This can allow for substantially enhanced on-detector processing or overall bandwidth.

4.9 X-rays

This technology would make possible to build stacks of 3D interconnected sensors/readout that can be used for pattern recognition tracking [13] and for X-ray detection applications with thin sensors. For mid-high X-ray detection a fair amount of material is necessary to achieve a reasonable detection efficiency. However a thick enough LGAD would lose all the properties of a thin sensor (good timing, fast repetition rate) and a standard stack of thin LGADs would have a fraction of inactive region. 3D integrated layers of LGAD and readout would have both the fast properties of thin sensors (allowing high repetition rate) and the large active thickness necessary for stopping high energy X-rays.

4.10 Dense active target

The stacks of 3D interconnected sensors/readout mentioned in the previous section could also be applied to the construction of high granularity active targets for particle decay reconstruction. The fast charge collection time allows for great pulse pair resolution, paired with high granularity and low inactive area it would allow to fully reconstruct particle decay chains. Fast high granularity active targets are of great interest, to give an example, for next generation pion and muon decay experiments.

5 Results and ongoing projects

5.1 Latest FNAL results

Ron Lipton Fermilab has had a long history of R&D into 3D integrated circuits. This began with the stringent requirements imposed by the ILC vertex detector. They worked with MIT-LL on

an early ARPA-sponsored 3D prototype run. They then moved to prototypes with Ziptronix and Tezzaron/NHanced utilizing foundry-provided TSVs and an early version of the DBI process. This 3D multiproject run - after a long development cycle and several iterations - yielded functional two-tier chips for ILC, HL-LHC, and X-Ray imaging. These chips were in turn 3D(DBI) chip-to-wafer bonded to silicon sensors - yielding a three-layer stack with readout layers 35 microns thick. This allowed an “apples to apples” comparison of identical ROICs and detectors were assembled with bump and DBI bonds. The DBI bonded assemblies had roughly half (37.7 ± 2 vs 70 ± 10) the noise of the bump bonded set [14] due to the lower interconnect capacitance.

During a following R&D run all three companies involved changed ownership and TSV capability in 130nm was no longer available. This run was never completed. The ASIC priority on the near future is the completion of the LHC upgrades and developments for the neutrino program. Fermilab is continuing to work with MIT-LL, NHanced and others on 3D technologies that could enable processing of fields of pixels using logic, neural networks, or machine learning layers on a 3D processing stack.

5.2 UCSC+Cactus ongoing projects

To expand

The University of California Santa Cruz (USCS) is working in collaboration with CACTUS materials to develop a 3D integration process for high granularity LGADs. The goal is the packaging of AC-LGAD sensors from the FBK RSD2 production with a dummy TSV wafer and prove successful interconnection.

6 Path for future development

The collaboration between partners in laboratories, universities and industry with established expertise in advanced packaging is crucial for the successful introduction of 3D integration in HEP. Such partnership can provide cost-effective implementations of this technology to use in a research setting. A few US based group are pursuing this goal in collaboration with small volume companies listed in section 3. A short description of the ongoing projects and results can be found in section 5.1.

7 Executive summary (1 page)

In the past years HEP experiments have been mostly relying on bump bonding for high density pixel to ASIC connection. The bump bonding technology was proven to be reliable however it is know to have several limitations: it only works down to 20-50 μm of pitch and has yield issues for finer connections. Furthermore the solder balls used for the connection increase the input capacitance to the amplifier and hence the noise. With bump bonding a silicon interposer is needed for planar connections, plus the sensor/chip need side extension to have external connections. In terms of mechanical properties the resulting connection is subject to heat stress since it involves different materials, the minimum thickness is also limited since both chip and sensor need thick enough support wafer.

The introduction of advanced packaging may solve many of these issue, allowing for the improvement of performance, yield and processing. 3D integration is a common widespread technology in industry, it allows tight packaging of sensor and readout chip. Furthermore it allows to stacks multiple chips in a single monolithic device. There are many technologies available for 3D integration,

the direct Bonding Interconnect (DBI) is the most widely accepted: silicon covalent oxide bonding or copper diffusion bonding. The process can be done for wafer to wafer (w2w) or die to wafer (d2w) assembly. Through Silicon Via (TSV) connections allows to have multiple planes stacked and connected with external connections without the need of extensions or silicon interposers. There are several advantages in using 3D integration in sensor to chip connection, a more exhaustive explanation is provided in Section 2:

- Less space: 3D chips can be multi layer and do not need extension or interposers for external connections. Reduction of single layer thickness, after integration all supports can be removed
- Very fine pitch bonding: down to a few micrometers
- Better connections: faster and shorter than in circuit boards, with reduced dissipated power
- Better performance: reduced input capacitance and lower noise
- Layered design: e.g. sensor + analog electronics + digital electronics, each layer can be manufactured by different producers
- Reduced thermal stress and increased heat dissipation since material is homogeneous, also increased robustness

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Advanced packaging and wafer to wafer bonding would facilitate several applications both in HEP and outside of HEP. A full description is provided in Section 4, here a summary list follows: 4D tracking with high granularity LGADs, 3D integrated SiPM with advanced signal processing, chip tile array assembled at wafer level with no edges, small pixels connection (10 um or less) that reduces the input capacitance of thin sensors (e.g. thin LGADs) increasing both space and time precision, double sided connection for LGADs to have readout on both sides, stacked 3D integrated chip, 3D network of algorithm cells for advanced pattern recognition, zero mass trackers with very thin and highly populated layers, sensor stacks for high energy X-ray detection. Finally it will advance the knowledge in substrate engineering, useful, for example, in the fabrication of buried p-n layers for LGADs, necessary for the production of DJ-LGAD and buried junction LGAD.

Therefore 3D electronics and sensor integration provide a variety of technologies that can meet the needs of future particle physics experiments. Combining these capabilities with silicon technologies developed for HEP, such as LGADs and active edge sensors, will allow the design of sophisticated detector systems that can meet the increasing challenges of next generation experiments.

References

[1] T. Al Abbas, N. A. W. Dutton, O. Almer, S. Pellegrini, Y. Henrion, and R. K. Henderson. Backside illuminated spad image sensor with 7.83m pitch in 3d-stacked cmos technology. In *2016 IEEE International Electron Devices Meeting (IEDM)*, pages 8.1.1–8.1.4, 2016.

[2] Edoardo Charbon, Claudio Bruschini, and Myung-Jae Lee. 3d-stacked cmos spad image sensors: Technology and applications. In *2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, pages 1–4, 2018.

[3] Michael Campbell, J. Alozy, Rafael Ballabriga, Erik Fröjdh, Erik Heijne, X. Llopart, T. Poikela, L. Tlustos, Pierpaolo Valerio, and Will Wong. Towards a new generation of pixel detector readout chips. *Journal of Instrumentation*, 11:C01007–C01007, 01 2016.

[4] Farah Fahim et al. Vertically Integrated Edgeless Photon Imaging Camera. 2017.

[5] Miho Yamada, Shun Ono, Yasuo Arai, Ikuo Kurachi, Toru Tsuboyama, Masayuki Ikebe, and Makoto Motoyoshi. 3D Integrated Pixel Sensor with Silicon-on-Insulator Technology for the International Linear Collider Experiment. In *IEEE International 3D Systems Integration Conference*, 10 2019.

[6] Jie Zhang et al. The TSV process in the hybrid pixel detector for the High Energy Photon Source. *Nucl. Instrum. Meth. A*, 980:164425, 2020.

[7] X. Llopart et al. Timepix4, a large area pixel detector readout chip which can be tiled on 4 sides providing sub-200 ps timestamp binning. *JINST*, 17(01):C01044, 2022.

[8] G. Pellegrini et al. Technology developments and first measurements of Low Gain Avalanche Detectors (LGAD) for high energy physics applications. *Nucl. Instrum. Meth.*, A765:12 – 16, 2014.

[9] H. F. W. Sadrozinski et al. Ultra-fast silicon detectors (UFSD). *Nucl. Instrum. Meth.*, A831:18–23, 2016.

[10] ATLAS. Technical Proposal: A High-Granularity Timing Detector for the ATLAS Phase-II Upgrade. Technical Report CERN-LHCC-2018-023. LHCC-P-012, CERN, Geneva, Jun 2018.

[11] M. Kovacs, G. Blanchot, T. Gadek, A. Honma, and A. Koliatos. HDI flexible front-end hybrid prototype for the PS module of the CMS tracker upgrade. *JINST*, 12(02):C02029, 2017.

[12] Saptadeep Pal and Puneet Gupta. Pathfinding for 2.5d interconnect technologies. In *2020 ACM/IEEE International Workshop on System Level Interconnect Prediction (SLIP)*, pages 1–8, 2020.

[13] Ted Liu, Jim Hoff, Grzegorz Deptuch, and Ray Yarema. A new concept of vertically integrated pattern recognition associative memory. *Physics Procedia*, 37:1973 – 1982, 2012. Proceedings of the 2nd International Conference on Technology and Instrumentation in Particle Physics (TIPP 2011).

[14] Ronald Lipton et al. Three Dimensional Integrated Circuits Bonded to Sensors. *PoS*, Vertex2014:045, 2015.