Report of the Production Readiness Review of the DUNE LArASIC

7–8 March 2022
Remote

Outline

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1 Executive Summary

This document is the report of the Production Readiness Review of the DUNE LArASIC which was held remotely on March 7th–8th 2022.
Given that the TSMC 180 nm production line might rapidly become inaccessible, the LArASIC design team has requested the authorization of launching the production of LArASICs version p5b needed for FD1 and FD2 as soon as possible and earlier than anticipated.
The p5 and p5b versions produced together on an engineering run submitted last August meet all DUNE requirements and their integration on the monolithic FEMB has been successful. The performance of the p5b version has been demonstrated to be equivalent to the performance of the p5 version, while its enhanced ESD protection has been demonstrated. There is no evidence at this stage that a design change is needed for LArASIC.
The p5b version is to be used in FD1 and FD2. Producing 250 wafers would cover the needs for equipping both detectors (including spares) with enough safety margin to mitigate all possible risks.
The full QC procedure as well as the hardware and software involved are not yet fully available but all elements are well defined and the design already at an advance state.

The review committee recommends to proceed with the order of 250 wafers with the current reticle as soon as possible.

2 Introduction

After the FDR of the cold electronics ASICs held in July 2021, an engineering run of the LArASIC was launched. The reticle contains the p5 version which had been extensively tested and satisfied the DUNE requirements and the p5b version which includes an enhanced version of the ESD protection. It was expected to have a PRR of the ASICs after the protoDUNE II run.
However, due to the ASIC industry turmoil, brokers and TSMC are starting to restrict access to certain production lines. In particular, that is the case for the technology used for the LArASIC (180nm on 8" wafer). IMEC announced the last "small customer" production orders must be released before September 2022. Although MOSIS did not make similar announcement, there is a high risk this could happen as the global ASIC crisis does not seem to be abating. That is the reason why the LArASIC team would like to order as soon as possible 250 wafers in order to obtain enough LArASICs for FD1, FD2 and spares with a good safety margin.
This order would happen much earlier than initially anticipated (it was foreseen to order the wafers for FD1 in Fall 2022 and the wafers for FD2 in 2023) and hence the full QC procedure, although well-defined and documented, is not yet fully ready.

3 LArASIC performance and FEMB integration tests

3.1 Findings

- The engineering run (6 wafers with the p5 and p5b versions on the reticle) was launched in August 2021. About 1800 packaged chips of each version were received in October 2021.
- 84 p5 chips were tested at room temperature and 55 at LN2 temperature. Respectively 4 and 3 chips had inactive channels, likely due to ESD during manipulation.
- 366 p5b chips were tested at room temperature and 221 (165 standalone chips and 56 mounted on 7 FEMBs) at LN2 temperature. Respectively 2 and 0 chips failed, unlikely due to ESD as the failures did not affect the inputs.
- The enhancement of the ESD protection of the p5b was confirmed with measurements (in addition to the fact that no ESD failures were observed during testing and FEMB assembly process).

- The design has been done to limit the hot carrier effect and a previous version of the LArASIC have been used in Microboone (7 years) and protoDUNE I (2 years) without degradation of performance. Specific lifetime studies are going to be done with version p5b. The setup for the 5b specific test is not yet ready but a p5 version has been running for 300 hours in LN2 with a 3V power supply (far above the nominal 1.8V) without observable change, which is very encouraging from the point of view of lifetime.
- Measurements with a first version of the monolithic FEMB housing p5 version of the LArASIC have shown that the DUNE requirements are fully satisfied and the performance of the p5b has been demonstrated to be equivalent to the p5.
    - The linearity measurements show slightly better performance when the single ended connection between the LArASIC and the COLDADC is used instead of the differential connection. It is within requirements for both schemes.
    - Less than 0.1% cross-talk performance is observed with both single ended and differential connections between the LArASIC and the COLDADC but slightly better with the differential connection.
    - Although the single ended connection is preferred (better linearity and lower power consumption at the expense of slightly worse cross-talk) no decision needs to be taken now as this is configurable on the FEMB.
- The final design of the FEMB is now available and 7 boards have been assembled with the p5b version LArASIC and the latest versions of COLDADC and COLDATA (chips from the 2021 engineering run). These boards were successfully tested. The enhanced ESD protection of the LArASIC p5b does not introduce any excess noise.
- 128 FEMBs are going to be produced for protoDUNEII requiring 1200 LArASIC p5b. A QC test stand is available and a subset of the future DUNE LArASIC QC will be applied.

3.2 Comments

- LArASIC p5 and p5b meet all DUNE requirements and their integration on the monolithic FEMB has been successful.
- The ESD improvement of p5b is effective as demonstrated by measurements and by the fact that no ESD issue was observed during testing of chips and assembly on FEMB. In addition, this new ESD protection does not introduce any increase in noise.
- There is no evidence at this stage that a design change is needed for LArASIC.
- Lifetime tests in LN2 needs to be further pursued and completed, though lifetime studies done to date show no evidence of aging.
- The current reticle, developed for engineering run, contains both p5 and p5b ASIC versions. It is more cost effective to use this mask set to launch production rather than creating a new mask with only p5b.

3.3 Recommendations

R1. Use the current reticle for launching production.

R2. Set up and conduct a lifetime test in LN2 either with chips or with an FEMB board. This recommendation can be completed after the wafers order is released.

4 LArASIC procurement plan

4.1 Findings

- FD1 and FD2 require 4920 FEMBs, to which 500 spare boards (~10%) are to be added. 43360 good LArASIC p5b are hence needed.

- It is expected to have a 90% yield for the production of LArASIC based on the limited amount of chips tested so far. An 80% yield is assumed to be safe. Hence 54200 LArASICs are to be produced.
- Each wafer contains 310 LArASIC p5b (and 310 LArASIC p5), leading to 175 wafers to be produced, i.e. 7 lots of 25 wafers.
- Given that the 180 nm production line might rapidly become inaccessible, and to further mitigate additional risks, it is requested to order 3 additional lots for a total of 250 wafers.
- The exact schedule of production is not known yet, but it is likely that TSMC will deliver the wafers lot by lot.
- Similarly, the packaging schedule is not known.
- Each chip has its own unique identification number (added on the package by the packaging company) which includes the lot number, meaning the yield per lot can always be monitored.

4.2 Comments

- Even though the production yield measured so far is good, it is safe to foresee a large safety margin as one could have unexpected lot-to-lot variations during the wafer production, unexpected bad batches of FEMB and losses at different stages (dicing, packaging, shipping, testing and assembly).
- The best schedule for packaging would be to have the lots packaged as they are delivered so that the production yield can be timely monitored but it is also possible that the packaging company want to package the full quantity in one go.

4.3 Recommendations

R3. Proceed to order 10 LArASIC wafer lots, 25 wafers/lot for a total of 250 wafers.
R4. Work out the delivery schedule with TSMC.
R5. Work out the packaging schedule and strongly consider getting the packaging done on a lot basis.
R6. Strengthen and document the narrative to properly justify the yields, risks and therefore the required number of procured lots.

5 LArASIC QC Plan

5.1 Findings

- In a first step, a limited number of LArASIC p5b will be fully characterized. Based on this characterization two sets of QC parameters will be defined in order to accept or reject a chip. One is for “reference chips” to be done on a limited number of chips and one for production QC. 14 tests are defined for the former out of which 6 and a subset of 5 will be executed for production QC.
- Considering a 60-minute thermal cycle, < 10-minute testing time per chip is deemed acceptable by the LArASIC team.
- As recommended during the FDR, the possibility of skipping the testing of the ASICs at LN2 temperature is considered. Only FEMBs would be cold testing (this is mandatory) and this is acceptable (i.e. it does not require too much rework of FEMBs) if the fraction of chips passing tests at room temperature and failing at LN2 temperature is lower than 10%.
- A reliable and easy-handle QC test stand, as well as a clear and routinely QC testing procedure including routine examination of the QC plans and test results, are to be made available to the different test sites.

- A unified test board for testing 8 LArASIC or 8 COLDADC or 2 COLDATA at room or LN2 temperature is being designed. A robotic system is being developed for having an automatic insertion of the chips in the sockets. Sockets will be on mezzanines for an easy maintenance.
- Most of the software is already available. The tests results will be stored in a data base being set up in MSU.
- The complete QC stations are expected during the Fall.
- A number of QC documents and procedure descriptions are already available.

5.2 Comments

- As mentioned in the introduction, the QC procedures are not expected to be fully ready prior to launching early production. Hence recommendations given here do not have to be completed before the wafers order is released.
- As there were issues in the past with ESD damages, documenting exhaustively the way the chips and boards are to be handled is necessary. This has already started and needs to be developed further.
- It is considered to have a specific test for controlling the uniformity of the calibration capacities.
- TSMC can provide fabrication QC data. These data could be useful in case of unexpected yield variations for instance. They should be requested and added the LArASIC QC record.
- CERN has used external testing companies for production testing of chips. In some cases, everything was delivered by the testing company. In other cases, both hardware and software were delivered by CERN and the company took care of the robotic aspect and of handling of the chips. Such an option saves time as the company run 24/24 and could still be considered especially if only testing at room temperature is considered.

5.3 Recommendations

These recommendations can be completed after the wafers order is released but before the packaged chips are delivered.

R7. Complete and document the detailed QC procedures.
R8. Complete the design and production of the QC stations.
R9. Review the handling procedure of ASICs/FEMBs to minimize ESD; update and document procedures accordingly.

6 Answers to Charge questions

1) Is the team ready to procure the full complement of LArASIC chips before the end of production at TSMC?

a) Have they demonstrated that the performance of the P5 and P5B chips matches design expectations and meets all DUNE requirements based on measurements taken with standalone chips and chips mounted on front-end motherboards, both at room temperature and in LN2?

b) Have they demonstrated that the additional protections against ESD damage on the P5B chips decrease the sensitivity of the LArASIC chip to electrostatic discharges while not degrading its performance?

c) Do measurements of chip yields from the engineering run support estimates for the minimum number of wafers required to populate the FEMBs for FD1 and FD2 within a comfortable safety margin?

d) Do these measurements indicate that the reticle used for the engineering run and the masks obtained from that reticle are adequate for the proposed production run?

Yes, the team is ready to procure the full complement of LArASIC now.

The results of standalone and FEMB tests with P5 and P5B match expectations and meet DUNE requirements both at room and LN2 temperature.

The enhanced ESD protection of LArASIC p5b has been demonstrated with measurements and with the fact that no ESD damage occurred during the testing of chips and the assembly of FEMBs. In addition, it has been demonstrated that this enhanced ESD protection does not introduce any excess noise.

The yield obtained after the testing of a few 100's chips of the engineering run is better than 90%. A conservative but necessary safety margin to account and mitigate for risks has been applied to reach the 250 wafers to be ordered.

The chips as produced during the engineering run are fully satisfactory. The reticle contains both p5 and p5b versions. Only p5b is to be used, but making a new reticle and new masks would require a new engineering run and its qualification which is costly and not wise in term of schedule.

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2) *Are the order specifications well-determined? Is the cost and production schedule understood?*

Yes, the order is well defined (same masks as for the engineering run to be used) and a quotation from TSMC is available. The production schedule still requires some clarifications (delivery schedule of wafer lots, packaging of lots, …) which will be worked out in due course.

3) *Is there an adequate plan for procurement and fabrication oversight?*
   a) *Are the details of the required Purchase Order (PO) for MOSIS/TSMC understood and can the PO be ready to submit on the needed time scale?*
   b) *Have any special concerns associated with large-scale production been adequately addressed?*

Assuming the authorization is obtained to procure the 250 wafers with DUNE project fund at BNL, the PO can be submitted from BNL.
Prepayment and single source justification are in place with BNL procurement system from the past multi-project wafer and engineering run submissions.

4) *Is it likely that an appropriate post-production QC plan for the LArASIC chips can be finalized?*

The team has extensive experience with chip QC from ProtoDUNE-1. QC for the ASICs from engineering run is ongoing and plans for the production ASICs QC are fully defined. The team has still to complete the test stations production, the detailed procedures documentation, the software and the storage of the results in a data-base but this is already well advanced and everything should be completed when the first production chips are delivered.

7 Summary and final conclusions

The LArASIC design team is to be commended for the quality of their work and the performances of the p5b version.

The review committee recommends the order of 250 wafers with the current reticle is released as soon as possible. In view of the long experience gained with the previous version of the LArASIC, there is no evidence that waiting for more tests (e.g. protoDUNE II run) will show problems to be fixed in this ASIC and enough handles are still in hand with the FEMB design to correct subtle issues which could

appear. Waiting for protoDUNE II could be problematic for the access to the 180nm technology and another iteration would impact the schedule by a year.

The list of recommendations is listed below with ***the indication of when they are to be completed***.

R1. Use the current reticle for launching production. ***Now***
R2. Set up and conduct a lifetime test in LN2 either with chips or with an FEMB board. ***Now for the setting up, but the test is can be completed after the wafers order is released***
R3. Proceed to order 10 LArASIC wafer lots, 25 wafers/lot for a total of 250 wafers. ***Now***
R4. Work out the delivery schedule with TSMC. ***Now***
R5. Work out the packaging schedule and strongly consider getting the packaging done on a lot basis. ***Before the wafers are delivered***
R6. Strengthen and document the narrative to properly justify the yields, risks and therefore the required number of procured lots. ***Now***
R7. Complete and document the detailed QC procedures. ***Before the chips are delivered***
R8. Complete the design and production of the QC stations. ***Preferably before the chips are delivered***
R9. Review the handling procedure of ASICs/FEMBs to minimize ESD; update and document procedures accordingly. ***Before the chips are delivered***

A. Review Charge

The committee is requested to review the readiness of the DUNE LArASIC chip for production and determine if it meets the requirements of production readiness as outlined in the LBNF/DUNE Review Plan (edms-2173197) supported by the DUNE Far Detector PRR deliverables outlined in (edms-2493568). Based on the documentation to be posted in edms-2314428, the committee should provide answers to the following questions:

1. Is the team ready to procure the full complement of LArASIC chips before the end of production at TSMC?
    a. Have they demonstrated that the performance of the P5 and P5B chips matches design expectations and meets all DUNE requirements based on measurements taken with standalone chips and chips mounted on front-end motherboards, both at room temperature and in LN2?
    b. Have they demonstrated that the additional protections against ESD damage on the P5B chips decrease the sensitivity of the LArASIC chip to electrostatic discharges while not degrading its performance?
    c. Do measurements of chip yields from the engineering run support estimates for the minimum number of wafers required to populate the FEMBs for FD1 and FD2 within a comfortable safety margin?
    d. Do these measurements indicate that the reticle used for the engineering run and the masks obtained from that reticle are adequate for the proposed production run?
2. Are the order specifications well-determined? Is the cost and production schedule understood?
3. Is there an adequate plan for procurement and fabrication oversight?
    a. Are the details of the required Purchase Order (PO) for MOSIS/TSMC understood and can the PO be ready to submit on the needed time scale?
    b. Have any special concerns associated with large-scale production been adequately addressed?
4. Is it likely that an appropriate post-production QC plan for the LArASIC chips can be finalized?

Review Findings:
The committee should present its findings, comments and recommendations in a final written report by March 15.

B. Review Committee

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C. Review Agenda

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