Answers to Committee's Questions for the Q/A Session

LArASIC Production Readiness Review

7-8 March 2022

Question 1. We would like to get clear numbers (see list below) to better understand the number of wafers to be ordered:

a) Total number of FEMB for FD1 = 3000
b) Total number of FEMB for FD2 =1920
c) Total number of spare FEMB = 500 (assume ~10% spare)
d) Sum of a)+b)+c) = 5420

e) Number of P5B LArASICs per FEMB = 8

f) Total number of LArASICs for FD1 required (+ spares) = 26400
g) Expected total yield of LArASICs for FD1 = >90%
h) Total number of LArASICs required for FD1 = 29400

i) Total number of LArASICs for FD2 required (+ spares)= 16900
j) Expected total yield of LArASICs for FD2 = >90%
k) Total number of LArASICS required for FD2 = 18800

l) Total number of LArASICS required for FD1 + FD2 including yield + spares = 48200

Question 1 (continued):

What is the basis of justification for the expected yield?

A yield of ~90 to 95% is typically expected from a good wafer run. Based on a small sample of chips cold tested from the engineering run, we believe the yield should be in this range

What is the risk that the yield will be smaller than the expected yield?

The yield could be lower than due to various reasons (packaging issues, mishandling during QC, shipping mishaps, etc.). The risk level is moderate. A conservative estimate of the yield factoring risks is ~80%

What is therefore a good assumption for the yield to account for the risk for g) and j)? 80%

Therefore, recalculate the total number of LArASICs that is needed? 54200

Number of LArASICs per wafer with the current mask set? 310

Total number of wafers needed = 175

Total number of Wafers Produced = 250

Given that we may not have access to the 180 nm production line later, a total of 250 wafers are requested to provide additional safety margin

Question 3. The wafers will be produced in lots of 25 wafers. Is there a schedule for the lots delivery (i.e. one per montn, …)? Is it expected to dice package and test the lots one by one (with the advantage of being able to control the yield of the production and possibly react in case of problems), or to have the testing and the delivery somehow uncorrelated?

- There is no schedule for the lots delivery yet before the PO is placed, besides
  - Fabrication will likely be done in multiple lots
  - Wafers will likely be delivered in batches from TSMC
  - This is expected given 250 wafers is counted < 0.03% of TSMC Fab6 annual production capacity
- Details of the production packaging and test plan to be worked out
  - Ideally this should be organized lots by lots to track the yield as suggested
  - Practically ASE may ignore this request given packaging vendors are busier than foundries, e.g. bPOL12V packaging delayed by ASE by 6+ months
  - We will work with ASE towards a scheme with the possibility to track the lots

Question 4. What is the expected date for releasing the order? Could the time until this date be used to run a number (how many?) of assembled FEMB's in LN2?

- Assuming green light is granted from PRR committee in mid March
  - Finance of this procurement is being worked out with DOE, should be clarified then
  - PO will be submitted in mid March, and be released by mid May
- Production assembly and test of ProtoDUNE-II FEMBs are ongoing now
  - We expect to have enough FEMBs for 2 APAs fully assembled, tested and shipped to CERN by early May
  - ~50 FEMBs will tested in LN2 before the PO is released to MOSIS/TSMC

Question 5. Could we have the detail of the time needed to test the chips at room temperature and at LN2 temperature including time to populate the boxes?

- Based on test results of the current dual-DUT test board, to perform test items listed on the slide#14 of LArASIC performance talk
  - It takes about 7 minutes to test a chip, most time is consumed by the inefficiency of test script which can be further optimized
  - The time for cold test is same as room temperature. However, the cool-down and warm-up of CTS take 60~90 minutes
  - To manually place a chip in the ASIC socket, it takes less than one minute per chip

Question 6. It was said there is a document about handling of wafers and chips, in particular to prevent ESD damages. Is it possible to present this document?

- A few procedures have been developed during the ProtoDUNE-I and SBND cold electronics productions, to describe the handling instructions and minimize the ESD damage
- The instructions include key statements below, and will be used as basis to formalize the procedure for DUNE QC document
  - Wear anti-static wrist strap (or similar equipment) while handing the boards
  - All instruments are well grounded
- Extra ESD protection measures, as suggested by PRR committee, will be included in the procedure for DUNE ASIC QC document

Requirements for the assembly house:

Extra ESD protection requirement for SBND AM.v1.pdf

Extra ESD protection requirements for AA-tech

1. **Baking is required before assembly**

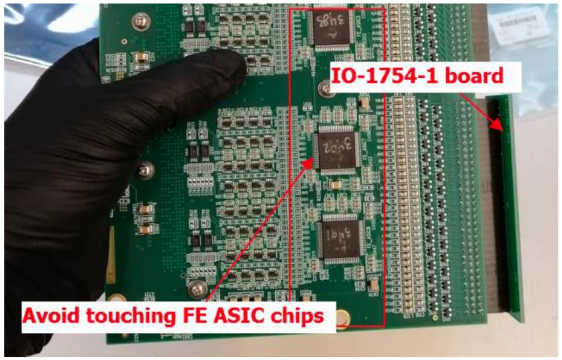
The FE ASICs belong to MSL level 3, so they need to **be baked for 12 hours at 125 ± 5 °C before assembly**, please refer to IPC/JEDEC J-STD-033 for bake procedure

2. **Plug IO-1754-1 board into connector SSW-132-21-G-T before installing them**

Keep IO-1754-1 boards always in SSW-132, don't remove them.

3. **Please wear anti-static wrist strap (or similar equipment) while handling the boards. Please make sure all instruments are well grounded.**

It is suggested to avoid touching FE-ASIC chips, try to hold the board as shown in picture below.



Requirements for the CE installation at CERN

The CE Installation and Check-out Procedure for APA. pdf

REMINDER: Wearing static wrist band is required

Barrack:

Preparation:Use spare FEMB board to set up WIB test bench.

1. Install PSL terminator boards for each CE box **before** Augie installs the cables.
2. Install PS and data cables for CE boxes (Augie)
   a. The warm end of cold cables should have terminator board. If doesn't, please plug in terminator board before install cables to CE boxes.
3. Set up WIB test bench test stand in Barrack
   a. WIB PS = 12 V
   b. WIB should not connected to PTB board
   c. WIB with adapter board
   d. Check current without FEMB (should be < 1.5A)
4. Check-out test after cable installation (**static wrist band**)
   a. Turn WIB bench test stand off
   b. Remover cable terminator boards, plug cold cables to WIB adapter slot0 (first slot)
      i. Power Cable and then data cable
   c. Remove PSL terminator boards

Reception_CHKOUT_Guide.pdf for SBND CE

2.2 Setup Procedures

1. **ESD Protection Warning**: Please make sure you wear anti-static wrist strip while touching any boards.
2. Measure PS output, make sure it output 12V current, set current limit to 5A.

9. Add a FEMB to WIB
   a. **Wear Anti-static wrist strip**, please avoid touch FE area if you are not wearing the gloves (sweat may contaminate FE chips)

   c. Plug FE input short boards from the FEMB

   d. Put FEMB into the anti-static bag and then the bubble bag

11. Turn PS off when you finish or before you leave, don't leave WIB on when there is no one present.

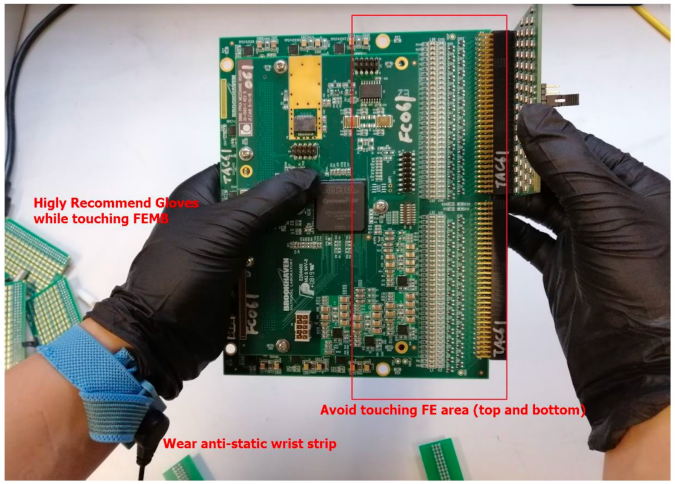


Figure 2 How to handle FEMB

Figure 3 Plug or Unplug FE short board

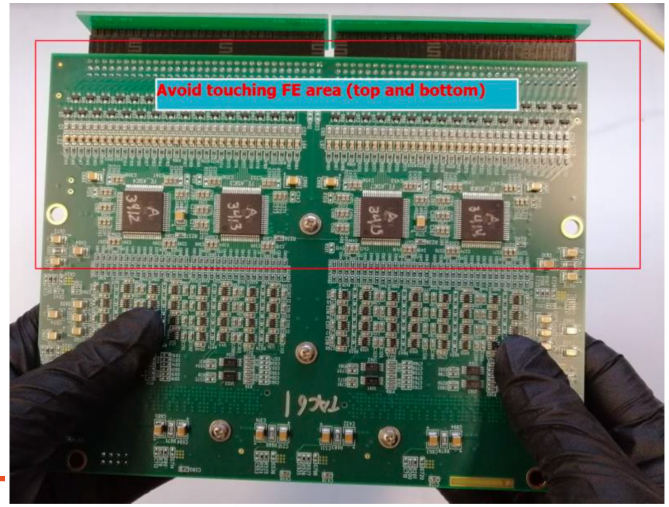


Figure 4 Avoid touching FE area (both top and bottom)

Question 7. P5b has an enhanced ESD protection. Would not it be useful to check on a few P5b per wafer that the leakage current remains at or below expectation given the 30X ESD increase in size at the input

- Extensive leakage current measurements have been made on P5 and P5A (with 1x, 5x, 15x and 30x ESD options) with SMU (source measure unit), and reported in FDR
  - https://indico.fnal.gov/event/49771/contributions/219885/attachments/145373/185066/LArASIC_FDR_Review_07212021_v3.pdf
  - Leakage current is also used to assess and confirm the ESD damage
- Leakage current was checked on P5B as well with SMU
  - Leakage current is also used to assess and confirm the ESD damage
  - The measured leakage current is close to the programmable leakage current (100pA, 500pA, 1nA and 5nA) when the channel is alive
  - There is no significant leakage current difference with the 30x ESD compared to 1x ESD

Question 8. There is no mention of testing the LArASIC in both single ended and differential mode. Although the single ended option is preferred in the current plan, is it planned to test the differential mode in production testing? If not, could you give the reason why?

- The test results were summarized and presented in the TPC electronics consortium meeting on 08/23/2021
  - Only conclusion was presented for LArASIC PRR yesterday
  - Slide#21 to slide#31 presented in https://indico.fnal.gov/event/50615/ summarized the FEMB performance with both single-ended and different modes
- The final choice of mode hasn't been decided yet, so both single-ended and differential modes will be tested in the production test for ProtoDUNE-II
  - Example summary reports of an LArASIC QC test with the dual-DUT test board are attached
  - Both power consumption and pulse response in the differential mode are tested
  - The decision will likely be made based on ProtoDUNE-II operation