Summary and Discussion

Cheng-Ju Lin
Lawrence Berkeley National Lab

LArASIC Production Readiness Review
7-8 March 2022

Charge 1a): Have they demonstrated that the performance of the P5 and P5B chips matches design expectations and meets all DUNE requirements based on measurements taken with standalone chips and chips mounted on FEMB, both at RT and LN2?

Results of standalone and FEMB testings with P5 and P5B match expectations and meet requirements

"*LArASIC performance and FEMB integration tests*" (S. Gao):

- Page 6: summary with P5
- Page 12-13: lifetime study
- Page 19-22: FEMB with P5B

Charge 1b): Have they demonstrated that the additional protections against ESD damage on the P5B chips decrease the sensitivity of the LArASIC chip to ESD while not degrading its performance

We believe the answer is YES!

"*LArASIC performance and FEMB integration tests*" (S. Gao):

- Page 10-11: ESD study with P5B
- See previous slide for P5B performance information

Charge 1c): Do measurements of chip yields from the engineering run support estimates for the minimum number of wafers required to populate FEMBs for FD1 and FD2 with in a comfortable safety margin

P5B yield based on a sample of ~200 chips tested in LN2 is > 98% (including packaging). The chip yield can be as low as 60% and we will still have enough P5B for FD1 and FD2

"*LArASIC performance and FEMB integration tests*" (S. Gao):

- Page 16: P5 and P5B yield from engineering run

"*FE ASIC procurement plan*" (H. Chen):

- Page 5: answer to the charge question

Charge 1d): Do these measurements indicate that the reticle used for the engineering run and the masks obtained from that reticle are adequate for the proposed production run?

"FE ASIC procurement plan" (H. Chen):

- Page 6: answer to the charge question

Link to LArASIC Reticle (MOSIS):

- https://edms.cern.ch/file/2314428/LATEST/MOSIS_Reticle.pdf

More information in the provided document on *"ASICs Production and QC Plan ver2"* (EDMS#2604783) : page 4-5

Charge 2): Are the order specifications well-determined? Is the cost and production schedule understood?

Charge 3a): Are the details of the required Purchase Order (PO) for MOSIS/TSMC understood and can the PO be ready to submit on the needed time scale?

Charge 3b): Have any special concerns associated with large-scale production been adequately addressed? Do these measurements indicate that the reticle used for the engineering run and the masks obtained from that reticle are adequate for the proposed production run?

See talk "*FE ASIC procurement plan*" (H. Chen):

- Page 8-9 address the charge questions

Charge 4): Is it likely that an appropriate post-production QC plan for the LArASIC chips can be finalized?

We have extensive experience with chip QC from ProtoDUNE-1. QC for the ASICs from engineering run is ongoing. For the production ASICs, we will scale up QC with the multi-chip test-board.

- See talk "*LArASIC QC Plan*" (S. Gao)
- More information in the provided document on *"ASICs Production and QC Plan ver2"* (EDMS#2604783)

Tomorrow (8-March):

- Q&A session starts at 9am CST (4pm CET)
  Same public Zoom link as today

- Executive Session after Q&A
  Same Executive Session Zoom link as today

Thank you for taking time to serve on the ASIC PRR Committee

Your assessments and recommendations are important to us

Questions and comments?