DUNE PRR: TPC Electronics ASIC
LArASIC QC Plan

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LArASIC QC experience in ProtoDUNE-SP/SBND

- P2 version of LArASIC
  - FE ASIC chips for APA1 to APA5 passed QC test at RT
    - 1,850 chips tested at warm
      - Rejected ~113 (5.6%) with warm selection cuts
        - including “fake” failure caused by mishandling or worn-out socket
  - FE ASIC chips for APA6/APA7/ICEBERG/SBND
    - 1,561 FE chips went through cold screening test. **Overall yield is > 90%.**
  - ProtoDUNE operation
    - 99.74% (15,320 of 15,360) of TPC channels are active
      - 4 inactive cold electronics channels when commissioning started
      - 2 more inactive cold electronics after >1 year running
      - We confirmed these 6 inactive channels were damaged by discharge after ProtoDUNE-SP demolition

Failure Mode at LN2	# of chip	Note
Baseline out of range	4	P5B fixed the baseline distortion
Power cycle failure (start-up issue)	23	P5B fixed the start-up issue
Input pin dead to external pulse	28	P5B has enhanced 30x ESD design
Other failures (socket issues or other errors)	86	
Total failures at LN2	141	

We should expect much higher yield with P5B LArASIC

LArASIC P5/P5B: Yield

- Dual-DUT test board has been used to test LArASIC P5/P5B chips
  - The second and third test stands for LArASIC are being prepared
  - Test ~20 chips with 2 CTS per day

LArASIC Version	Temp.	Tested Chips#	Good #	Yield
P5	RT	55 (old packaging batch)	55	100 %
P5	RT	84 (new packaging batch)	80	~95.23 %
P5	Cold/LN2	60	57	~95 %
P5 (ENG Run)	RT	49	49	100%
P5B (ENG Run)	**RT**	**366**	**364**	**99.4 %**
P5B(ENG Run)	**Cold/LN2**	**165 + 56***	**165 + 56***	**100 %**

- P5
  - At RT: 4 chips with inactive input channels (likely caused by ESD discharge before testing)
  - At LN2: 3 chips with inactive input channels (permanent damage caused by ESD discharge over handing)
- **P5B (ENG RUN)**
  - At RT: 2 chips were likely caused by manufacture defects
    - Fail mode of chip#198: ch6 no response, outputs 0V with DC coupling
    - Fail mode of chip#269: Control register for ch15 works can't config ch15 properly
  - AT LN2
    - 165 chips were tested by dual-DUT test board
    - 56 chips were tested on 7 FEMB boards. These 56 chips only passed the warm test before assembly

Dual-DUT test board and MSU CTS

LArASIC Documentation

LArASIC Documentation	2314428	LArASIC_P5_Datasheet_V1.pdf	Datasheet for version P5 of LArASIC. Includes expected performance from simulation.
		LArASIC_P5A_Datasheet_V1.pdf	Datasheet for version P5A of LArASIC. Version P5A is identical to version P5 except that it includes different combinations of ESD protections and RQI subtraction (channel dependent), as discussed on pages 4 and 5 (otherwise the two documents are identical)
		LArASIC_P5B_Datasheet_V1.pdf	Datasheet for version P5B of LArASIC. Version P5B is identical to version P5 except that it includes minor modifications (improved input ESD, S16 global bit toggle, as discussed on page 3
		LArASICDevelopment.docx (document updated 7/14, added appendix on ESD protection and Reset Quiescent Current)	This document starts with the measurements performed on the P4 version of LArASIC, followed by the design changes that were implemented as a consequence in the P5 version, as well as the tests done in a parallel development (P5A) to improve the ESD protection and try to understand the issues related to RQI subtraction. The document ends with the measurements of the P5/P5A performance, and with a proposal for the reticle for the engineering run of LArASIC.
		P5LArASICDesignSimulation.pdf (document added 7/14)	Design and simulation of the single ended to differential buffer.

Summary of requirements on ASICs	2397298	ASIC_Requirements_v3.docx	Summary list of the requirements affecting the DUNE ASICs
Preliminary Manufacturing and Procurement Plan and Preliminary QC Plan	2604783	2604783_ASIC_Production_QC (need to update the document to add sections on cost estimates and more details on the schedules)	Document describing the production plans and the preliminary quality control procedures for the ASICs. This includes a detailed description of the measurements to be performed as well as a conceptual design of the test equipment.

LArASIC for DUNE-FD1 and FD2

- Designed to operate in liquid Argon (87K)
  - Appropriate design rules for operation in cryogenic liquids are used to ensure LArASIC will operate with minimal losses of channels throughout the expected lifetime of the DUNE experiment (~30 years)
  - FEMBs in cryostat (liquid Argon) is not accessible for repair or replacement
- Total ~43,300 packaged chips in need
  - 24,000 LArASIC for DUNE-FD1-HD
  - 15,360 LArASIC for DUNE-FD2-VD BDE
  - 10% spares
- Assuming 90% yield of the packaged chip
  - This yield includes warm screening, screening in LN2, installation on FEMBs, FEMB quality control at room temperature, FEMB quality control in LN2
  - **Total ~48,100 packaged chips to be tested**
    - The TPC electronics consortium plan involves having multiple sites using the same QC procedure.
    - The plan assume each chip passing warm test will be tested at LN2 to assure the cold yield

Performance Characterization vs. QC Testing

- Performance Characterization
  - has the ASIC met all the functionality requirement?
  - explore the optimal configuration for the ASIC
  - investigate potential design/manufacture defects
  - focus on a small batch of chips
    - functionality and performance are thoroughly studied
  - a golden reference for QC is determined during the performance characterization
- QC testing
  - **Develop a criteria to screen the ASIC chip after LArASIC is completely characterize**d
    - Normally, it is not necessary to get the optimal performance during QC. It is more important to gain the consistent performance for majority of chips.
  - Most failure modes have been identified during the performance characterization
    - There could be few failure modes later recognized during the early stage of the QC activity
    - Performance characterization and QC can't assure all potential failure modes are addressed
  - Result of QC testing
    - **PASS**: the chip passes the pre-defined tests, achieve the performance consistent with the golden reference
      - Possible criteria: cut ASICs with any of those values >3(?) sigma from channel expected response
    - **FAIL**:
      - A pre-defined failure mode is observed
      - Its performance is out of tolerance range compared to the reference chip
  - Reliable and easy-handle QC test stand, clear and routinely QC testing procedure
    - A non-expert with a couple of hours training should be able to perform the QC testing
    - QC test stand and the test procedure should be able to prevent an operator from making mistake
      - The test should be automatically performed once the chip is installed in the socket
    - Considering 60-minute thermal cycle, < 10-minute testing time per chip is acceptable

Strategy for the ASIC cold screening

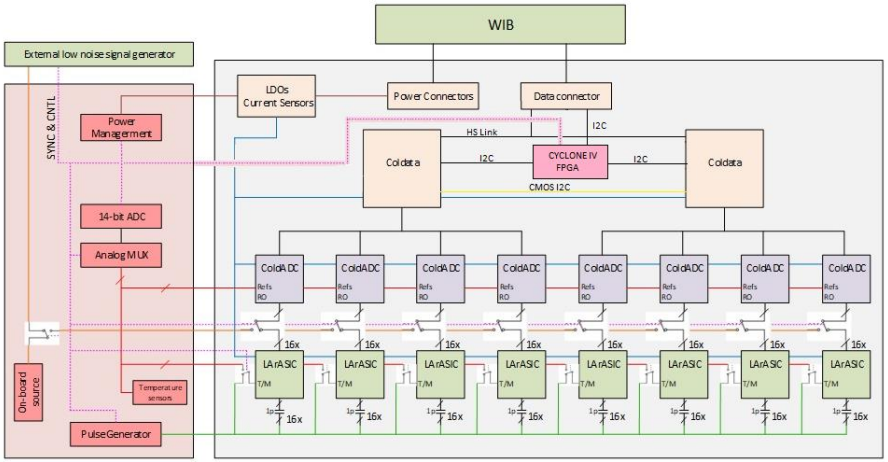
- Warm QC Screening is necessary
  - QC test at room temperature removes chips with manufacture defects
  - Hardware test setup is easy to extend, easy to operate, and reliable
    - Much less ASIC socket worn-out compared to “Cold” Test
    - Require less resources, such as manpower or cost
- The cold screening test is not reliable enough for high-yield ASIC chips
    - Chip socket is easy to worn-out at cold
    - Cooldown may cause misalignment between chip’s pins to socket’s pads
    - “False” cold test result is foreseeable high
- **Can we skip/minimize the ASIC cold QC screening?**
  - The ASIC QC plan keeps the assumption that there is a cold yield required to perform cold QC test for each ASIC.
  - Because the cold screening of FEMB boards is unavoidable, **if the cold yield is high enough**, a small portion (5~10%) of ASIC will be tested at cold instead of all chips.
    - The ASIC cold failure is a negligible contribution on the yield of FEMB boards
    - The current on-going LArASIC QC for ProtoDUNE-II will provide the statistics result to answer this question.
- All test sites should use the same hardware test setups calibrated by golden reference chips
  - Robotic chip handing system would be helpful to avoid manual handing uncertainty
- QC data storage
  - Test result will be uploaded to the central hardware database
  - Raw data and test result will be backed up locally.

LArASIC QC Items

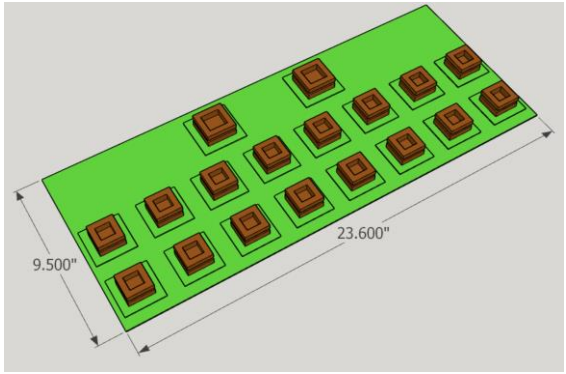
Test Item	Description	Reference chips	Chips for QC	FEMB QC
Power Consumption	Measure the power consumption on the three rails of LArASIC (VDDP, VDDA, VDDO), for each of six configurations (two baseline references: 200 mV and 900 mV; three configurations of the output buffer: bypassed, single ended, differential)	Required	Required	No
Power Cycling	a number (>5) power on/off cycles, measure the pulse response with a certain configuration (e.g., 14mV/fC, gain, 2.0us peak time, 200mV baseline, 500pA leakage current)	Required	Required	Required
Register configuration	check through SPI interface for register configuration W/R	Required	Required	Required
Bandgap	Measure the bandgap reference voltage	Required	Required	Required
Temperature sensor	Measure the voltage of embedded temperature sensor	Required	Required	Required
Channel response monitoring	Check response of each channel through the monitor pin	Required	Required	Required
Internal DAC measurement	measure INL/DNL of 6-bit DAC (4 ranges for 4 gains)	Required	subset	subset
baseline measurement through monitoring pin	Measure baseline through the monitoring pin (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	subset
baseline measurement	Measure baseline with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	subset
Noise measurement	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents). A reference capacitive load of ~150 pF at the inputs.	Required	subset	subset
Calibration with internal-DAC	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	subset	subset
Calibration with external precise source	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	No	No
Crosstalk	Measure with ColdADC (1 gains x 4 peak times)	Required	No	No
Internal calibration capacitor measurement	Measure the capacitance of the calibration capacitor	Required	No	No

Hardware: DUNE ASIC Test Board (DAT)

- DUNE ASIC Test (DAT) Board
  - Unified ASIC test board for LArASIC, ColdADC, and COLDATA QC
    - Compatible power and data interface with WIB. It acts as exactly as a FEMB to WIB
    - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
    - Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites
  - A single big board solution with ASIC socket mezzanines
    - ASIC socket suffers mechanical degradation through thermal cycling
    - More commercial semiconductor devices have been identified for cryogenic operation
      - Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ
  - Unified ASICs and FEMB QC with the same SW set
    - Can benefit directly from the WIB, back-end DAQ, **analysis software developments**
    - Some extra software effort for ASIC QC can be implemented as a widget to the available software

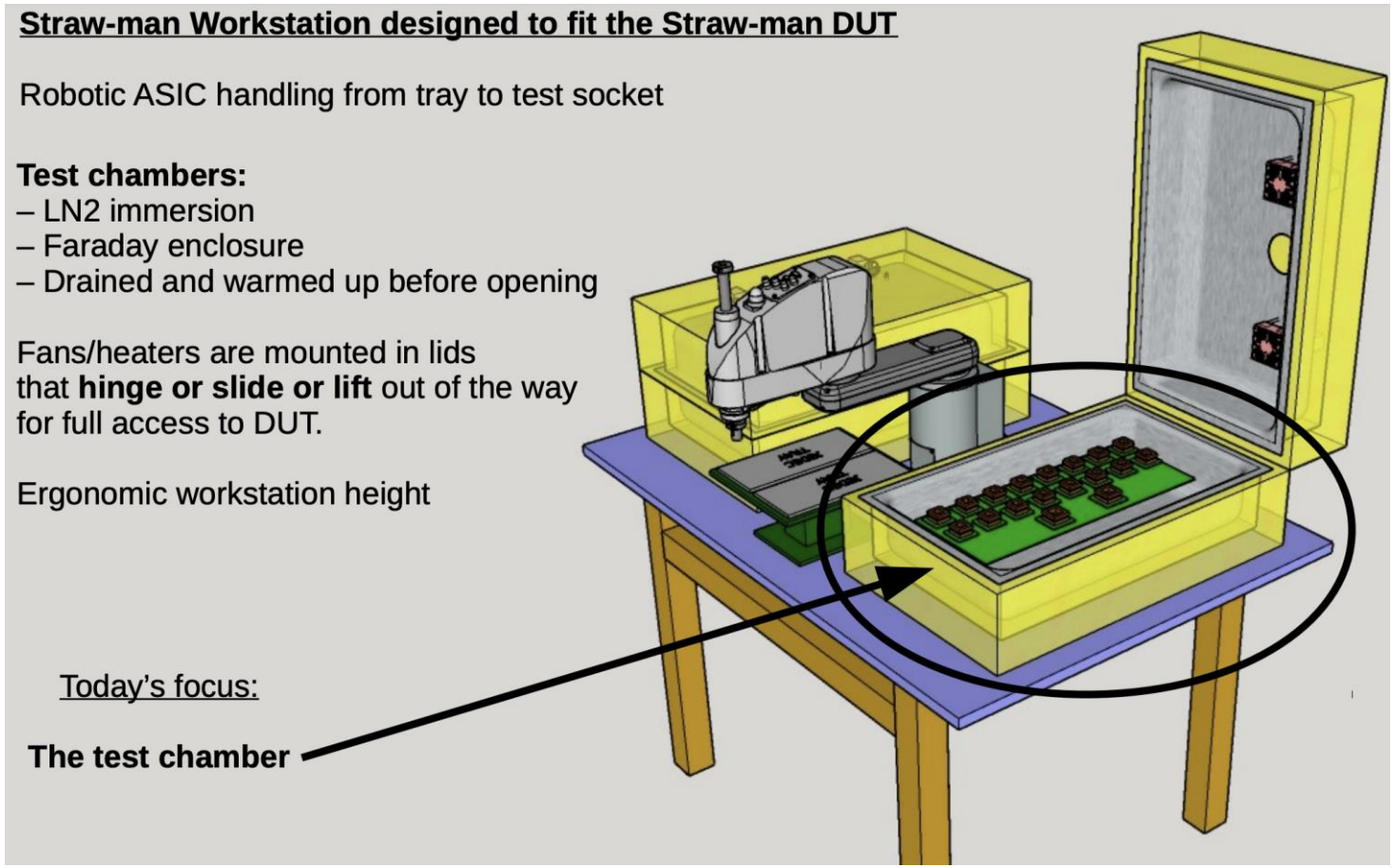


Schematics is done, layout is ongoing



Hardware: DUNE RTS

- Robotic Testing Station



RTS is designed by Dean Shooltz, Kendall Mahn, Carl Bromberg from Michigan State University

Software for LArASIC QC

- Unified ASICs and FEMB QC with the same SW set
  - Can benefit directly from the WIB, back-end DAQ, **analysis software developments**
  - Some extra software effort for ASIC QC can be implemented as a widget to the available software
    - Additional I2C registers that control the dedicated hardware on the test board
  - Test software will be mostly in the form of Python scripts.
    - Same test software for all test sites
    - Most of them have already been developed for WIB FW/SW development
    - Test result is automatically generated and transferred to the central hardware database
      - Each run of LArASIC testing has a unique key
- Continuous software development to achieve “The Five S’s”
  - Refer to Brett’s talk “Testing environment, interface to data storage and databases”
    - https://indico.fnal.gov/event/49447/
  - **Sampling**: Software to perform the basic test data acquisition.
  - **Store**: How we store and organize the acquired data.
  - **Summarize**: Extract important values from all samples into unified representation.
  - **Sync**: Copy samples and summaries to a central location.
  - **Serve**: Distribute and display summaries, statistics, inform hardware selections.

LArASIC QC Management

- QC activities in all sites will be monitored and led by the TPC electronics consortium
  - Maintain central repo for the testing software
  - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup (both DAT and RTS) and the same QC procedure
- LArASIC Identifier
  - EDMS-2505353 specifies a scheme for identifying all the detector components
    - LArASIC p5b from the engineering run: D0300200aa-nnnn
      - aa=01, 02, … is the serial number of the batch of 25 wafers that were ordered
    - Each chip will be marked a unique serial number by the packaging house
- LArASIC handling
  - LArASIC belongs to MSL level 3
  - Follow Standard IPC/JEDEC J-STD-033
    - Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices
- QC data storage
  - The hardware database is getting close to a useable state (Paul Laycock)
    - (to do) define what data needs achieved to form the component template for the hardware DB. The component template just defines what data is associated with each object.
    - A test summary in a data interchange format (e.g. HDF5, CSV, JSON) will be stored in the central hardware DB
  - All the raw data from testing is achieved locally

LArASIC QC Timeline and Resources

- The ASIC test board (DAT) and the robotic and cryogenic system (RTS) is expected to be ready by the end of 2022
- Plan to build a total of six replicas of the robotic test system
  - Two independent test stands for each of the three ASICs
- Assuming that LArASIC cold test can't be skipped (**worst case**)
  - ~100 chips per day
    - 6 thermal cycles per day, 2 RTS, 8 DUT chips per DAT
  - Assuming that 10% of the chips are tested again, 200 working days per year. QC starts in 01/2023
    - Test ~27,000 (30,000/1.1) chips by 07/2024 (300 working days)
      - Sufficient for the FEMBs for the first far detector module available by Fall 2024
    - Test ~48,000 (53,000/1.1) chips by 08/2025 (550 working days)
      - Sufficient for the FEMBs for the second far detector module available by Fall 2025
    - FEMB QC and ASIC QC can be proceeded in parallel
- Based on the LArASIC cold test for ProtoDUNE-II
  - 100% yield with >100 P5B chips is encouraging to consider that cold test for partial LArASIC chips (e.g., 10%).
    - both cost and labor for QC test will significantly decrease
    - FEMB cold test is unavoidable, each ASIC will be tested at cold after assembly
      - The criteria is that the yield of LArASIC chips should have negligible impact on the yield of FEMB boards.

Summary

- Previous and current LArASIC QC activities gains the experience for the coming DUNE ASIC QC
- LArASIC QC requirement and items are well explored and understood
- New hardware setup (both the ASIC test board and robotic test system) will increase the efficiency and reliability of ASIC QC for large quantity
- QC management and data storage is being detailed in the coming months
- Cost and timeline is understood and manageable
- We will be ready for LArASIC QC for DUNE FDs by the end of 2022