DUNE PRR: TPC Electronics ASIC

LArASIC Performance and FEMB Tests

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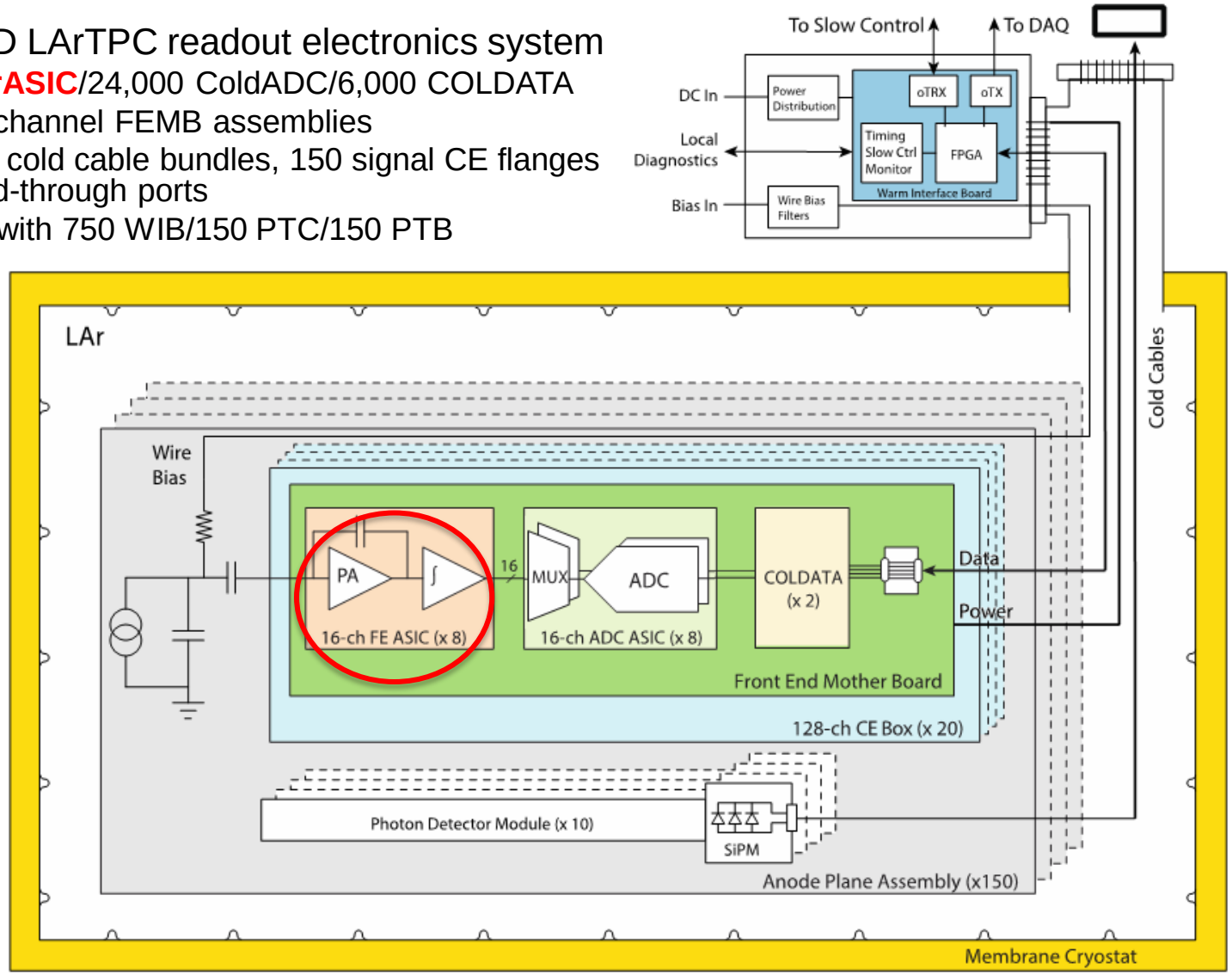
- Summary

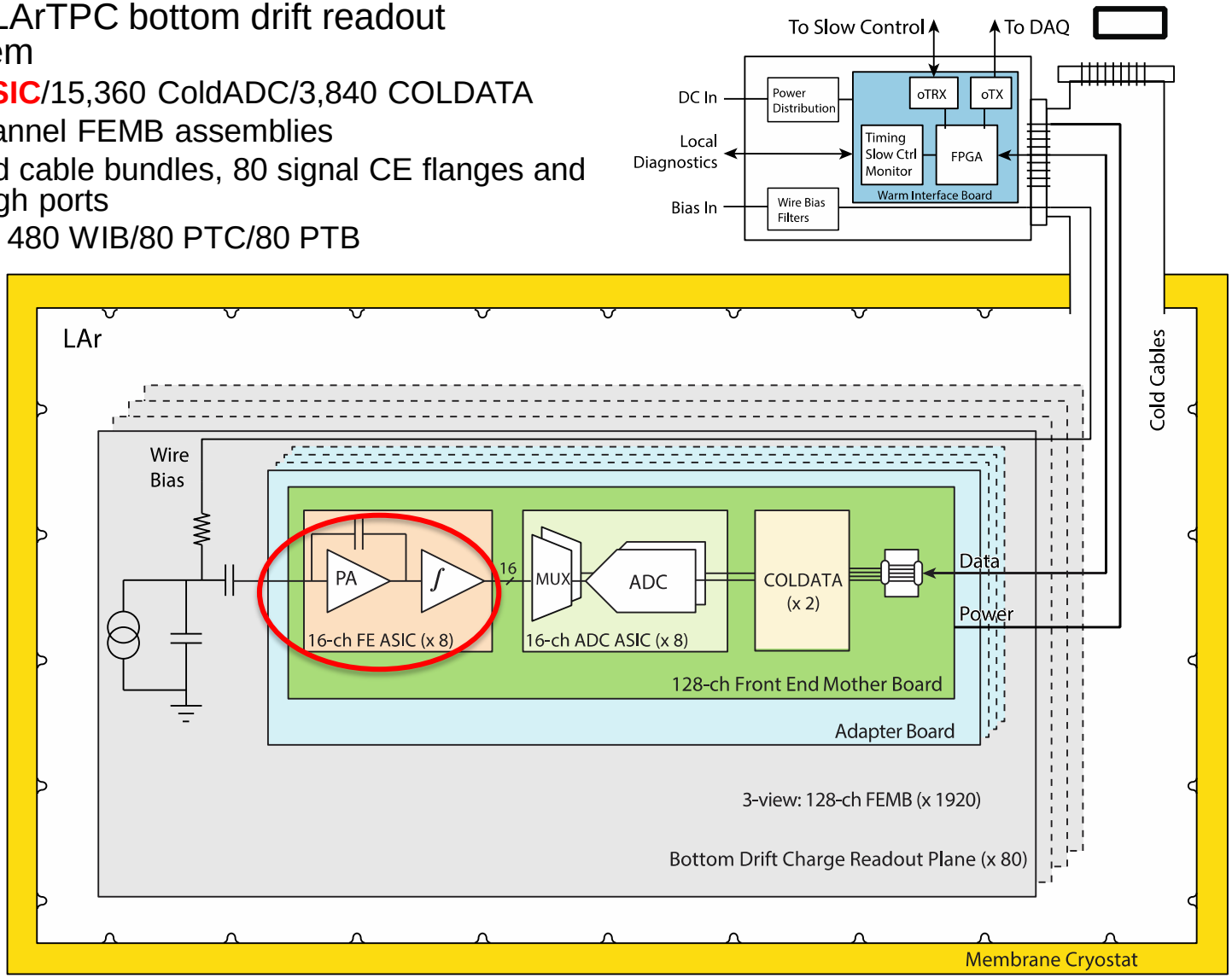
FD1-HD

- DUNE FD1-HD LArTPC readout electronics system
  - **24,000 LArASIC**/24,000 ColdADC/6,000 COLDATA
  - 3,000 128-channel FEMB assemblies
  - 150 sets of cold cable bundles, 150 signal CE flanges and 75 feed-through ports
  - 150 WIEC with 750 WIB/150 PTC/150 PTB



FD2-VD (Bottom Drift Electronics)

- DUNE FD2-VD LArTPC bottom drift readout electronics system
  - **15,360 LArASIC**/15,360 ColdADC/3,840 COLDATA
  - 1,920 128-channel FEMB assemblies
  - 80 sets of cold cable bundles, 80 signal CE flanges and 40 feed-through ports
  - 80 WIEC with 480 WIB/80 PTC/80 PTB



LArASIC Requirements and Specifications

- https://edms.cern.ch/document/2397298/1
- System noise < 1000 e^- [SP-FD-2]
- FE peaking time adjustable from 1 to 3 μs [SP-FD-13]
- Signal saturation level ~500,000 e^- (80 fC) [SP-FD-14]
  - **Gain of the front-end amplifier ~ 10 mV/fC [SP-ELEC-2, 2284]**
- Dead channels < 1% [SP-FD-28]
- Cold electronics power consumption < 50 mW/channel [SP-FD-21]
- Two baselines in the front-end amplifier [SP-ELEC-1, 2283]
- Input capacitance to front-end ASIC should be optimized for 120 to 210 pF [SP-ELEC-12]
- Channel-to-channel crosstalk < 1% (goal of < 0.1%) [SP-ELEC-11]
- Monotonic saturation recovery [SP-ELEC-10]

Summary of FDR

- System noise < 1000 e- [SP-FD-2] (**Achievable**)
- FE peaking time adjustable from 1 to 3 µs [SP-FD-13] (**Confirmed**)
- Signal saturation level ~500,000 e- (80 fC) [SP-FD-14] (**Confirmed**)
  - **Gain of the front-end amplifier ~ 10 mV/fC [SP-ELEC-2, 2284]**
- Dead channels < 1% [SP-FD-28] (**Achievable**)
- Cold electronics power consumption < 50 mW/channel [SP-FD-21] (**Confirmed**)
- Two baselines in the front-end amplifier [SP-ELEC-1, 2283] (**Confirmed**)
- Input capacitance to front-end ASIC should be optimized for 120 to 210 pF [SP-ELEC-12] (**Confirmed**)
- Channel-to-channel crosstalk < 1% (goal of < 0.1%) [SP-ELEC-11] (**Confirmed**)
- Monotonic saturation recovery [SP-ELEC-10] (**Confirmed**)
  - No ledge effect up to 2 pC

FDR Findings

- FDR Review Report
  - https://edms.cern.ch/file/2604156/1/DUNE_TPC_Electronics_ASIC_FDR_report_v03c.docx
  - During the preliminary design review (PDR) in February 2020, the version p3 of this ASIC was reviewed. Since then, the versions p4, p5 and p5a have been designed and tested.
  - The specifications (requirements) of this ASIC have been updated as requested during the PDR
  - The p4 version aimed at **fixing the "ledge effect", fixing the start-up problem of the band gap reference**, adding a Single-Ended to Differential Converter (SEDC) for differential interface to ColdADC and improving the uniformity of output DC baseline by introducing 16x RQI (reset quiescent current) subtraction in the second stage of the charge amplifier. The two first points were successfully tested. The new RQI circuitry led to random non-working channels at LN_2 temperature. This is due to large increase of the mismatches at low temperature and missing correct simulation models of the technology at this temperature. The SEDC exhibited too much power consumption.
  - The p5 version **fixed the large current consumption of the SEDC and removed the RQI circuitry**. In addition, a p5a version with several electrostatic discharge (ESD) protection circuits (as recommended during the PDR) were prototyped.
  - All versions were successfully tested and the team plans to submit on the same reticle as the p5 version and **a p5b version with the most robust ESD protection circuit tested in version p5a.**
  - The packaging will be the same as the one used up to now.

FDR comment and Recommendations

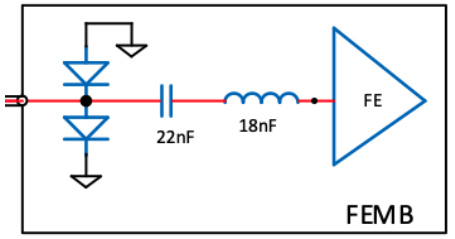
- Comments
  - The LArASIC design is **meeting all requirements** and the issues discussed during the PDR are solved.
  - The level of system tests completed so far with the most recent version of the ASIC (p5) is limited due to the availability of the new Front-End Mother Board (FEMB). However, no show stopper has been detected during the numerous tests done.
  - The production of the engineering run will allow to equip the ProtoDUNE-II TPC and to perform extensive system tests.
  - **The reticle contains both the p5 and p5b versions.** The selection of which version to be used in DUNE will be done at a later stage. At the time of the PRR, it will be decided whether a new mask set will be done to include only the selected version or whether the two versions are kept at the expense of wasting half of the wafers. This will mainly depend on the number of detectors to be equipped.
  - The QC procedure is defined but not yet fully validated (see later).
- Recommendations
  - **Go ahead with the engineering run production.**
  - **Actively continue the tests with the new FEMB.**

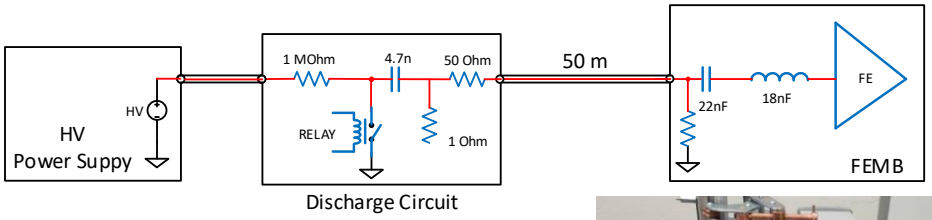
LArASIC Developments

- Goal of P5 LArASIC
  - Remove RQI subtraction to fix a few non-operational channels in LN2 (Success)
  - Modify SEDC buffer for stable and low noise operation (Success)
  - Modify Test Charge Injection Pulser DAC in terms of its linearity (Success)
  - Retain improvements achieved in P4 (ledge effect elimination, bandgap cold startup) (Success)
- Goal of P5A LArASIC
  - Explore different ESD protection schemes (Success)
  - Further investigate the RQI subtraction issue (Success, issue located)
- **Goal of P5B LArASIC (Verified after FDR)**
  - Apply ESD scheme with higher discharge tolerance (Engineering run, Success)
  - Data sheet can be reached: https://edms.cern.ch/document/2314428/

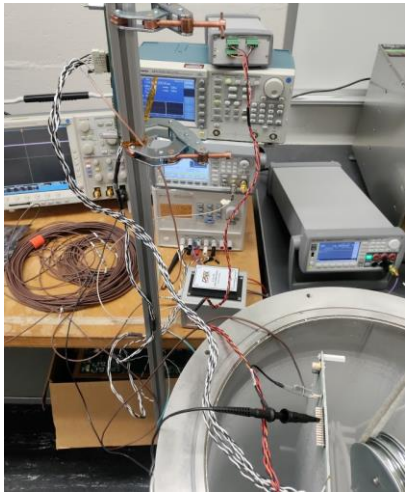
Enhanced ESD protection of P5B

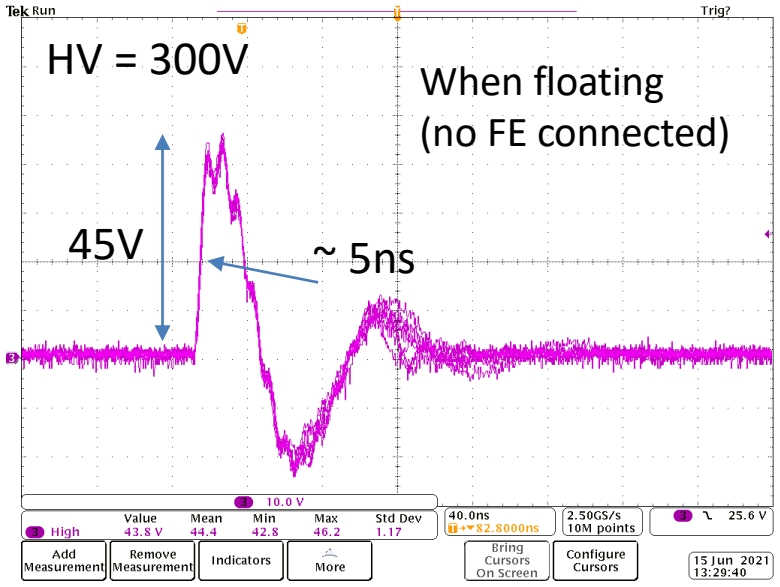
- P5 and previous version of LArASIC are vulnerable to the discharge damage
  - We suffered a lot for LArASIC failure during ASIC screening, FEMB assembly and installation
  - ProtoDUNE-I: ~40 channels got damaged during the discharge event between 01/15/2020 to 09/01/2020
    - Accidental large discharge during detector commissioning is rare
    - The protection diodes effectively mitigate most discharge
    - Previous studies indicate that FE is vulnerable to large discharge rate





- The principle is to get a very fast pulse signal (>20V)
  - 1 Ohm to offer a fast RC constant
  - Two 50 Ohm resistors for termination
  - 50m cable further mitigates the signal refection





Test Result

- To kill/damage channels **in one pulse or (< 10 pls)**

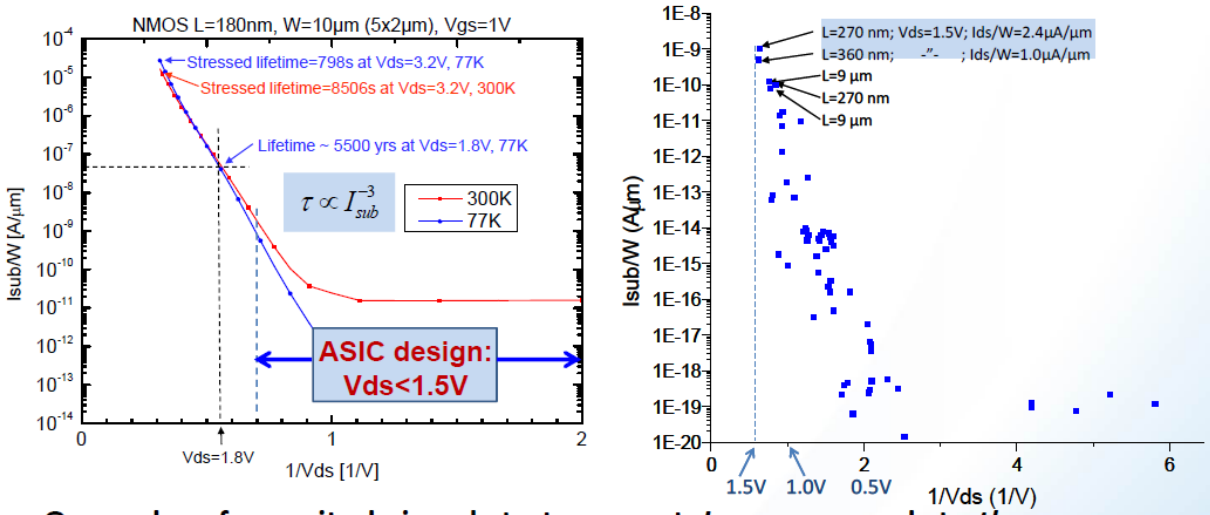
	RT		LN2	
LArASIC	-HV (+Pulse)	+HV (-Pulse)	-HV (+Pulse)	+HV (-Pulse)
P5, 1x	(+31V)	(-44V)	(+59V)	(-91V)
P5A, 30x	(+84V)	(-130V) <100 pls	(+154V) <5 pls	(-172V) <25 pls
P5B, 30x	+82V / 1 pls	-153V / 1 pls	(+118V) / 2 pls	(-153V) / > 10 pls

- Observations:
  - ESD tolerance increases with 1x to 30x ESD
  - ESD tolerance is higher at negative : **-ESD > +ESD**
  - ESD tolerance is higher at LN2 as compared to RT: **ESD(LN2) > ESD(RT)**
- **The external protection diode is still required for detector operations**
  - ESD tolerance is still not sufficient to prevent damage caused by accidental detector discharge
  - The enhanced ESD protection is expected to mitigate the LArASIC failure during QC and FEMB assembly

Lifetime Study

- The remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to channel hot carrier effects (HCE)
- **LArASIC is designed for long lifetime at cryogenic temperatures**
  - Low voltage and current in each transistor

Measurement Type II: Substrate Current Density I_{sub}/W vs $1/V_{ds}$



- **One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.**
- **I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced* V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.**

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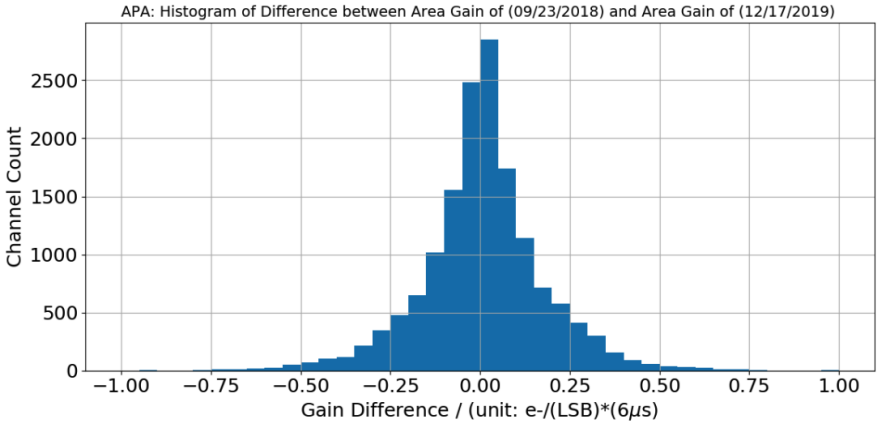
To alleviate the lifetime risk, **custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years**

Any transistor falling in the region V_{ds} <1.5 V and I_{sub}/W < 10^{-9} A/m should have a very long lifetime

S. Li, et al, "LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Transactions on Nuclear Science, Volume: 60, Issue: 6, Part: 2, Pages: 4737-4743 (2013)

Lifetime Study

- LArASIC in MicroBooNE: **No observable change after seven years**
- ProtoDUNE-I (SP): No measurement degradation is observed over a year
  - The measured gain shift is around 0.13% and 0.4%RMS, with an excellent agreement between 2018 and 2019 (around 0.01% shift with 0.3% RMS)
- The lifetime study of LArASIC will take place in two different phases, the exploratory phase and the validation phase. Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is the preparation phase. The most time and effort will focus on the exploratory phase, we will gain (or lose) confidence based on the test results in this phase. Validation phase will be useful to validate what we would learn in the exploratory phase, and collect more information to prepare for future review(s)
  - **A P5 LArASIC was stressed at 3.0V over 300 hours in liquid nitrogen, no significant change in current drawn is observed.**
  - The recommended voltage for CM018/G is 1.8 V + 10%, which limits the stress voltage
    - commercial chips designed in TSMC 180 nm, e.g., AD9265 and AD9650, the absolute maximum rating is 2.0 V which is consistent with 1.8V + 10%
  - Test setup will be optimized with the dual-dut test board to observe more performance parameters
  - More tests will be carried out after the busy ProtoDUNE-II production



ProtoDUNE-SP: Good reliability over a year operation

LArASIC QC for ProtoDUNE-II

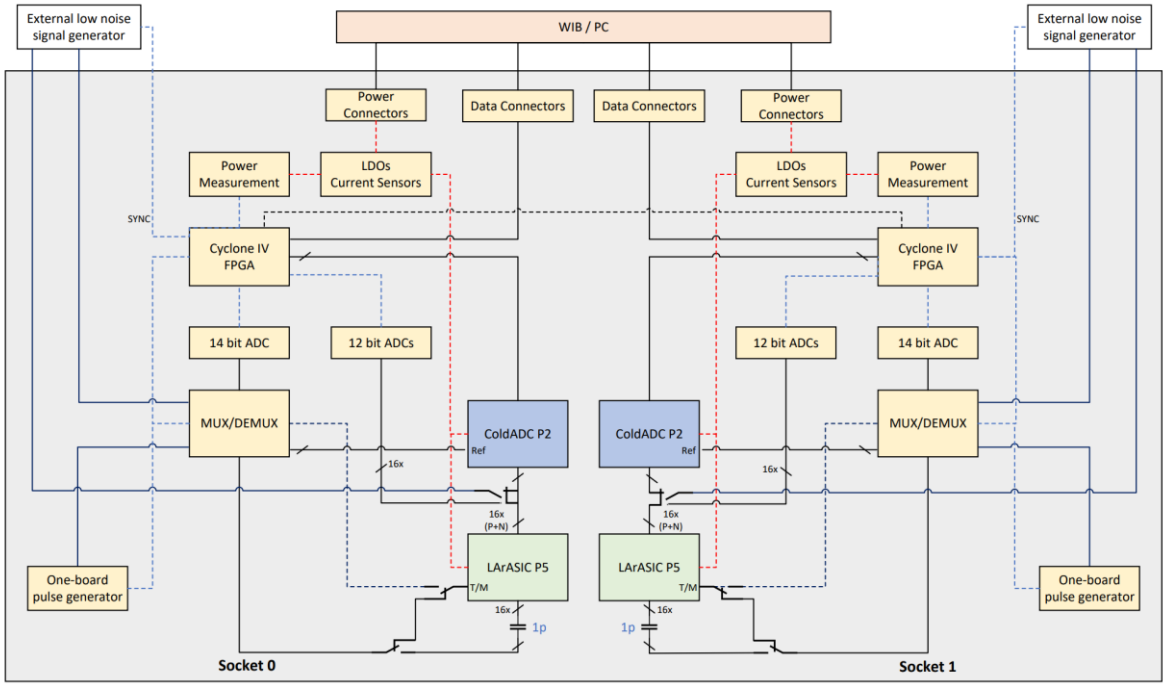
- Received ~1.8k P5 and 1.8k P5B chips on 01/10
  - Released P5/P5B ENG run to TSMC on August 31
  - IMEC/GTK package 6 wafers of P5/P5B in LQFP128 package
  - Expect ~1,200 LArASIC (including spares) for FEMB assembly
    - ProtoDUNE-II HD: 80 FEMBs (80x8), ProtoDUNE-II VD: 48 FEMBs (48x8)

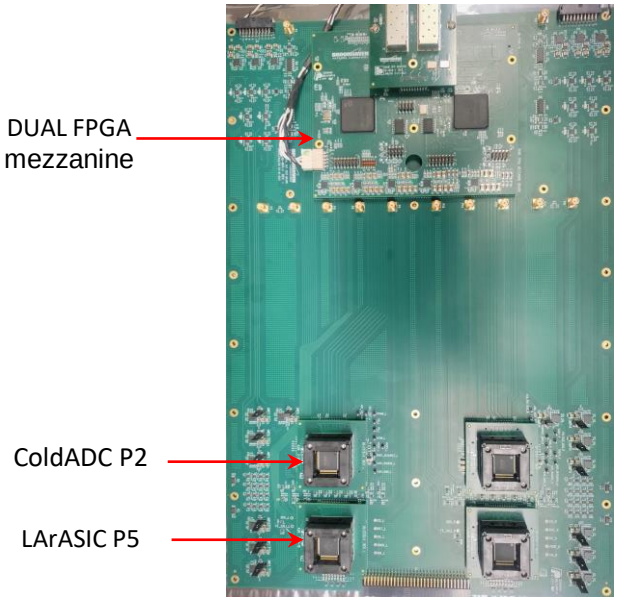
QC Item	Description
Power consumption	Each LArASIC has 3 power rails (VDDP, VDDA, VDDO) of which voltage and current are recorded under 3 configurations (default, SE on, and SEDC on)
FE power cycle	To check pulse response during each power cycle
SPI checkout test	Write and read to LArASIC register
Charge pulse direct to input	To check that input is connected to preamplifier (rare case)
Channel pulse response checkout (pulsing from internal DAC)	• Baseline measurements (200mV/900mV) • Pulse response with different peaking time
Monitoring	• Check response from each channel (through test pad) • Baseline measurements (through commercial ADC) • BGR voltage measurement • Temp. sensor voltage measurement
Noise measurements	With different peaking time and buffer configuration
Full chain linearity measurements (LArASIC+ColdADC)	• Input from internal DAC • Direct input from external pulse generator • Input from test pin and through internal calibration capacitor • Gain, linearity and pedestal measurements

QC items for ProtoDUNE-II is subset of future DUNE LArASIC QC (limited by Dual-DUT test board)

LArASIC QC Test Stand: Dual-DUT Test Board

- Dual-FPGA FM + Test Motherboard + 2 DUTs
  - Can characterize LArASIC thoroughly
  - The assembly will be submerged in LN2
- Interface
  - Data is readout through UDP interface of Dual FPGA mezzanine
  - Can be readout by WIB as well (require FW update)
- Support LArASIC/ColdADC characterization





LArASIC P5/P5B: Yield

- Dual-DUT test board has been used to test LArASIC P5/P5B chips
  - The second and third test stands for LArASIC are being prepared
  - Test ~20 chips with 2 CTS per day

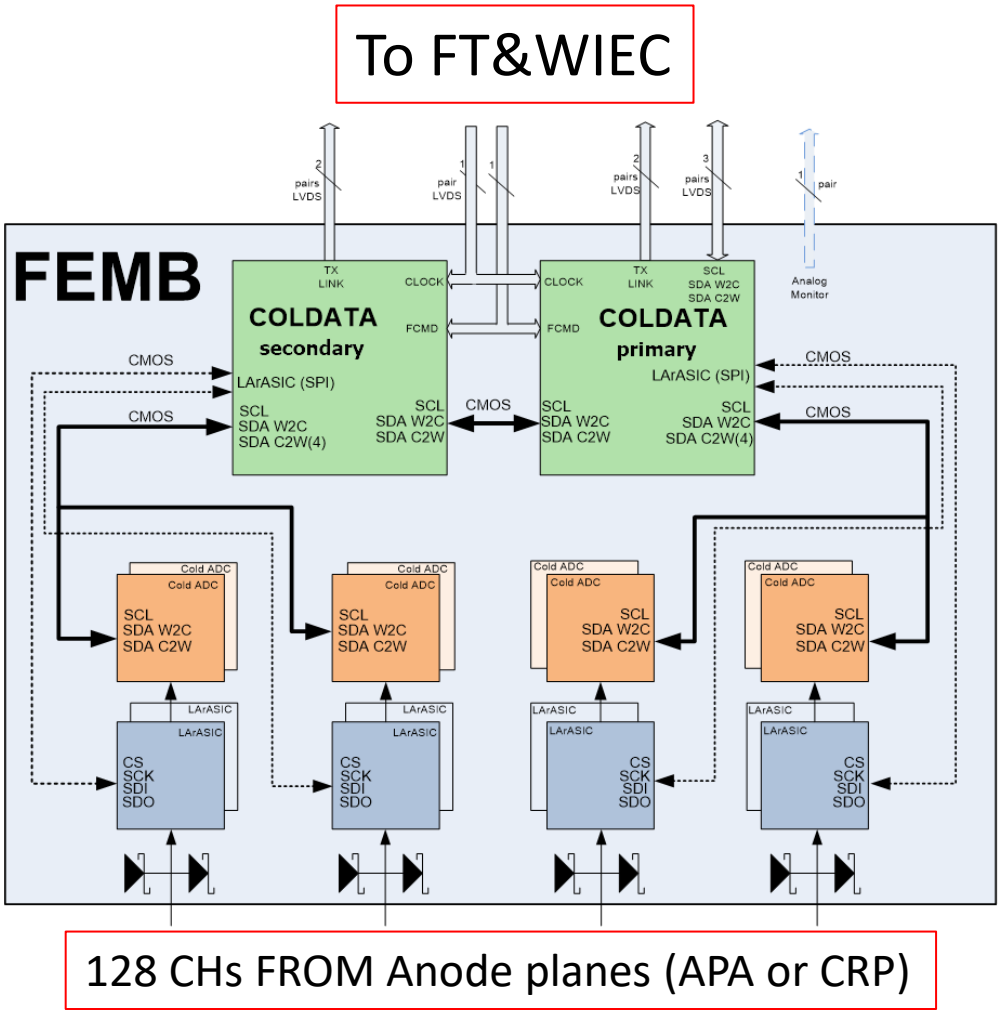
LArASIC Version	Temp.	Tested Chips#	Good #	Yield
P5	RT	55 (old packaging batch)	55	100 %
P5	RT	84 (new packaging batch)	80	~95.23 %
P5	Cold/LN2	60	57	~95 %
P5 (ENG Run)	RT	49	49	100%
P5B (ENG Run)	**RT**	**366**	**364**	**99.4 %**
P5B(ENG Run)	**Cold/LN2**	**165 + 56***	**165 + 56***	**100 %**

- P5
  - At RT: 4 chips with inactive input channels (likely caused by ESD discharge before testing)
  - At LN2: 3 chips with inactive input channels (permanent damage caused by ESD discharge over handing)
- **P5B (ENG RUN)**
  - At RT: 2 chips were likely caused by manufacture defects
    - Fail mode of chip#198: ch6 no response, outputs 0V with DC coupling
    - Fail mode of chip#269: Control register for ch15 works can't config ch15 properly
  - AT LN2
    - 165 chips were tested by dual-DUT test board
    - 56 chips were tested on 7 FEMB boards. These 56 chips only passed the warm test before assembly

Dual-DUT test board and MSU CTS

The Monolithic FEMB with 3-ASIC

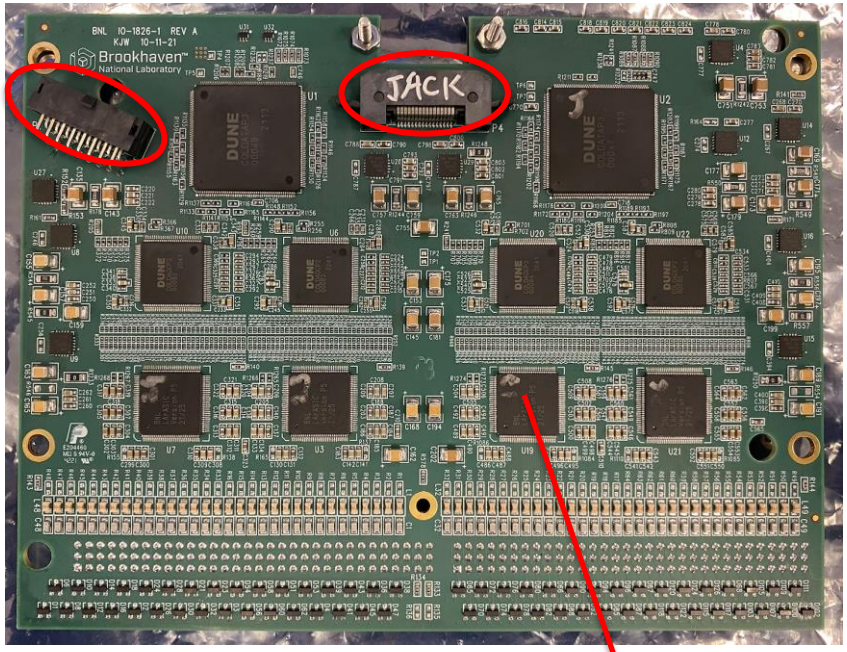
- 8x LArASIC (P5B)
  - 16-ch programmable charge amplifier
  - Enhanced ESD protection
- 8x ColdADC (P2)
  - 16-ch, 12-bit, 2 MS/s ADC
  - INL < 5 LSB, DNL < 0.3 LSB
- 2x COLDATA (P4)
  - Used to be FPGA in ProtoDUNE-I
  - Serializer and controller
    - 2 x 1.25 Gb/s TX data link per chip



The FEMB design is finalized, verification with P4 COLDATA has been performed.

The Monolithic FEMB

- P5B LArASIC has enhanced ESD protection for FE inputs
- Both 9m/22m cables are verified with the FEMB



P5 was replaced by P5B

Room Temperature				
	Warm side w/ 22m cable		Cold side	
	Power (W)	Power(mW/CH)	Power (W)	Power(mW/CH)
SE Buf OFF	5.026	39.3	4.430	34.6
SE Buf ON	5.619	43.9	4.876	38.1
DIFF	5.796	45.3	5.018	39.2

LN2 Temperature				
	Warm side w/ 22m cable		Cold side	
	Power (W)	Power(mW/CH)	Power (W)	Power(mW/CH)
SE Buf OFF	4.444	34.7	4.338	33.9
SE Buf ON	5.089	39.8	4.947	38.6
DIFF	5.292	41.3	5.134	40.1

Note:

- Power Consumption is calculated with the optimum setting of each power rail. We assume at FEMB input side, 2.45V for ADC, 2.2V for FE, 2.45V for COLDATA before regulators
- The maximum dropout voltage of regulator is 55mV based on datasheet, 200mV is reserved
- If power dissipation of DC-DC modules on WIB is also taking account, per channel power consumption is slightly higher but still lower than 50mW/Ch.

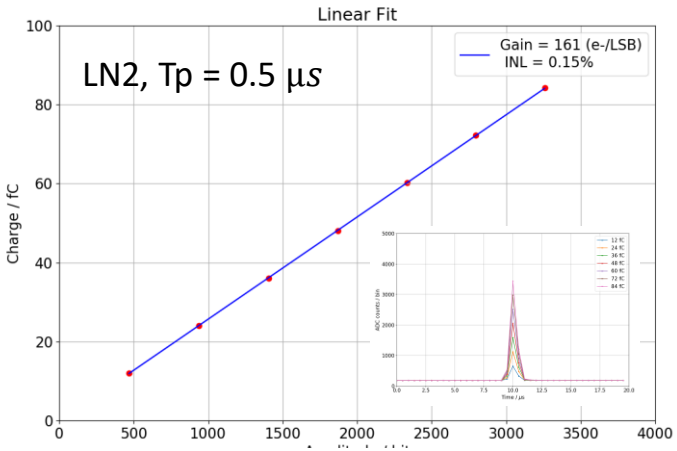
The Monolithic FEMB Performance

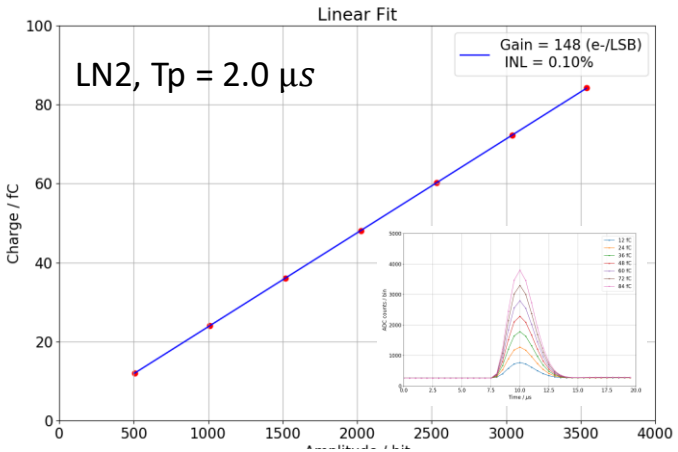
- Presented in the CE consortium meeting on 08/23/2021 and 10/25/2021
  - https://indico.fnal.gov/event/50615/
  - https://indico.fnal.gov/event/51298/
- The monolithic FEMB meets the DUNE requirement
  - **Single-ended interface between FE and ADC is slightly preferred**
    - Pro: less power consumption
    - Pro: slightly better noise performance
    - Pro: slightly better linearity
    - Con: slightly worse crosstalk
  - The option of differential interface between FE&ADC is reserved on the FEMB
    - They can be switched on through FEMB configuration

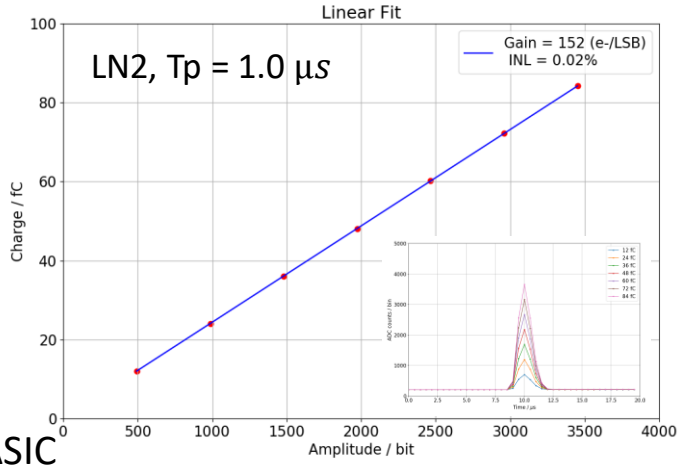
Report on 08/23/2021: Linearity measurement

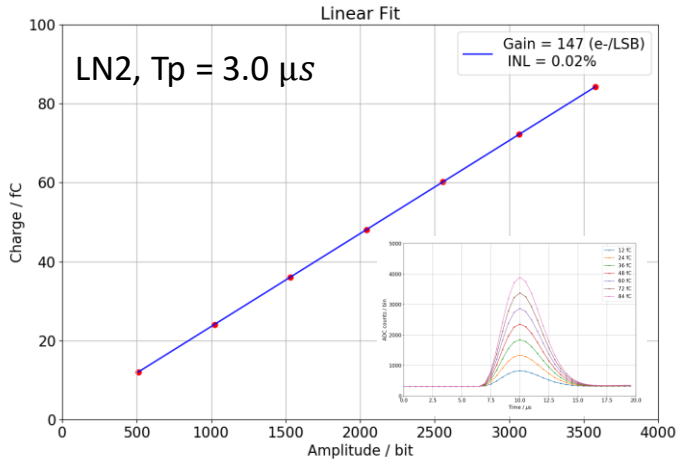
- Signal generator Keysight 33600A is used to inject calibration pulses with precise amplitude. Voltage resolution of 33600A is 14-bit and the accuracy of amplitude is ± 1 mVp-p. Previous measurements with P2 LArASIC in 2019 show that the non-linearity of 33600A output is < 0.05%.
- External reference capacitor was calibrated again recently, stable at 1.203pF over a few years
- To avoid potential effects from crosstalk, only one chosen input channel (chip#3CH3) receives the calibration pulse at a time

- FEMB Configuration
  - LArASIC
    - 14mV/fC
    - 500pA
    - 200mV baseline
    - single-ended with buffer bypassed
  - ADC:
    - single-end mode with SDC bypassed







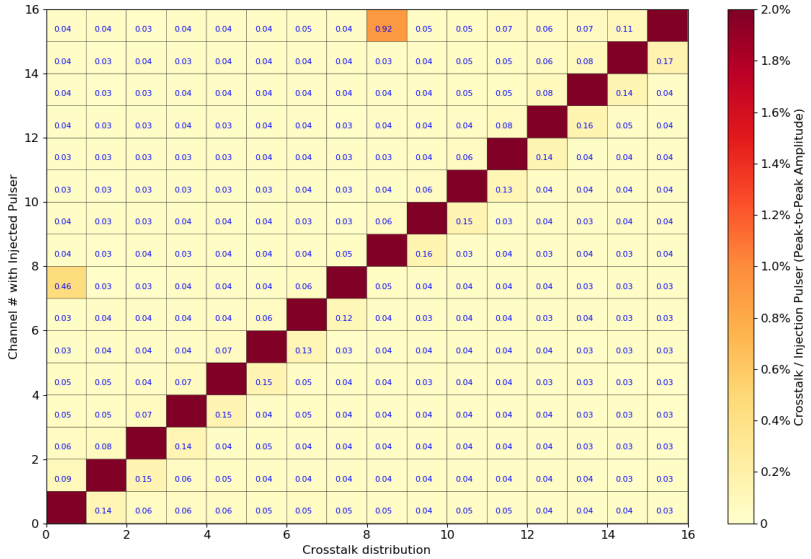


Non-linearity <= 0.1% in 90 fC range at LN2 when peak time >= 1.0 μs

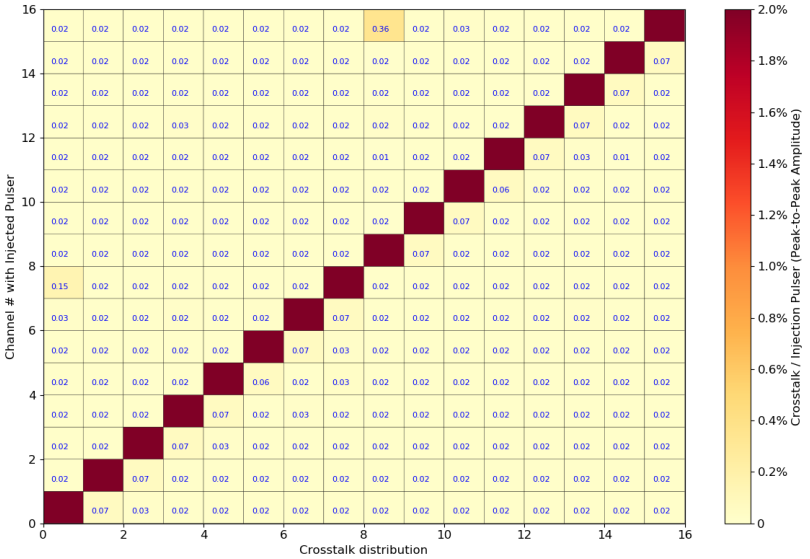
Note: Tested with P5 LArASIC

Report on 08/23/2021: Crosstalk Study (LN2)

- Crosstalk of LArASIC and ColdADC readout chain
  - With external ~84fC injected on CHIP#3
    - External charge: 84fC = 70 mV from signal generator * 1.203pF reference capacitor
  - Differential interface has less than a half of crosstalk level than single-ended interface
  - Except CH0 (affected by CH7) & CH8 (affected by CH15), crosstalk < 0.1% at LN2 for both SE and DIFF interface.



Single-ended interface at LN2



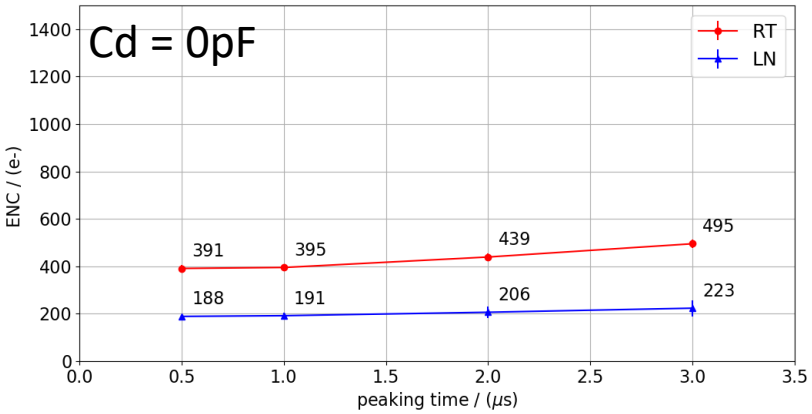
Differential interface at LN2

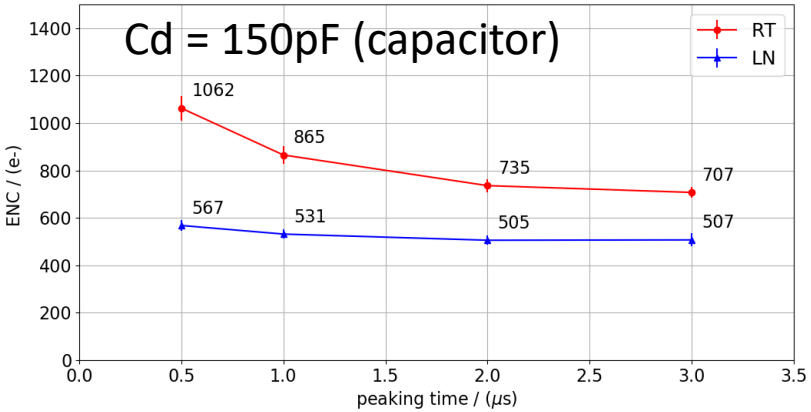
Other LArASIC and ColdADC readout chains have the similar results

Note: Tested with P5 LArASIC

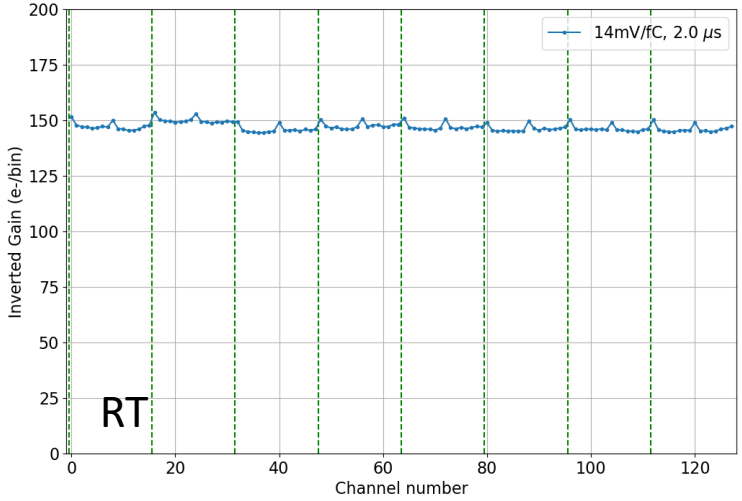
Performance of FEMB with P5B LArASIC

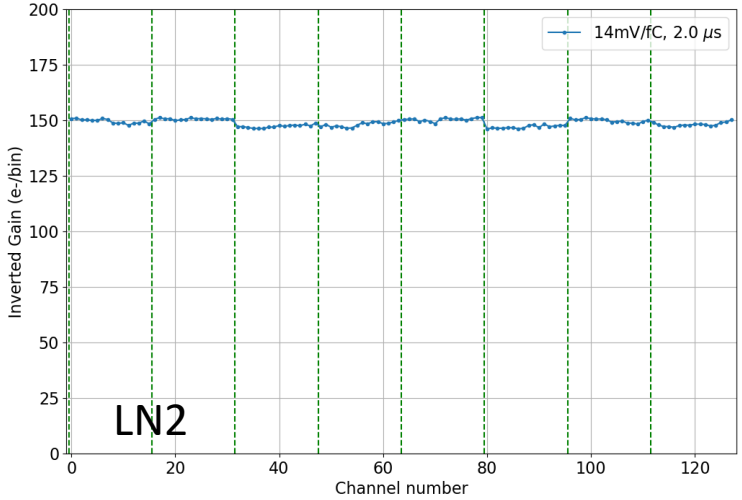
- Noise Performance (SE interface between FE & ADC)





- Gain Performance (SE interface between FE & ADC)

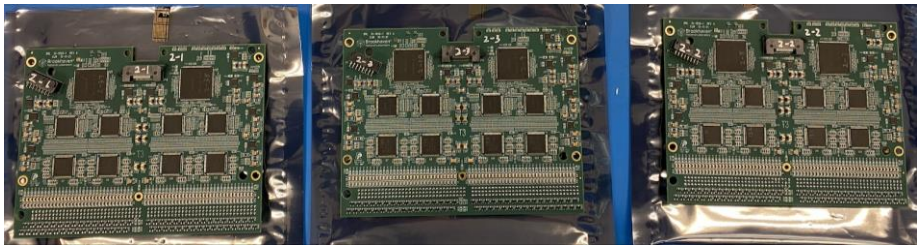




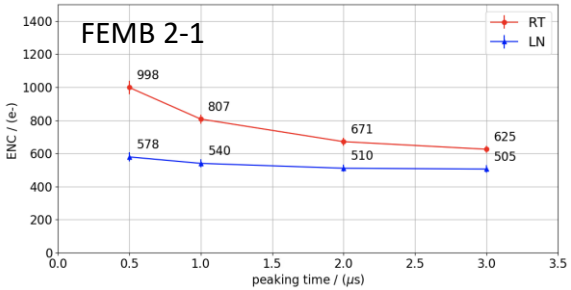
Note: The option of differential interface between FE&ADC is reserved on the FEMB

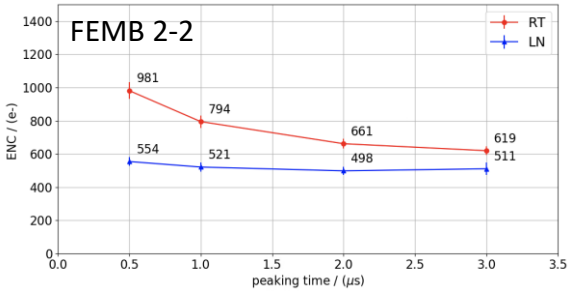
7 FEMBs with P5B chips pass the check-out test

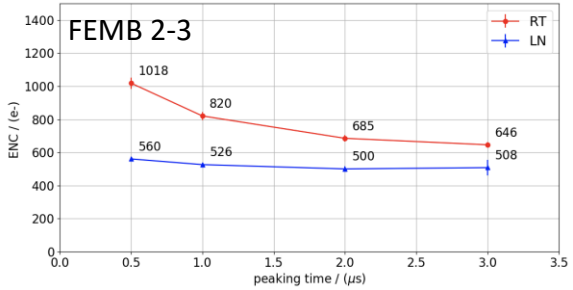
- These 7 FEMBs are for debugging and BNL integration test purpose
  - LArASIC and ColdADC chips passed warm test only
  - Pass quick check-out test, both RT and LN2
    - Noise and Gain @ 14mV/fC were measured

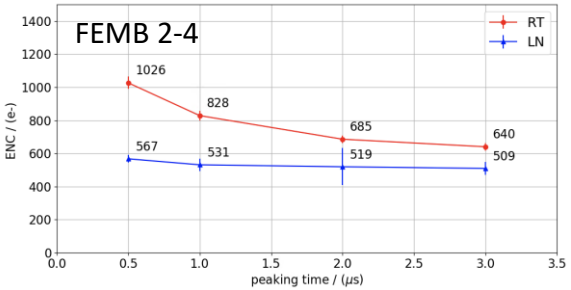


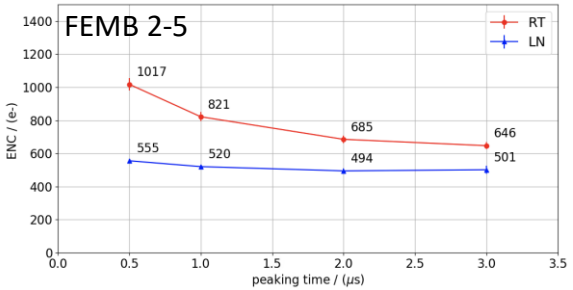
6 FEMBs received on 03/04/2022

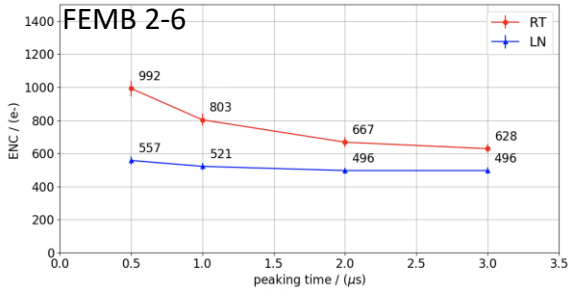












Brookhaven National Laboratory DUNE

Summary

- Engineering Run for P5B LArASIC is successful
  - Achieve expected goal for enhanced ESD protection w/o compromising LArASIC performance
- The monolithic FEMB design is finalized for ProtoDUNE-II
  - FEMB meets the project requirements
  - Promising QC result for P5B
- P5B LArASIC is ready for production
  - 24,000 LArASIC for DUNE-FD1-HD
  - 15,360 LArASIC for DUNE-FD2-VD
  - QC for LArASIC for DUNE FD1&FD2 will be discussed later

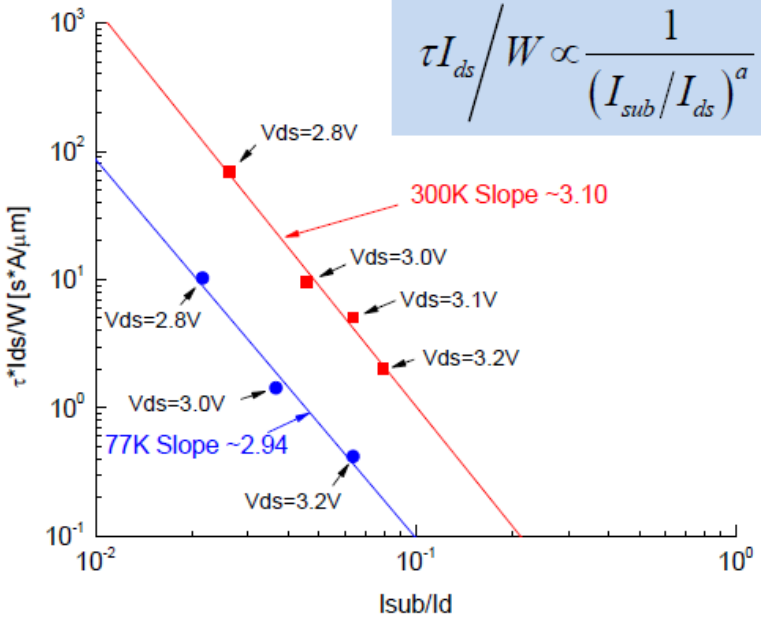
Backups

Appendix

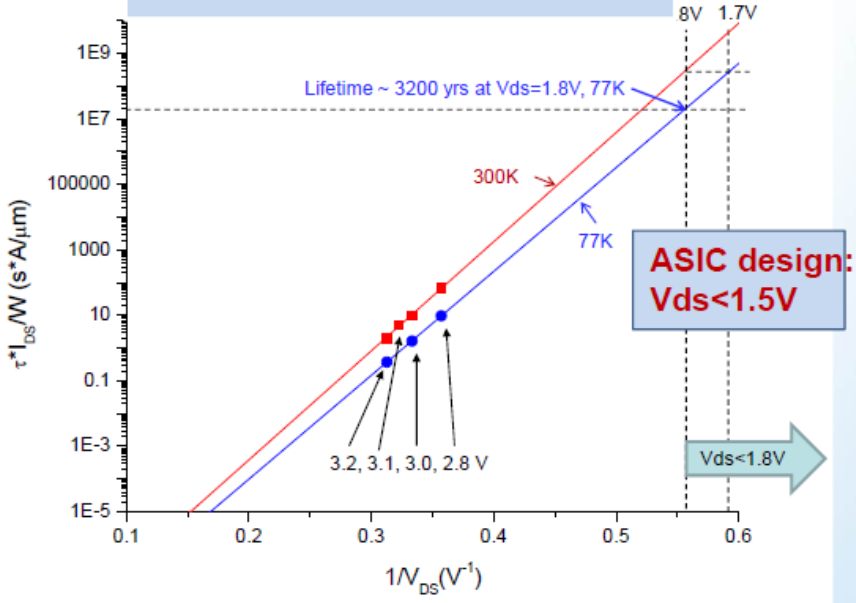
Accelerated Lifetime Measurements (180 nm)

Measurement Type I: "Stress Plot"

$$\tau I_{ds} \Big/ W \propto \frac{1}{(I_{sub}/I_{ds})^{a}}$$



$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds} - V_{dsat}}$$



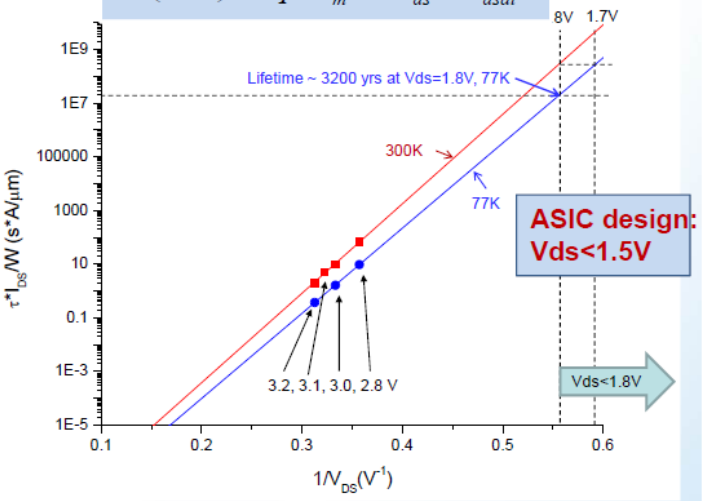
- *If the measured points at both 300K and 77K are close to the characteristic slope for the interface state generation, $a = \varphi_{it}/\varphi_i \approx 3$, it confirms that the degradation follows basic relations for interface state creation. Substrate current must be measured for this stress plot.*
- *The lifetime prediction plot (right) can be derived from the stress plot (left), or from direct measurements of τ vs. V_{ds}, without measuring the substrate current*

Lifetime Study

- The only remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to channel hot carrier effects (HCE).
  - Most failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature.
  - Lifetime due to HCE aging: A limit defined by a chosen level of monotonic degradation
    - The device “fails” if a chosen parameter gets out of the specified circuit design range. This aging mechanism does not result in sudden device failure.

- LArASIC is designed for long lifetime at cryogenic temperatures, with minimum gate length of 270 nm in TSMC 180 nm technology.
  - To alleviate the lifetime risk, custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years, by selection of Vdd and L, essentially to get out of the region of degradation measurable after 30 years.
    - S. Li, et al, “LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling,” IEEE Transactions on Nuclear Science, Volume: 60, Issue: 6, Part: 2, Pages: 4737-4743 (2013)

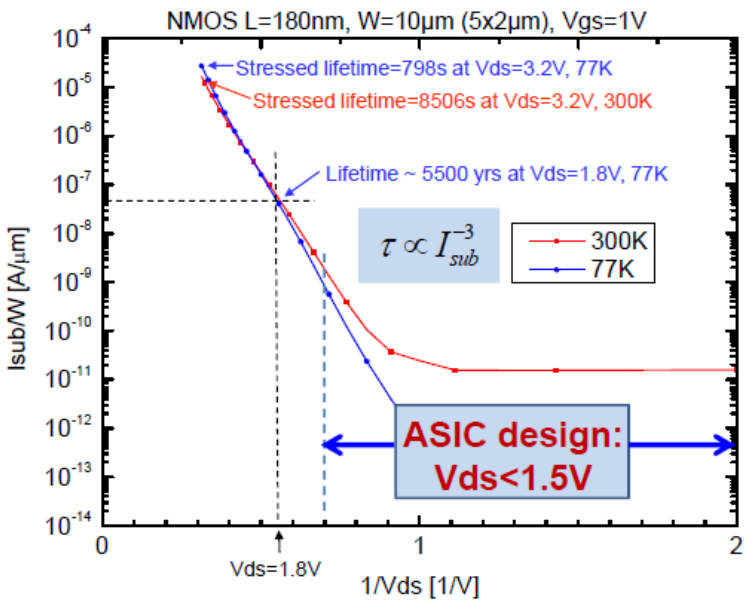
$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds} - V_{dsat}}$$

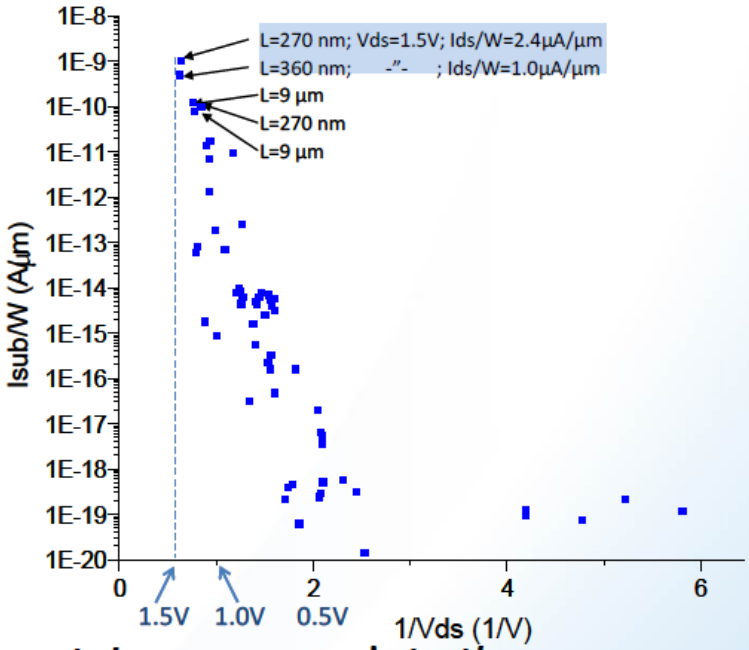


Accelerated Lifetime Measurements (180 nm)

Appendix

Measurement Type II: Substrate Current Density I_{sub}/W vs $1/V_{ds}$





- One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.
- I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced* V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.

Brookhaven Science Associates

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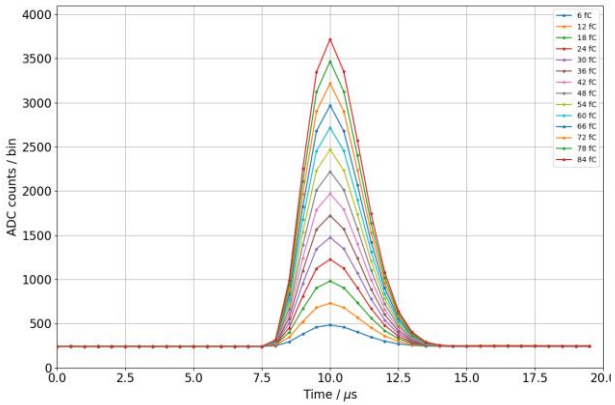
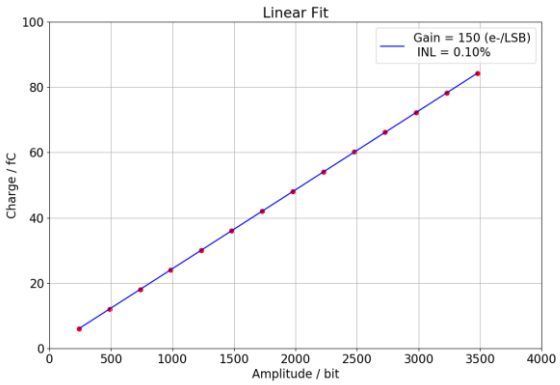
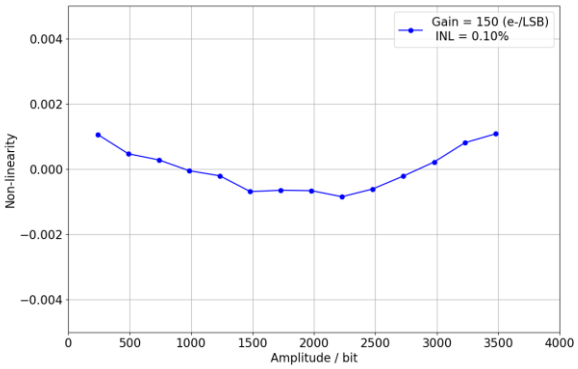
FEMB Characterization (RT)
Linearity measurement with external calibration source

- Signal generator Keysight 33600A is used to inject calibration pulses with precise amplitude. Voltage resolution of 33600A is 14-bit and the accuracy of amplitude is ± 1 mVp-p. Previous measurements with P2 LArASIC in 2019 show that the non-linearity of 33600A output is < 0.05%.
- External reference capacitor was calibrated again, stable at 1.203pF over a few years
- To avoid potential effects from crosstalk, only one chosen input channel receives the calibration pulse at a time

- FEMB Configuration
  - LArASIC: 14mV/fC, 2.0us, 500pA, 200mV baseline, single-ended with buffer bypassed
  - ADC: single-end mode with SDC bypassed





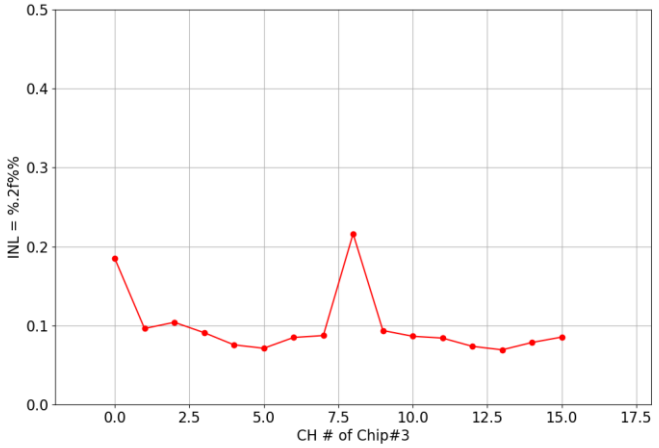


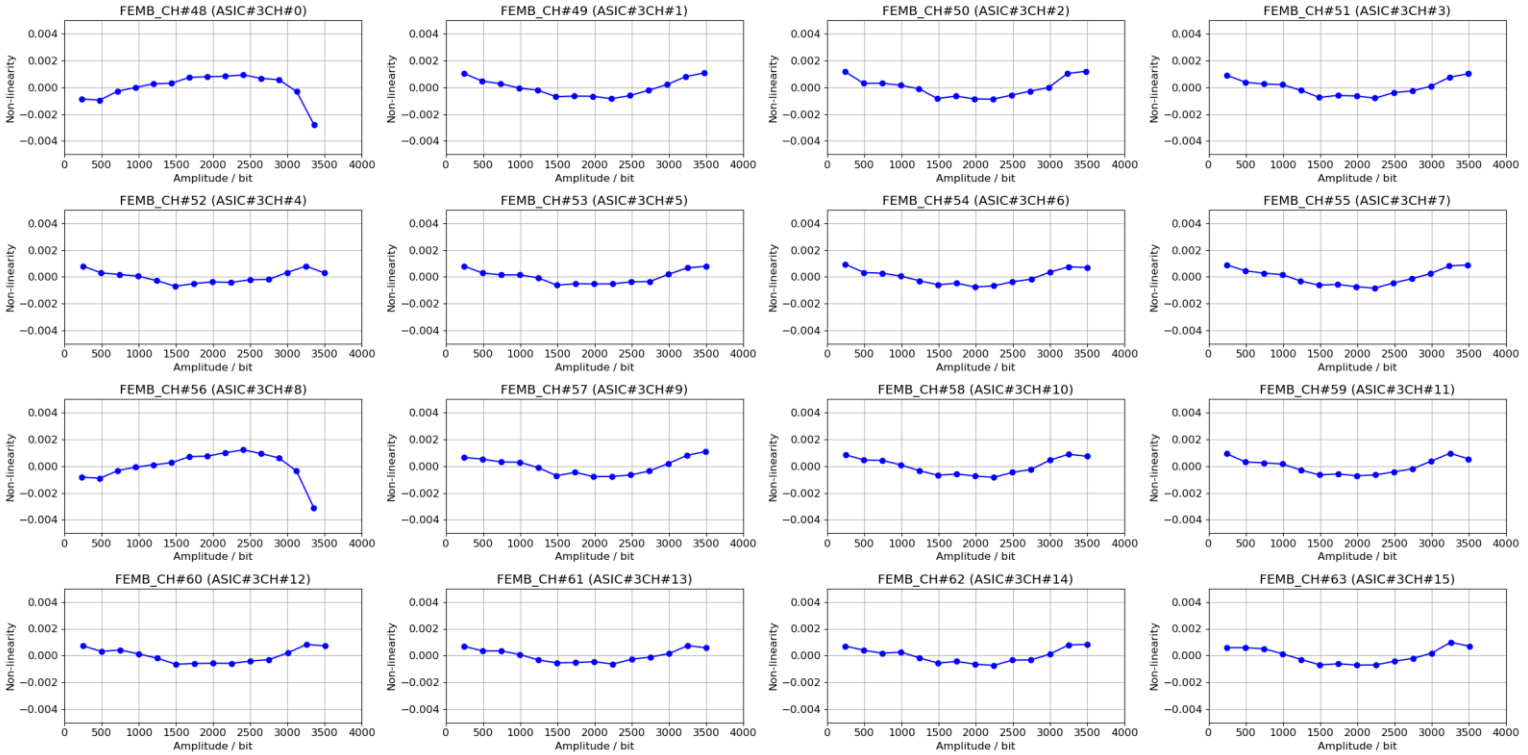
CHIP#3CH#1 at RT: Gain = 150 (e-/LSB), INL = 0.1%

Note: Tested with P5 LArASIC

INL Distribution (RT)

- CH0 & CH8 have slightly larger non-linearity
  - DUNE requirement < 1%
  - Likely caused by ColdADC
  - < 0.1% non-linearity can be achieved for all channels when full scale < 80 fC



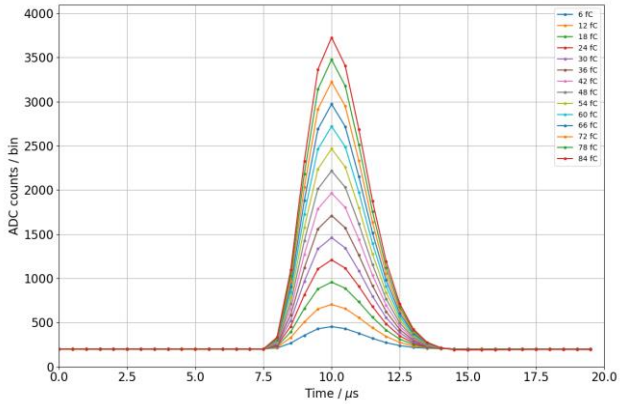


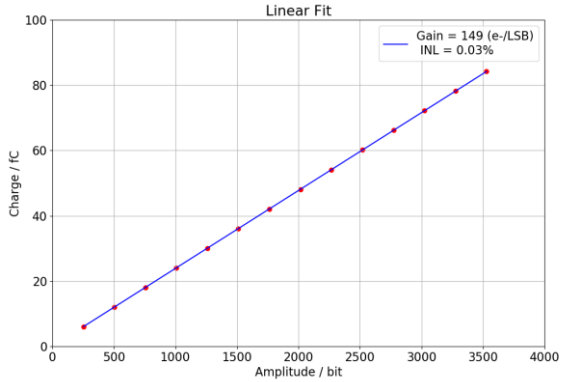
Note: Tested with P5 LArASIC

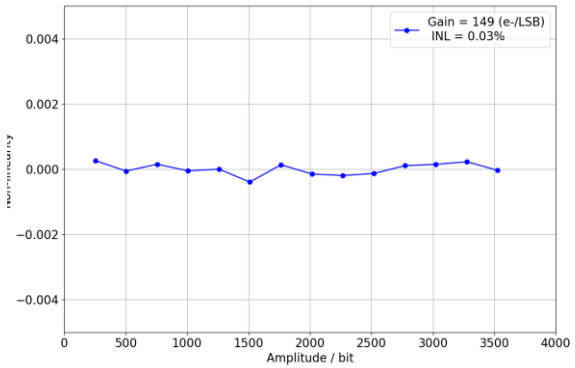
FEMB Characterization (LN2)

Linearity measurement with external calibration source

- Signal generator Keysight 33600A is used to inject calibration pulses with precise amplitude. Voltage resolution of 33600A is 14-bit and the accuracy of amplitude is ± 1 mVp-p. Previous measurements with P2 LArASIC in 2019 show that the non-linearity of 33600A output is < 0.05%.
- External reference capacitor was calibrated again, stable at 1.203pF over a few years
- To avoid potential effects from crosstalk, only one chosen input channel receives the calibration pulse at a time
- FEMB Configuration
  - LArASIC: 14mV/fC, 2.0us, 500pA, 200mV baseline, single-ended with buffer bypassed
  - ADC: single-end mode with SDC bypassed





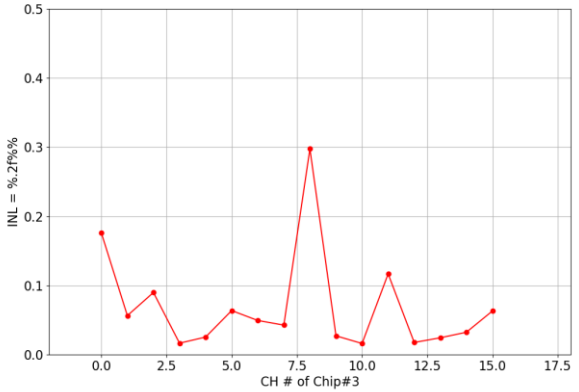


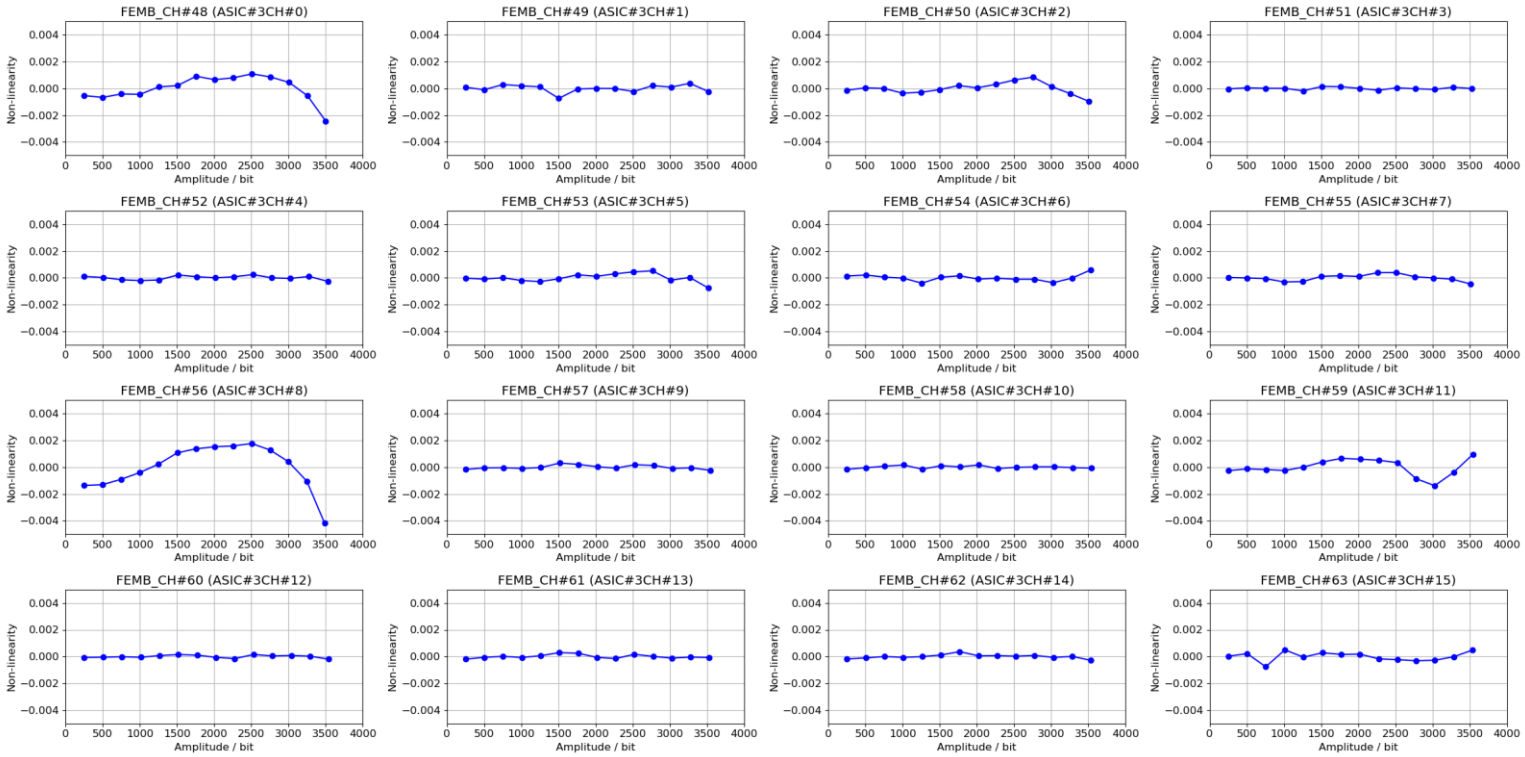
CHIP#3CH#1 at LN2: Gain = 150 (e-/LSB), INL = 0.03%

Note: Tested with P5 LArASIC

INL Distribution (LN2)

- CH0 & CH8 have slightly larger non-linearity
  - DUNE requirement < 1%
  - Likely caused by ColdADC
  - **< 0.1% non-linearity can be achieved for most channels when full scale < 80 fC**
  - calibration pulser: 5mV*1.203pF / step





Note: Tested with P5 LArASIC

chip#3 on board