Overview, LArASIC Requirements and Recommendations from FDR

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LArASIC Production Readiness Review
7-8 March 2022

Thank you for taking time to serve on the ASIC PRR Committee

Your assessments and recommendations are important to us

Goal of this review:

We would like to obtain the approval from the Committee to proceed with the production of LArASICs for Far Detector#1 (FD1) and Far Detector#2 (FD2) ASAP

Why:

Due to the ASIC industry turmoil, brokers and TSMC are starting to restrict access to certain production lines. In particular, the 180nm technology production on 8” wafer. This is the technology for LArASIC. We would like to obtain enough LArASICs for FD1 and FD2 + spares before we get lock out of the production line

Message from IMEC

Dear Europractice member and TSMC 8 inch technology user,

First of all a healthy and successful New Year from the entire imec team!

As you are all aware 2021 has been a challenge in many aspects. The Semiconductor Supply Chain is one of them.
The impact of the pandemic on the semiconductor ecosystem is significant and has led to quite some changes in the way of working for all of us. The wafer shortages and the medium-term forecasts at the large foundries have led to a stronger push into 12 inch technologies. The key reason for this is that most large foundries only plan capacity expansion on 12 inch, whereas 8 inch factories are also fully loaded but will not get further capacity investments.

This observation, together with the vision that innovation for the future will be more significant when using 12 inch technologies, has led to the decision that **TSMC will stop offering access to 8 inch technologies in the Europractice program as of September 2022**. This means that the last MPW/Mini@sic run on TSMC 8 inch Logic/Mixed-Signal or BCD will take place end of August 2022. The technology categories involved are all 180nm flavors and the 130nm flavors that runs on 8 Inch.

We realize that this is a very abrupt halt to some of the most popular technologies around and will provide guidance to the community to migrate to other relevant technologies of which a few examples are shown below;

We regret this decision that forces us to change our offering unexpectedly.
Despite the fact that we believe that this decision by TSMC is irreversible, we will do all that is reasonably possible to extend the support for ongoing critical projects.

In the case that this would not be possible, the Imec Europractice team will provide guidance towards the best possible technology for your future work.

Kind regards,
imec Europractice team

LArASIC Production Request

Number of ASICs Needed (assume 10% of spare FEMBs)

ASIC	FD1 (3,000 FEMBs)	FD2 (1,920 FEMBs)	FD1+FD2
LArASIC	26,400	16,900	43,300

Production request:

- Would like to submit an order for 250 wafers of LArASIC
- Each wafer has 310 P5b and 310 P5 chips
- Assume final yield of 80% → 65,000 P5b chips
- We are using the same mask as engineering run. There is an additional ~65K of P5 chips on the wafer
- Preliminary yield from engineering run:
  - Dicing and packaging yield is 98.7%
  - Warm test 366 P5b LArASIC with 2 chips failed, out of which ~200 were tested in LN2 with no failures

Documentation for this Review

REVIEW DOCUMENTATION (list in xlsx):

DUNE FD1 TDR (Chap 4: TPC Electronics)

DUNE FD2 CDR (Chap 4: Charge Readout Electronics)

ASICs Final Design Review (final report from Committee)

Requirements

LArASIC:

- LArASIC P5B Datasheet
- LArASIC Development Plan
- LArASIC Reticle (MOSIS)

Frontend Motherboard (FEMB) Schematics

QC test-board schematics (multi-ASICs)

ASICs Production and QC plans

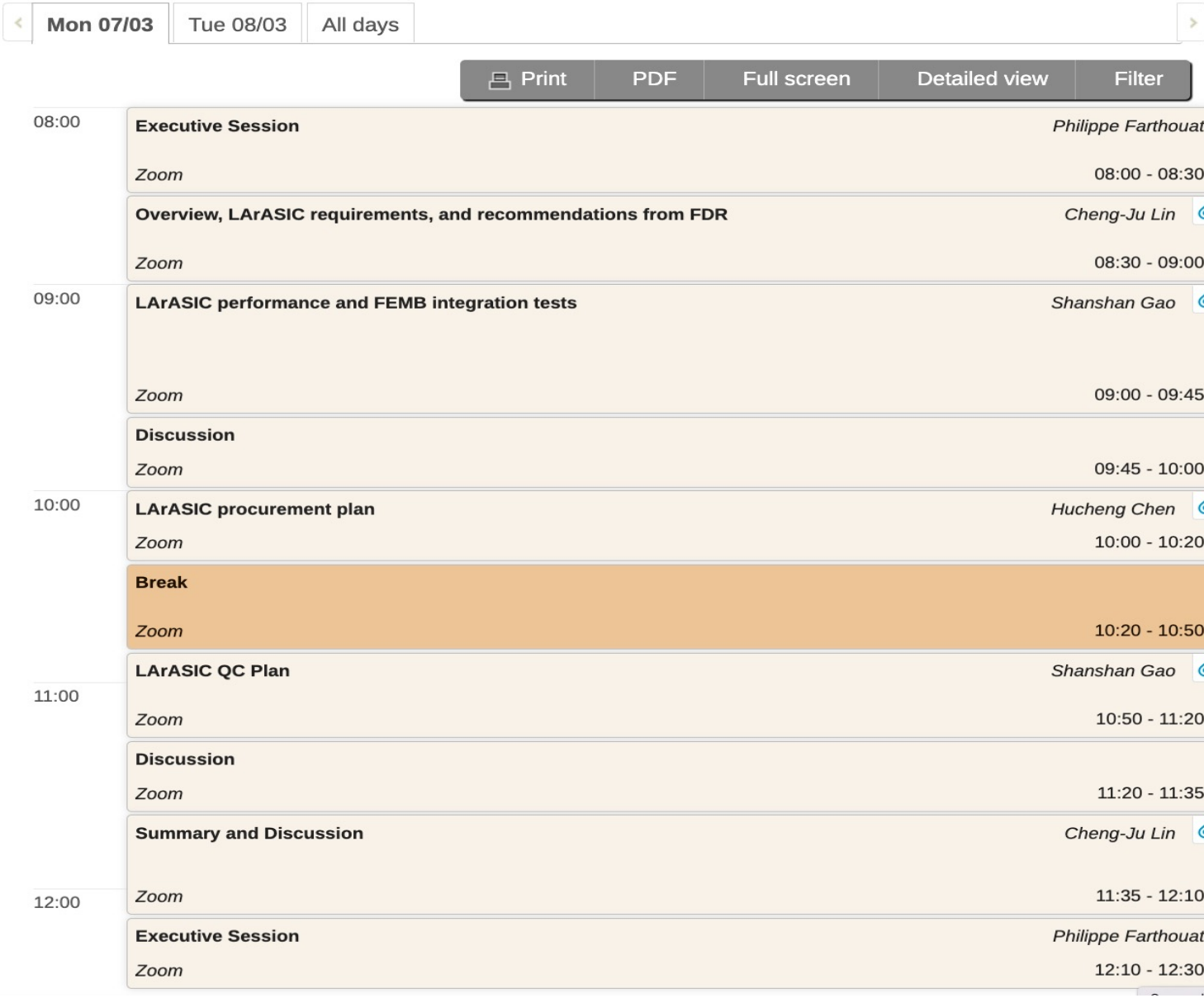
Institutional MOUs: FD1, FD2

Answers to recommendations from the final design review

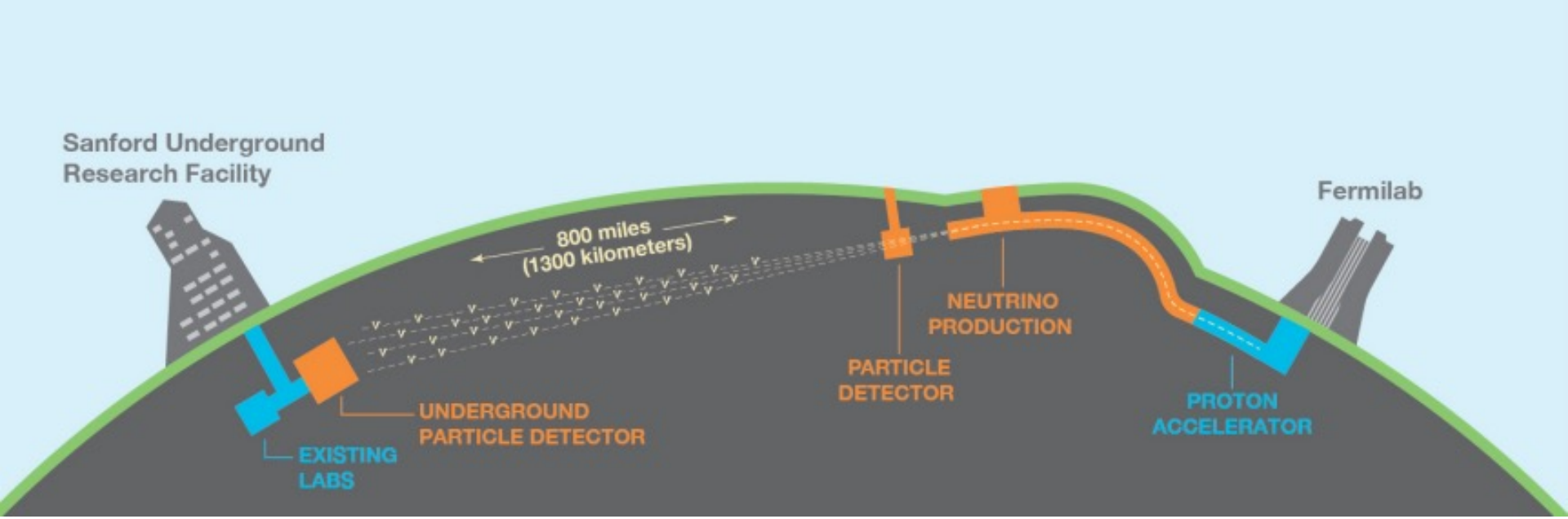
Link to the documentation page is provided on the Review homepage

https://indico.fnal.gov/event/53072/page/2862-review-documentation

Agenda for this Review

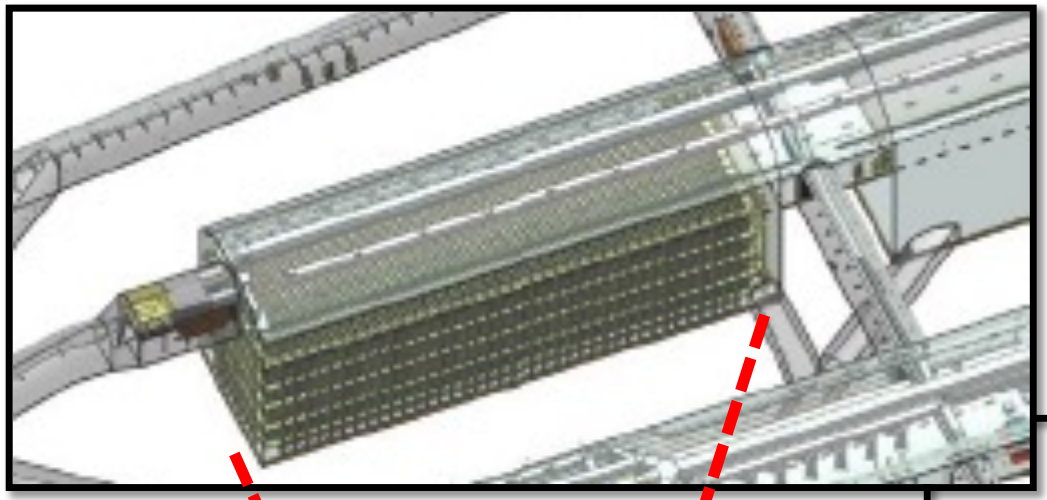


Deep Underground Neutrino Experiment (DUNE)



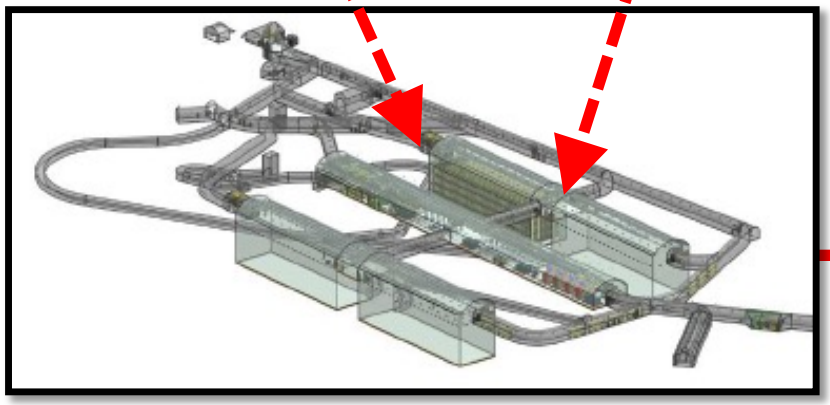
- Future flagship neutrino oscillation experiment
- Three major components: neutrino beamline, near detector, and liquid Argon far detector modules
- Broad physics program: BSM studies supernovae, solar neutrinos, three-flavor oscillation measurements
- >1300 people, > 200 institutions, 33 countries + CERN

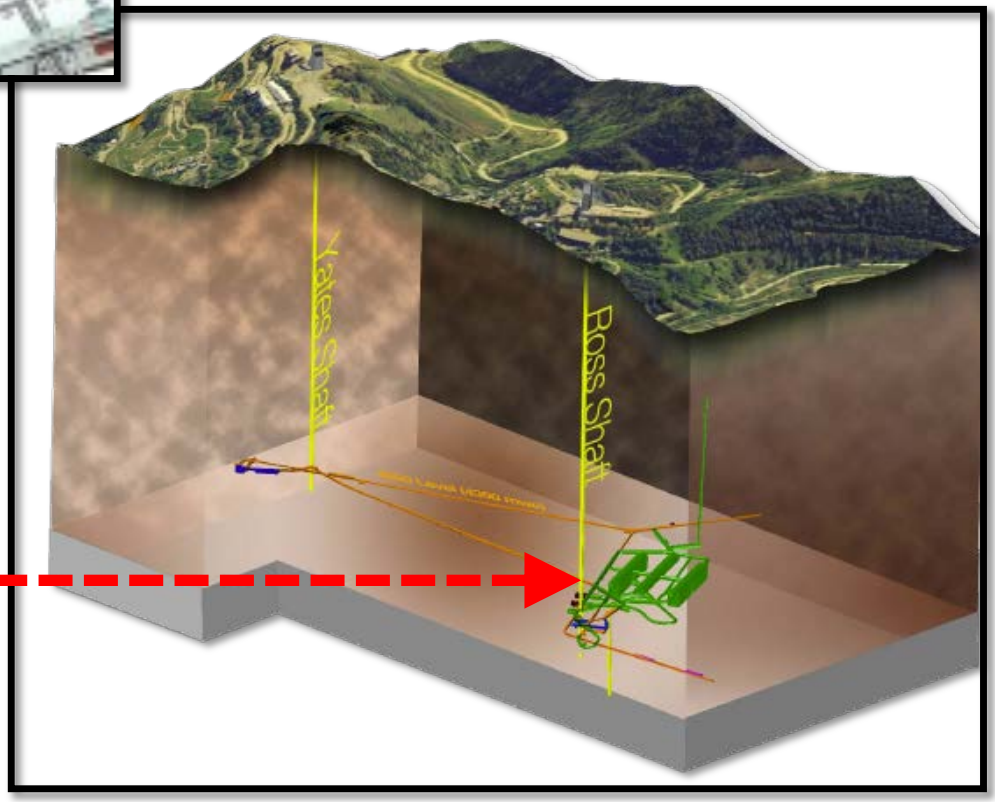
DUNE Far Detectors



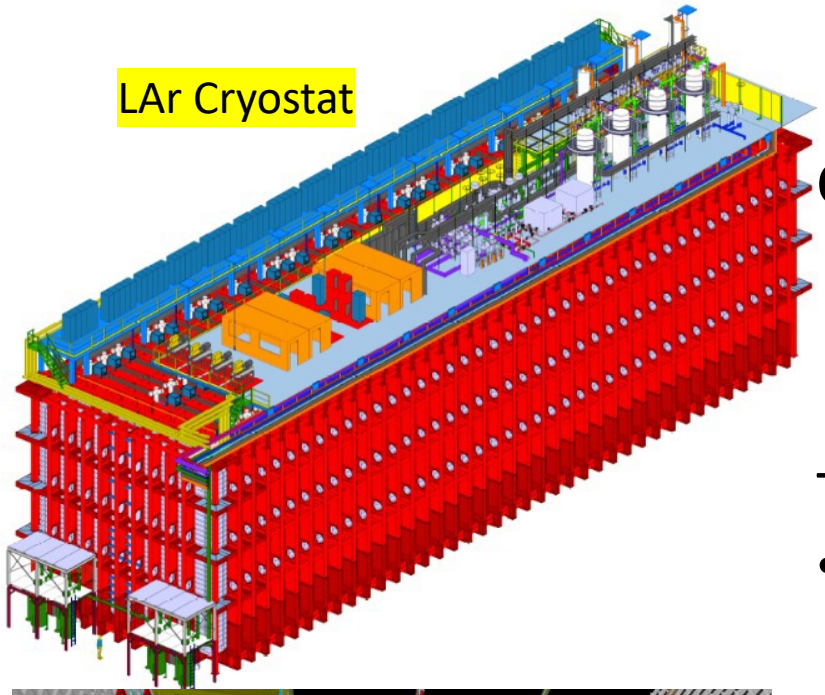
Four 10-kTon (fiducial) liquid argon detectors

~1500m underground



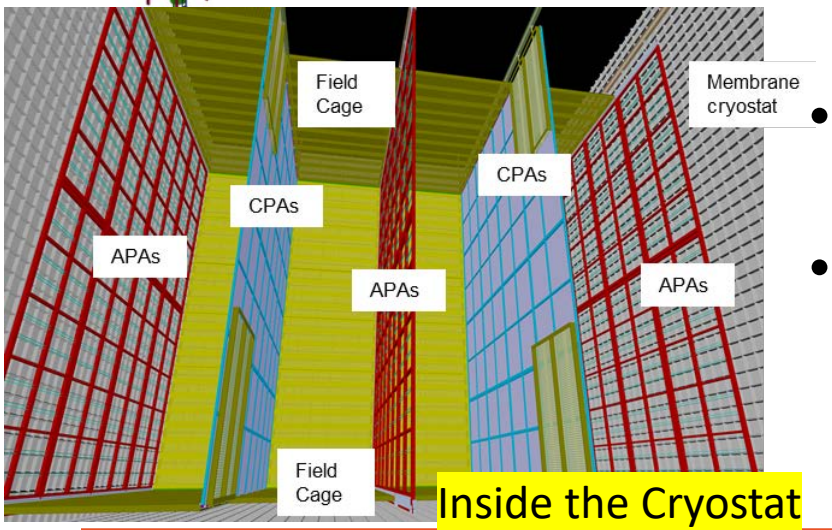


DUNE Far Detector #1



Cryostat dimensions:

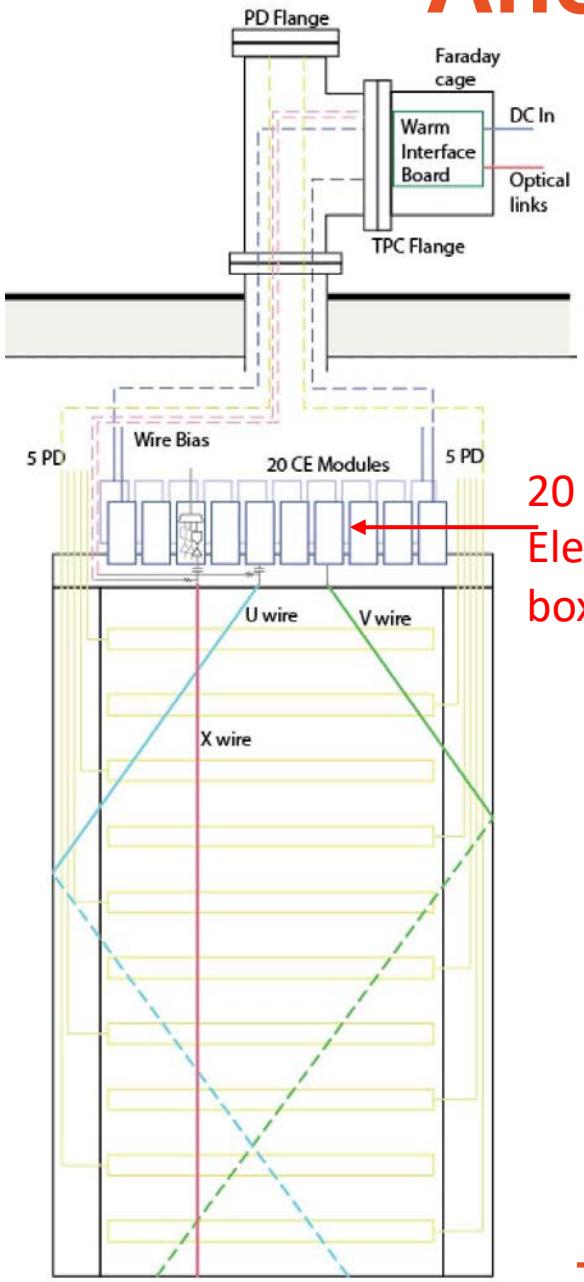
~65m (L) x 19m (W) x 18m (H)



Time Projection Chamber (TPC) Elements:

- Anode Plane Assembly (APA). Sense wires for detecting drift electrons in the TPC
- Cathode Plane Assembly (CPA) at -180kV. Electron drift field of 500V/cm
- Distance between CPA and APA plane = 3.6m (maximum electron drift distance)

Anode Plane Assembly (APA)

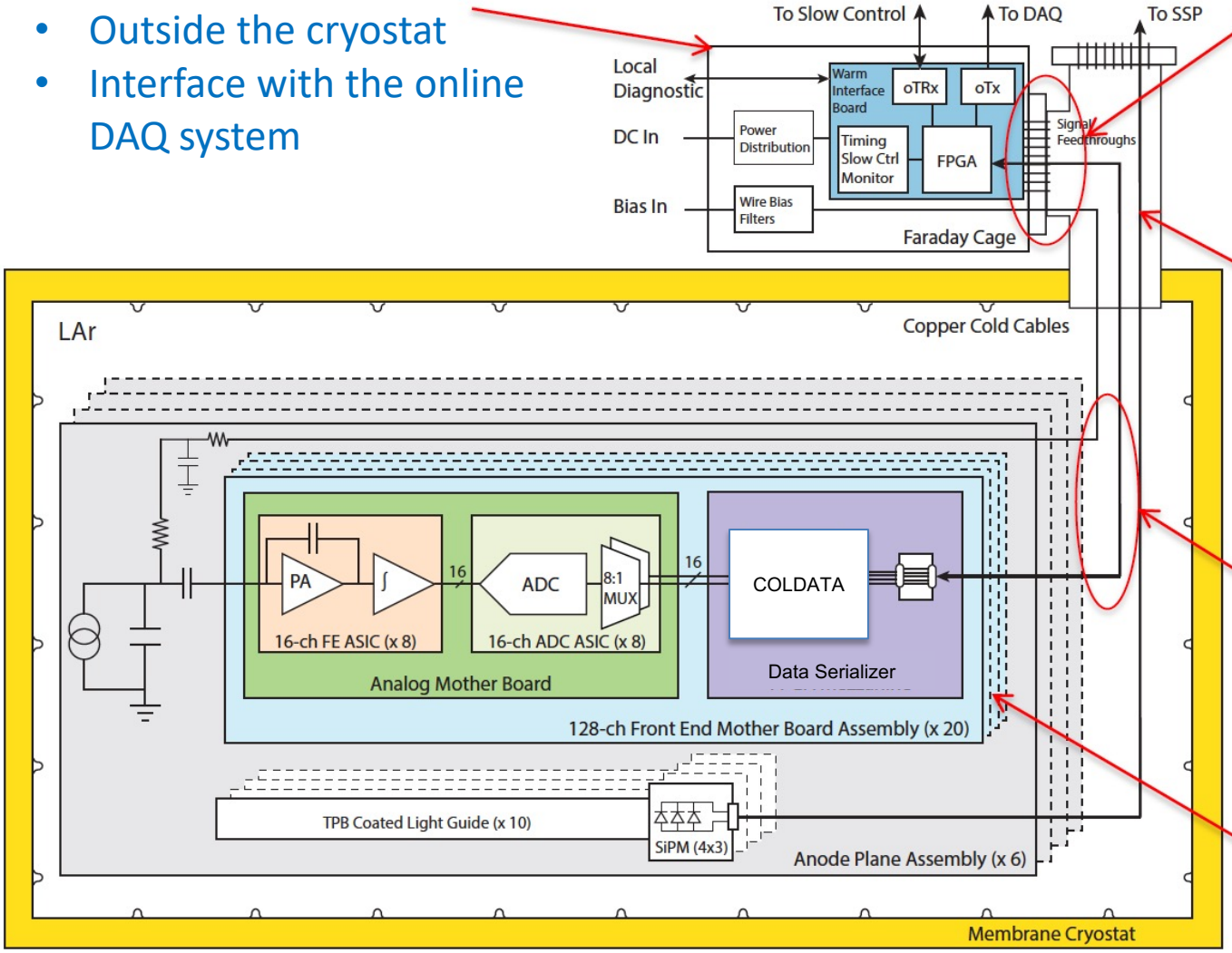


- Far detector #1 has 150 APAs
- Each APA has four wire planes:
  - 960 grid wires (un-instrumented)
  - 800 U (1st induction wires)
  - 800 V (2nd induction wires)
  - 960 X (collection wires)
- Readout electronics are integrated close to the sense wires on the APA and immersed in LAr to yield the best SNR → Cold Electronics
- 20 Cold Electronic (CE) Boxes are mounted on the top of each APA and connected to 2560 sense wires

TPC Readout Electronics

Warm interface electronics:

- Outside the cryostat
- Interface with the online DAQ system



CE Flange:

- On top of the cryostat
- Connect cold cables to the Warm Interface Electronics

Signal feedthrough:

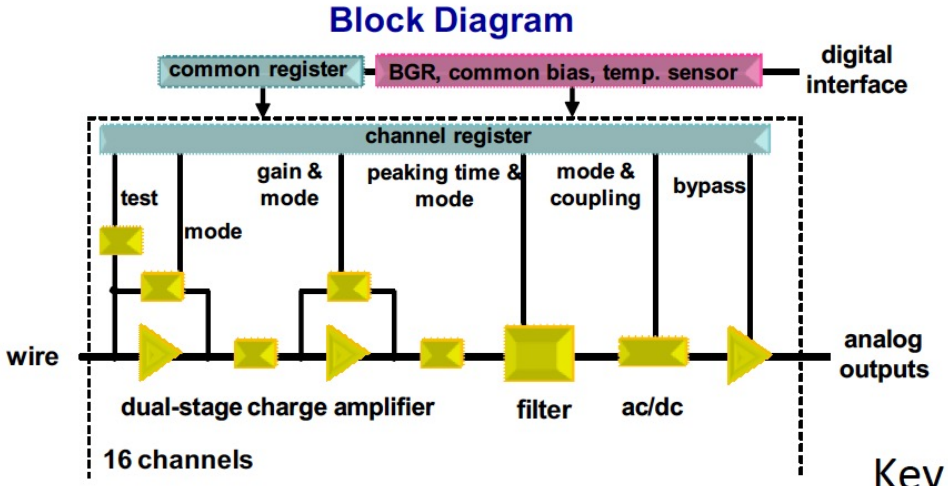
- 14” conflat
- Cable strain relief

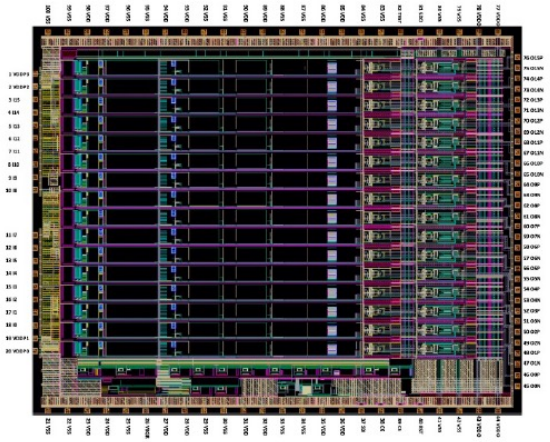
Cold cables:
Low voltage and data cable to Frontend motherboard

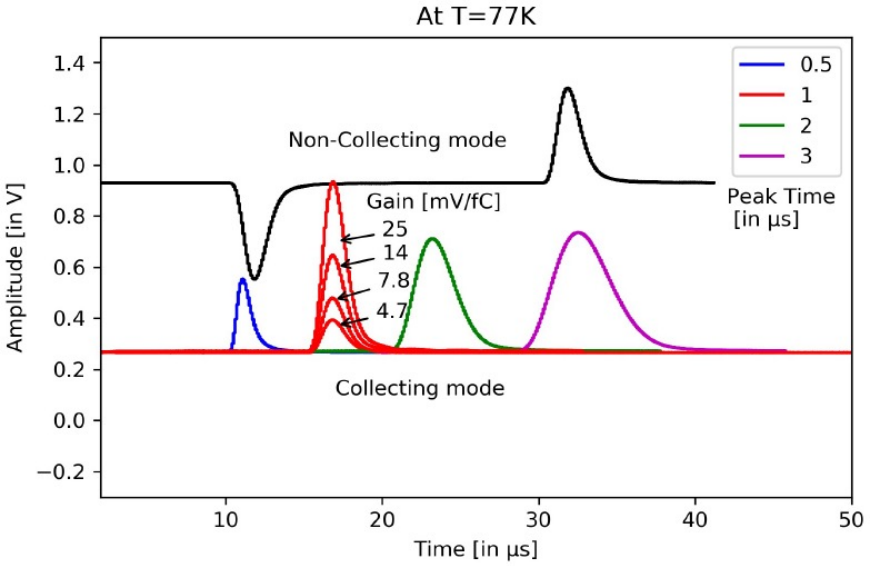
Frontend Motherboard (FEMB): 128 channels of digitized wire readout enclosed in CE box

LArASIC ASIC

16-ch programmable charge amplifier working at 77-300K for neutrino experiments





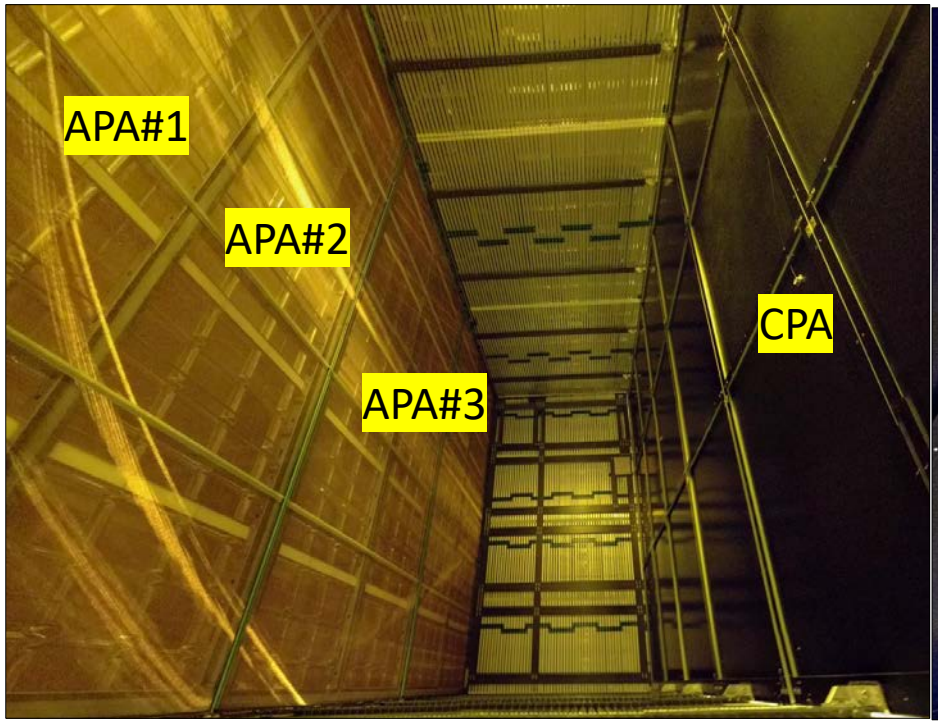


Measured waveforms at cold

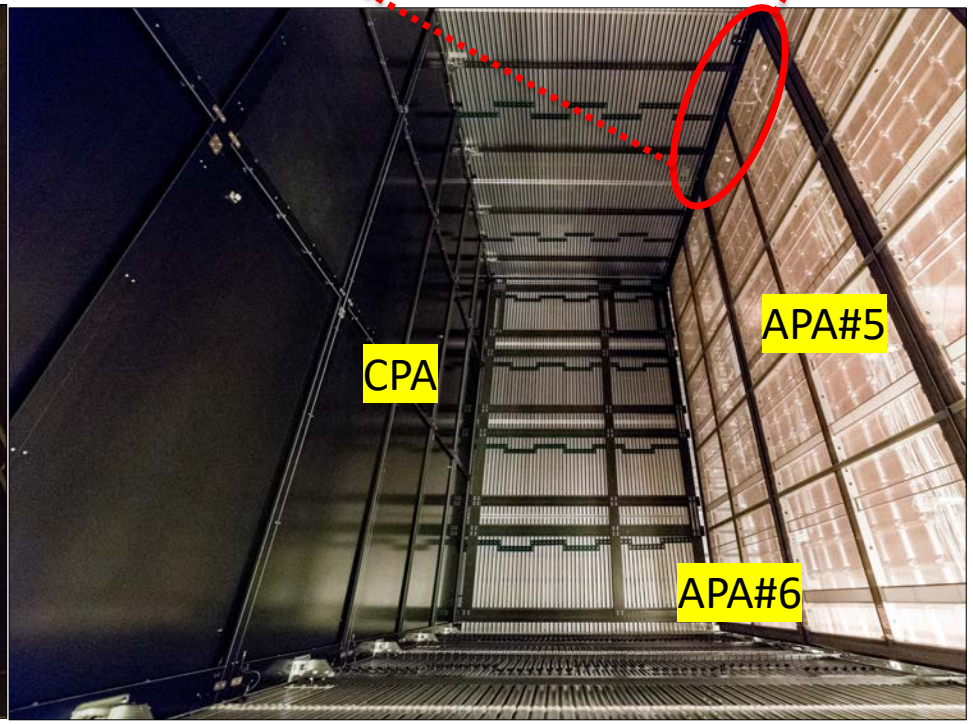
Key Features

- Two-stage charge amplifier, high-order filter (5th)
- Adjustable reset quiescent current settings
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC
- Adjustable peaking time: 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode
- Rail-to-rail analog signal processing
- Bandgap referenced (BGR) biasing circuits
- Integrated temperature sensor
- Integrated 6-bit adjustable range pulse generator
- SPI interface for 144 configuration registers
- Technology CMOS 0.18 µm, 1.8V
- Leverages the existing cold models

ProtoDUNE-1 operated in LAr for about 2 years



Beam-Right TPC Volume

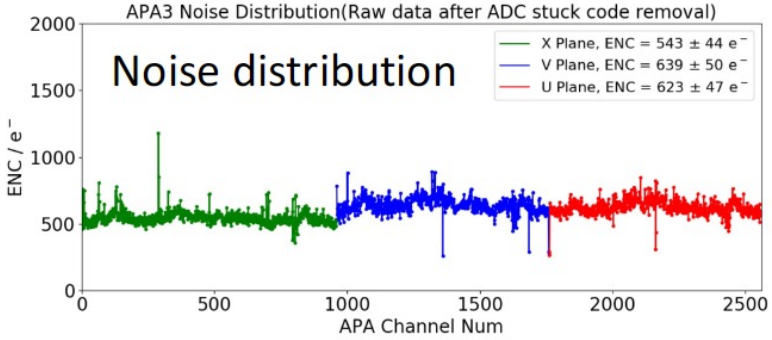


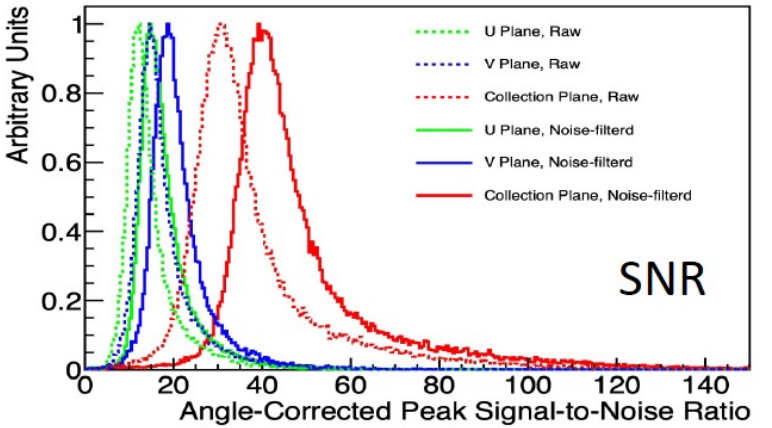
Beam-LEFT TPC Volume

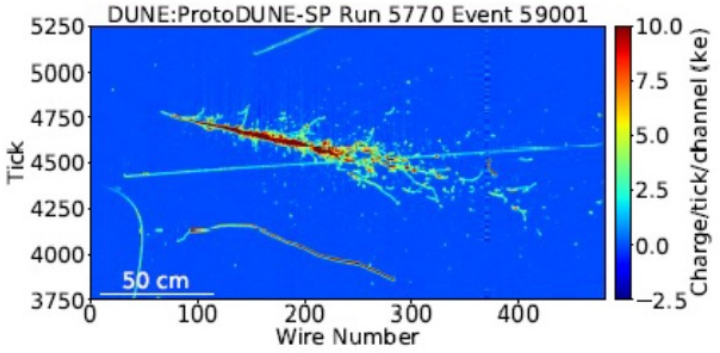
BERKELEY LAB DUNE

ProtoDUNE Run-1 Performance

- **High yield**
  - 99.74% (15320 of 15360) of TPC channels are active
    - Only 4 inactive cold electronics channels when commissioning started
    - 2 more inactive cold electronics after >1 year running
- **Low noise**
  - 92.83% TPC channels are good with excellent noise performance
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
- **Good stability**
    - No measurable degradation is observed over a year
- CE is demonstrated as the promising technology towards DUNE LArTPC
  - Final design will be verified in ProtoDUNE-SP RUN-II in 2022

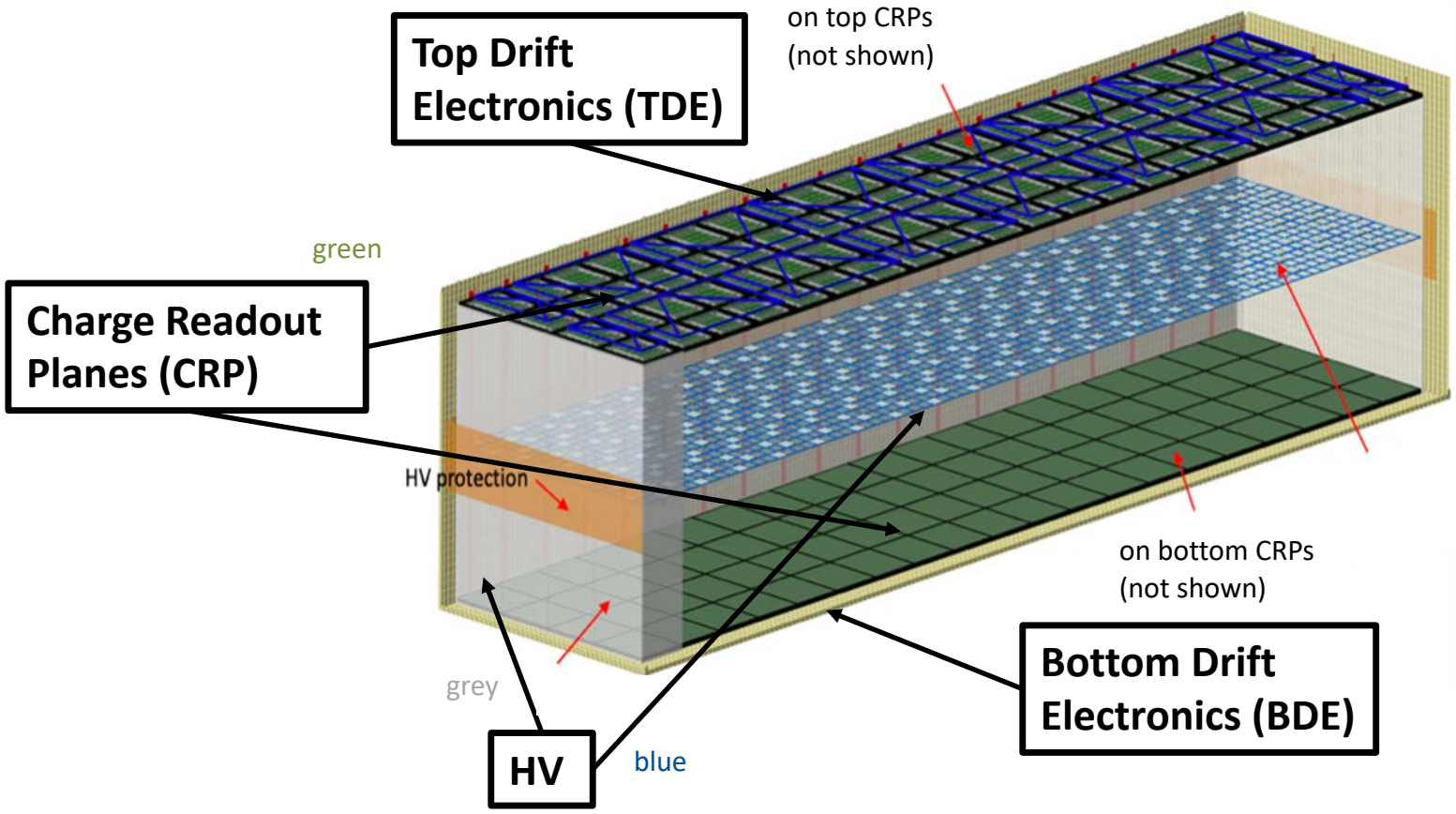






A 6 GeV/c electron candidate

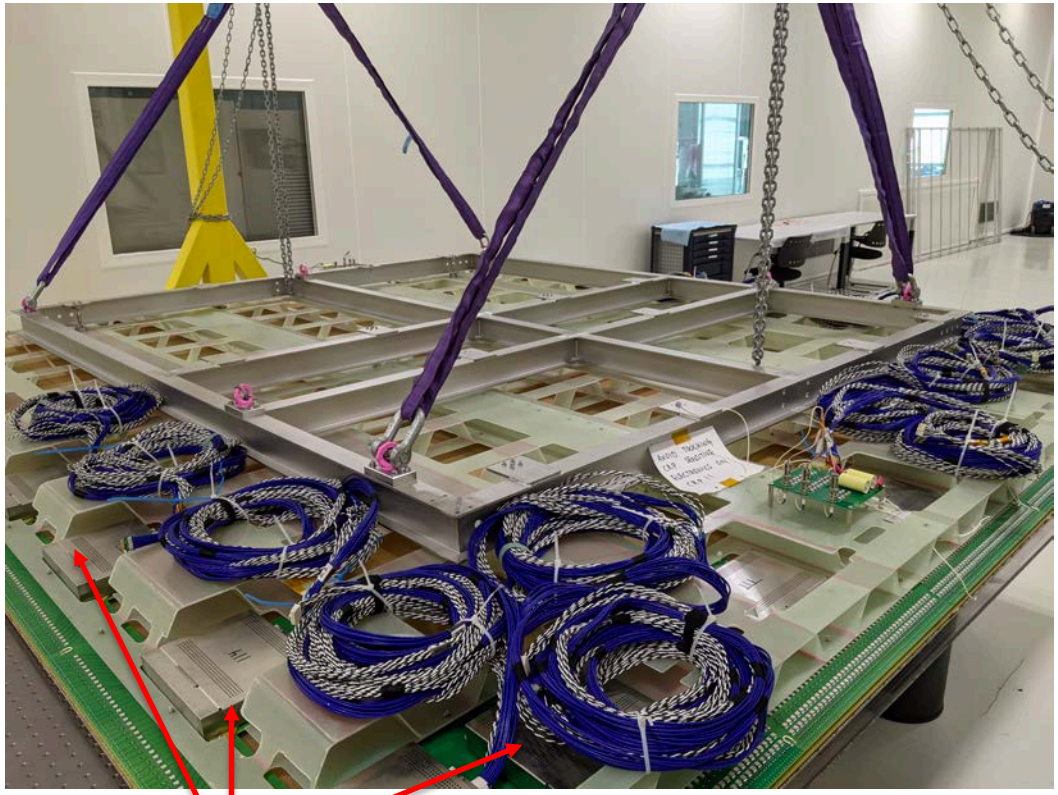
DUNE Far Detector #2



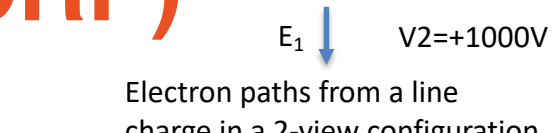
Readout electronics for the 80 CRPs on the bottom drift volume are the same as the readout electronics for FD1

FD2 Charge Readout Plane (CRP)

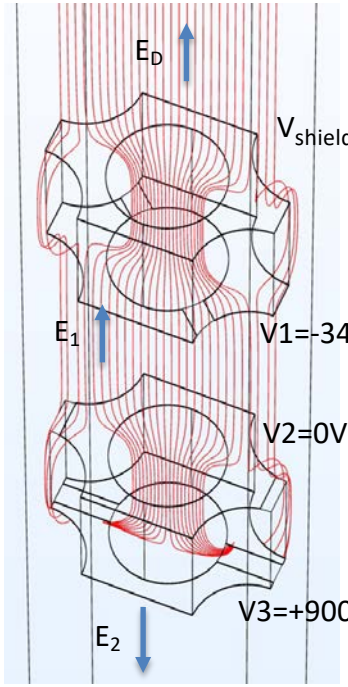
- Replacing wires with copper strips on PCB
- Perforated PCB allows electrons to drift through the induction planes



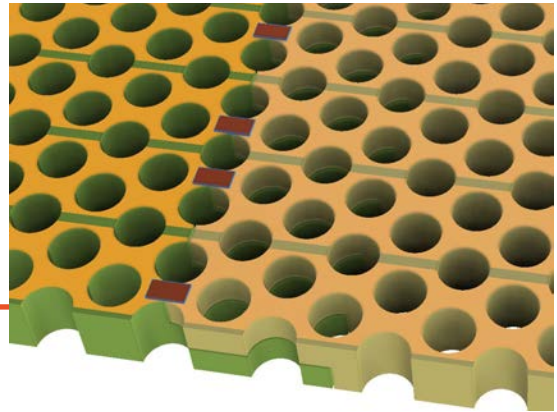
Same FEMB as FD1



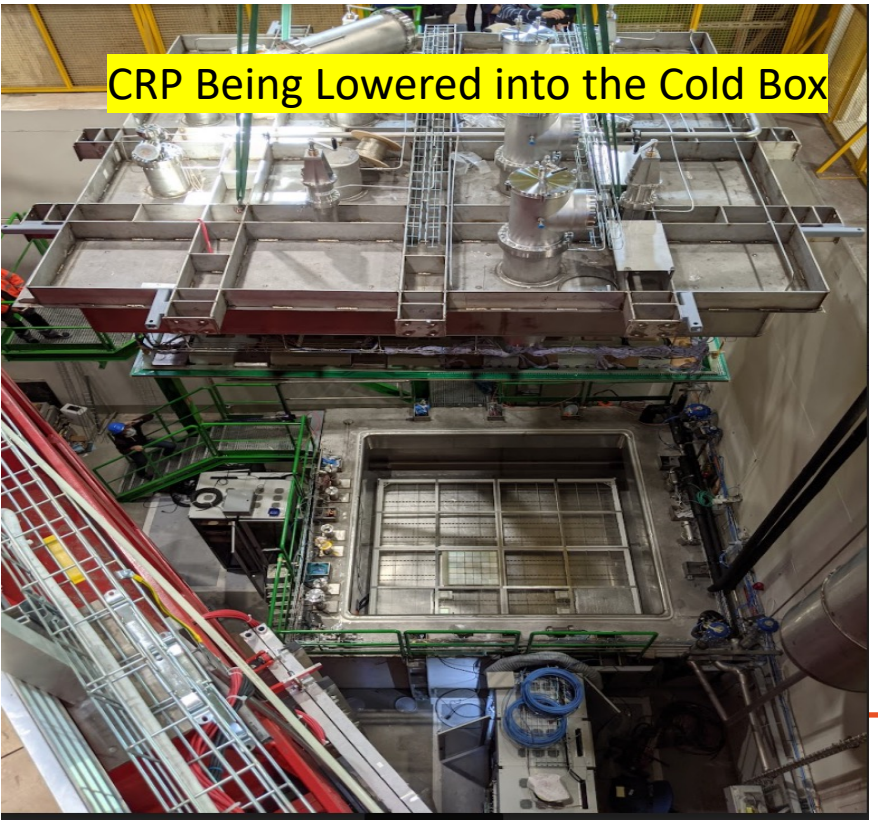
Electron paths from a line charge in a 2-view configuration

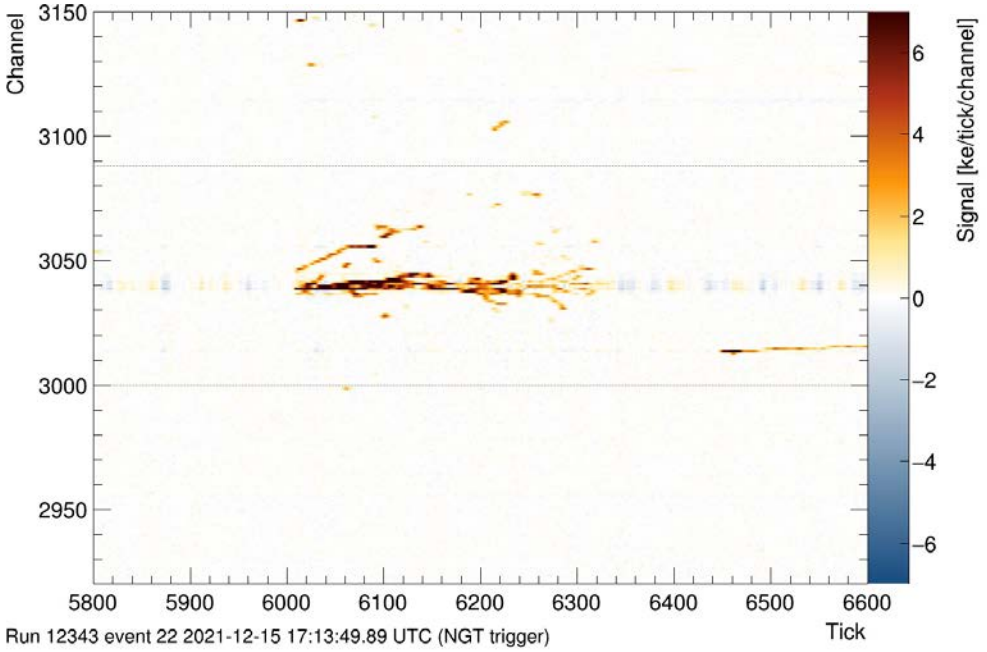


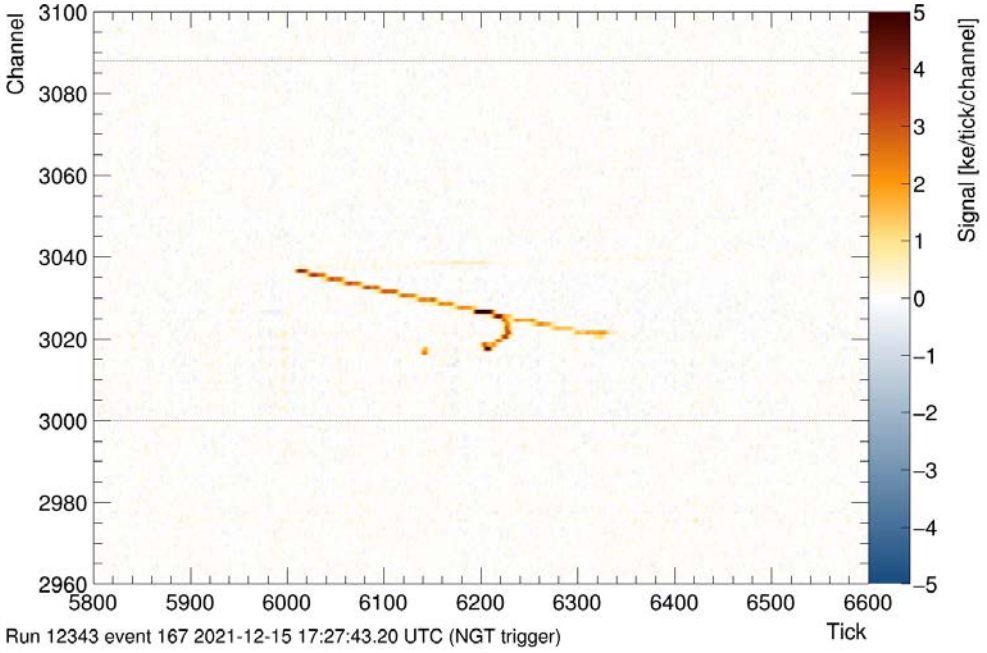
Electron paths in a 3-view configuration with a shield plane facing the cathode.



CRP Cold Box Test at CERN







LArASIC Requirements

Complete set of TPC electronics requirements is in EDMS#2397298

Requirements relevant for LArASIC:

- System noise < 1,000 e^-
- Frontend shaping time adjustable in the 1-3 μs range
- Input capacitance optimized for 120 to 210 pF
- Signal saturation level 500,000 e^-
- Two baselines in the FE amplifier
- Gain: ~ 10 mV/fC
- Power consumption < 50 mW/channel
- Monotonic saturation recovery after large pulse
- Channel-to-channel crosstalk < 1% (goal of <0.1%)
- Double pulse resolution ~ 5mm
- Fraction of dead channels < 1% over lifetime

LArASIC P5 and P5b meet all requirements → See S. Gao's presentation

(Note: Lifetime study was performed using earlier version of LArASIC. Will repeat the study using P5b)

Recommendations from FDR (i)

Status of the recommendations are tracked in EDMS#2708343

Four recommendations are relevant for LArASIC

1) **Go ahead with the engineering run production:**

   Engineering run was completed. A total of 12 wafers were produced and 6 wafers packaged. The packaged chips were delivered in early January 2022

2) **Actively continue the tests with the new FEMB:**

   One FEMB was modified to use ASICs (LArASIC P5B+ColdADC P2+COLDATA P4) from the engineering run. See S. Gao's presentation for the results.
   6 new FEMBs are expected to be delivered this week (28 Feb) from the assembly house

Recommendations from FDR (ii)

3) QC plan should include routine, detailed, qualification of the test equipment to validate the ASIC test procedure. Since the test sockets are known to have reliability issues, a cleaning procedure might be explored for sockets and possibly for chip leads prior to insertion in sockets:

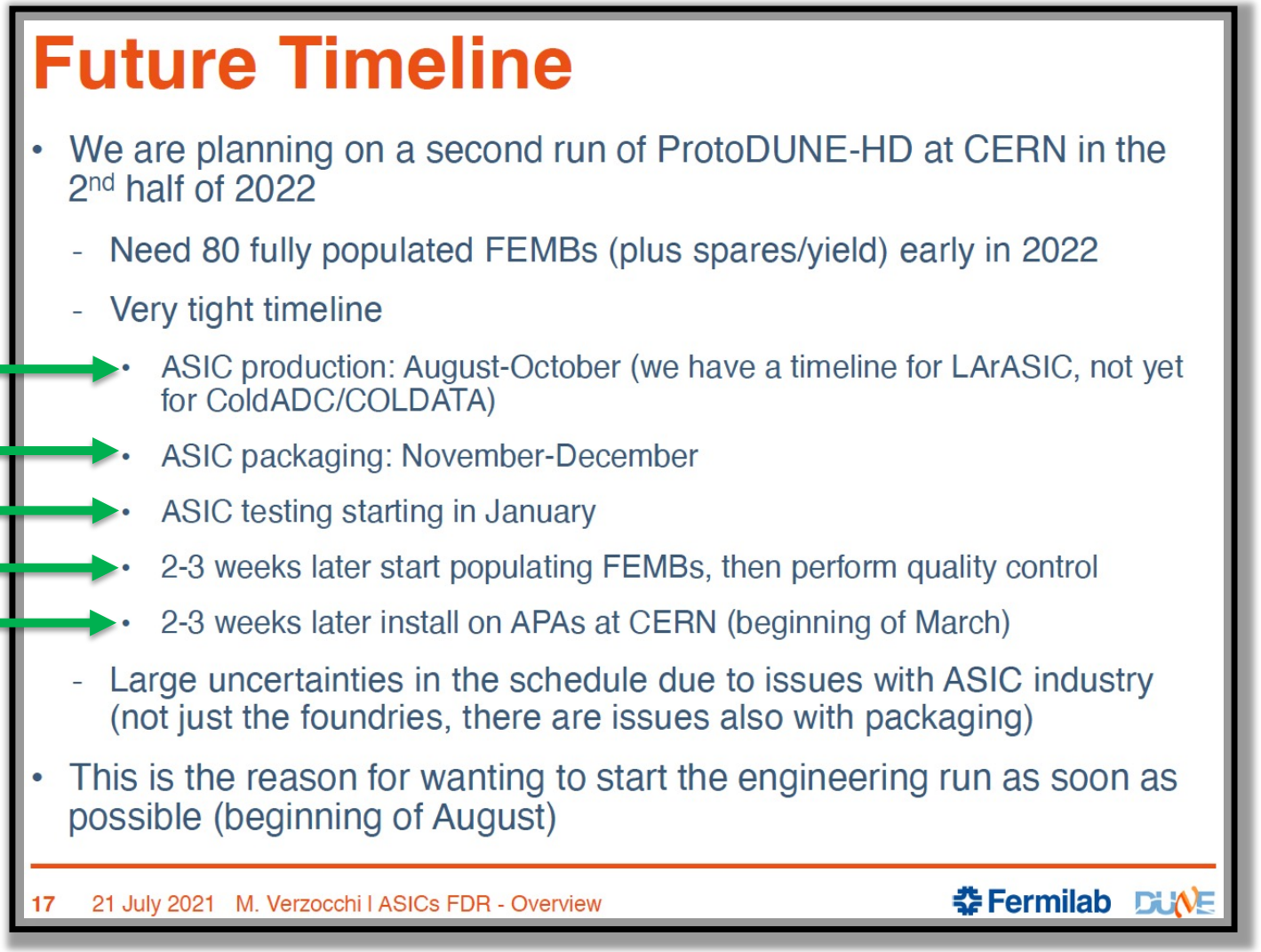
- Plan to include a set of reference ASICS at QC sites to perform routine qualifications of the equipment
- Sockets are implemented in mezzanine so they can be easily replaced in case of reliability issue is confirmed
- Exploring cleaning procedures that can be implemented as part of the QC
- Status of this recommendation: ongoing

Recommendations from FDR (iii)

4) **A cost analysis should be done:**
   a) **Perform cold testing on a small sample of every new batch to understand the quality of the ASIC batch**
   b) **Assume no significant issues found, perform warm testing of the rest of the batch and assemble on FEMB. Cold test FEMB and over produce 15 – 20% of FEMBs to account for failures:**

- We plan to follow the recommendation of the Committee to minimize costly cold testing on all the ASICs if the yield is found to be high
- Based on a sample of 350 warm tested LArASIC P5b from the engineering run, the yield is >99%. Out of which ~200 chips have also been tested in LN2 with 100% yield
- Status of this recommendation: ongoing

Plan Presented at the FDR (July 2021)



DONE

DONE

In progress

In progress

Current CERN schedule begins in late March

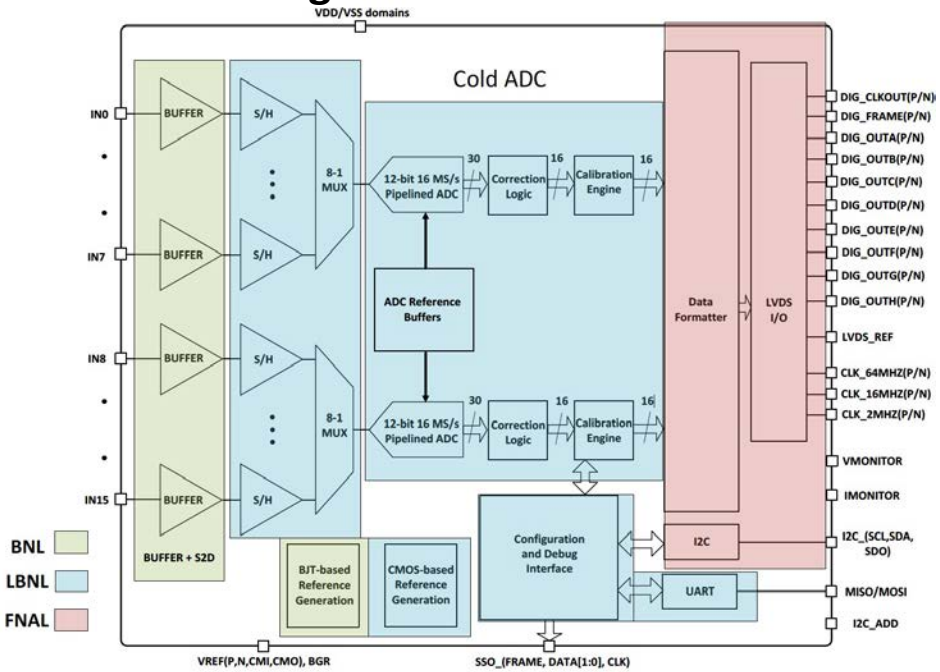
BERKELEY LAB DUNE

Thank You !

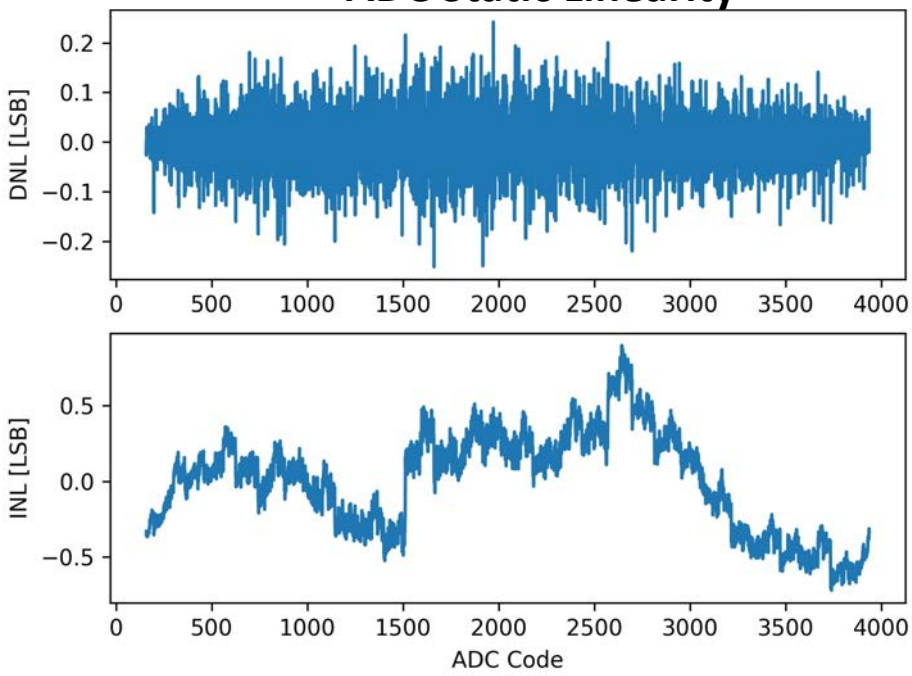
BACKUP SLIDES

ColdADC ASIC

ADC Block Diagram



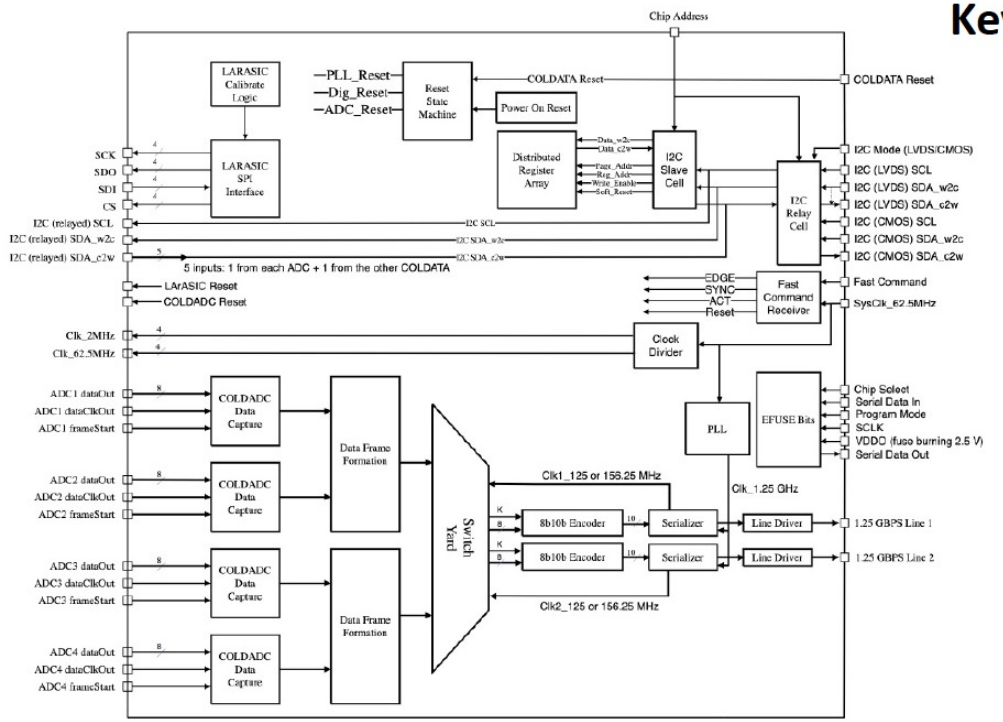
ADC Static Linearity



Key Features

- 16-channel, 12-bit 2MS/s digitizer ASIC for 77-89K
- Two 15-stage piped-line ADCs
- Designed by joint team from LBNL, FNAL, and BNL
- Low-noise and long lifetime operation in LAr
- 65nm CMOS process, 9 metal stack
- Digital self-calibration for interstage gains
- Chip size: 6860 μm x 7610 μm

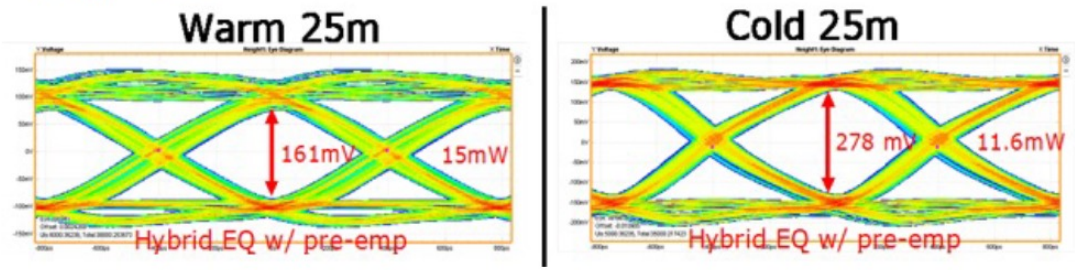
COLDATA ASIC



Key Features

- Designed by Fermilab and SMU
- Design for cryogenic, long lifetime operation
- Control 4 ColdADCs and 4 LArASICs
- Accept data from 4 ColdADCs
- Format ADC data (truncate to **12 or 14** bits) & pack into an array of 8-bit words
- Combine packed arrays from pairs of ADCs into 2 output data frames
- Encode the output data using 8b10b
- Drive the output data to a WIB at 1.25 Gb/s
- Digital-On-Top design methodology
- 65nm CMOS process, 9 metal stack
- Chip size: 7730 µm x 7730 µm
- Leverages the existing cold models

BER < 10^{-15}



Line driver eye diagram measurement result