4-Dimensional Trackers

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1 Introduction

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Precision Timing information at the level of 10-30ps is a game changer for detectors at future collider experiments. For example, the ability to assign a time stamp with 30ps precision to particle tracks will allow to mitigate the impact of pileup at the High-Luminosity LHC (HL-LHC). With a time spread of the beam spot of approximately 180ps, a track time resolution of 30ps allows for a factor of 6 reduction in pileup.

Both ATLAS and CMS will incorporate dedicated fast-time detector layers for the HL-LHC upgrade [1, 2]. Timing information will be even more important at future high energy, high luminosity hadron colliders with much higher levels of pileup. For example, one of the key challenges at a future 100 TeV p-p hadron collider will be the efficient reconstruction of charged tracks in an environment of unprecedented pileup density. A powerful way to address this challenge is by fully integrating timing with the 3-dimensional spatial information of pixel detectors. An integrated 4-dimensional tracker with track timing resolution at the levels of ∼10ps can drastically reduce the combinatorial challenge of track reconstruction at extremely high pileup densities [3].

While timing information will be critical to mitigate the impact of pileup, it is not the only way in which it will enhance the event reconstruction of future hadron and lepton colliders. Timing information offers completely new handles to detect and trigger on long-lived particles (LLP) [2, 4], expand the reach to search for new phenomena by providing new handles on the data [2], and enabling particle-ID capabilities for pion/kaon separation at low transverse momentum [2]. 4D devices with coarse timing capabilities at ∼ns level but with similar granularity as regular tracking devices at the other end of 4D phase space can complement the fast timing layers for an enhanced overall 4D tracking.

The optimal design of future 4D trackers will involve three key considerations: sensors with adequate spatial and time resolution, low power and low noise readout electronics, and overall detector layout, including material considerations. Significant R&D is required to understand how to best design 4D trackers and how all these aspects will impact physics performance.

The following sections describe specific considerations for the integration of timing within tracking detectors at various future collider detectors and upgrades of existing experiments.

1.1 Hadron colliders: HL-LHC and FCC-hh

Valentina Maria Martina Cairo

The Inner trackers of the ATLAS and CMS Experiments at the Large Hadron Collider (LHC) will be upgraded to cope with the extreme conditions of the High-Luminosity phase of the LHC, currently foreseen to take place towards the end of 2027.

[Add something about CMS?]

The CMS Experiment is planning to install a MIP Timing Detector (MTD) with different sensor strategies in the barrel and endcap regions. The barrel will rely on scintillator crystals and silicon photomultipliers, whereas the endcap timing layer (ETL) will consist entirely of silicon sensors. [2]

Jenni: The motivation and physics cases for the CMS timing detector endcap are essentially the same as for ATLAS, so perhaps this section can just be combined for the two experiments. J: I think CMS also estimates that the inner tracker/pixels need to be replaced after some years in the HL-LHC, but I don't know if it has been planned to include timing also in the IT at that point.

The ATLAS Inner Detector, currently based on both silicon and gaseous technologies, is planned to be replaced by a full-silicon Inner Tracker (ITk) [5, 6]. ATLAS will also be installing a High Granularity Timing Detector [1] in the forward pseudorapidity region, which will help mitigate the effects of pileup interactions and distinguish between collisions occurring close in space but well-separated in time. Due to the high radiation dose in proximity of the interaction point, the two innermost pixel layers of the ITk will have to be replaced after a certain number of years of data taking. This represents a unique and exciting opportunity for the physics community to study the impact that fast-timing through 4D tracking would have on challenging physics cases (Higgs pair production, Vector Boson Fusion production of Higgs bosons decaying to invisible particles, etc) if used in the ATLAS barrel region. This would allow to bring in technological innovation and fully exploit the potential of HL-LHC by complementing the capabilities of the HGTD. Even a single pixel barrel layer with timing capabilities could be a vast improvement in terms of performance and physics results, but detailed simulation studies are needed to evaluate the potential of such detector layout and eventually probe its feasibility. The time resolution needed to substantially boost the ATLAS performance is to be evaluated along with the amount of material introduced in the tracker with the usage of 4D silicon modules by means of tracking performance feat as well as more complex objects such as b-jets.

Beyond HL-LHC, one of the key challenges in the design of Future hadronic Circular Colliders (FCC-hh [7]) arises from an increased number of pile-up events O(1000), up an order of magnitude more than at the HL-LHC. This implies that particle tracking and identification of vertices based on traditional 3D tracking would be extremely difficult, making a very clear case for the usage of 4D technology in all tracking layers. In fact, with trackers providing timing information, in addition to the longitudinal position measurement, the pile-up discrimination power opens up in 2 dimensions, time and space, and one key question to answer is again what timing resolution per track is needed. As shown in Fig. 1, studies on primary vertexing at the FCC-hh demonstrate that 2D vertexing with an extreme timing resolution of 5 10 ps per track is essential to keep the levels of effective pile-up[1] under control at large pseudorapidities ($|\eta| > 3$) which would otherwise reach level of tens or hundreds leading to large merging effects in vertex reconstruction and large confusion in vertex selection.

At the same time, the higher energies and luminosities typical of the FCC-hh, pose very stringent constraints on the detector design itself, for instance on the radiation hardness of the silicon modules, limiting either the lifetime of the inner detector or the number of suitable technologies.

[1]Effective pile-up is defined as the number of pile-up vertices which effectively lead to a confusing assignment of low p_T tracks to the original primary vertex

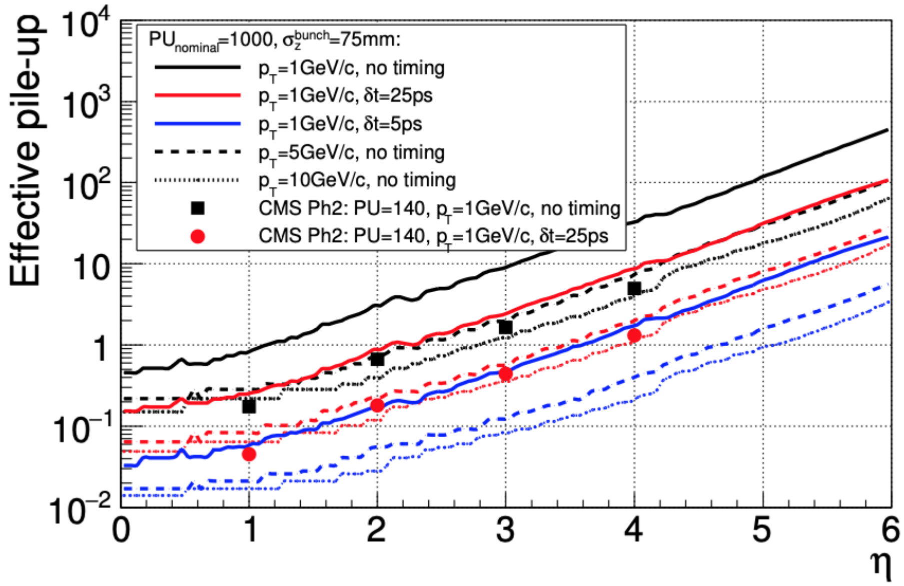

Figure 1: From Ref. [8]. An effective pile-up in the FCC-hh tracker. Several options of timing resolution per track in 2D vertexing are assumed: no timing (black), δ t = 25 ps (red) and δ t = 5 ps (blue). Several p_T values are shown: 1 GeV/c (solid), 5 GeV/c (dashed) and 10 GeV/c (dotted). For reference the effective pile-up for CMS Phase 2 layout, p_T = 1 GeV/c and nominal pile-up=140 is added.

In the layouts under study [7], the beampipe is supposed to have a radius of 20 mm, and at 25 mm the radiation levels are of the order of 0.4 GGy after 30 ab^1 and approximately 1 MeV neq fluence (6×10^{17} per cm^2), which corresponds to approximately 30 times (600 times) more radiation compared to HL-LHC (LHC), making none of the existing technologies suitable, but rather requiring dedicated Research and Development efforts targeting extreme timing resolutions and radiation hardness.

1.2 e^+e^- colliders: ILC, CLIC, C^3 (?)

Valentina Maria Martina Cairo, Lucie Linssen

The usage of 4D tracking technology at e^+e^- colliders is subject to very different conditions compared to that of experiments at hadron machines: both the numbers of collisions per beam crossing and the radiation levels are orders of magnitude lower, but the physics measurements are normally targeting very high precision, imposing track parameter resolutions to be extremely good, thus requiring very low passive material in the vertexing and tracking detectors.

Most of the studies performed so far focus on the usage of time at the ns resolution level as part of the object reconstruction chain, while studies of potential applications of precision timing at the ps level are still to be further investigated in e^+e^- colliders. Both aspects will be summarised below.

The International Linear Collider (ILC) [9] is a proposed 20 km e^+e^- linear collider at the energy frontier, with a initial baseline center-of- mass energy of 250 GeV. Two detector concepts have been studied at the ILC: the Silicon Detector (SiD) and the International Large Detector (ILD).

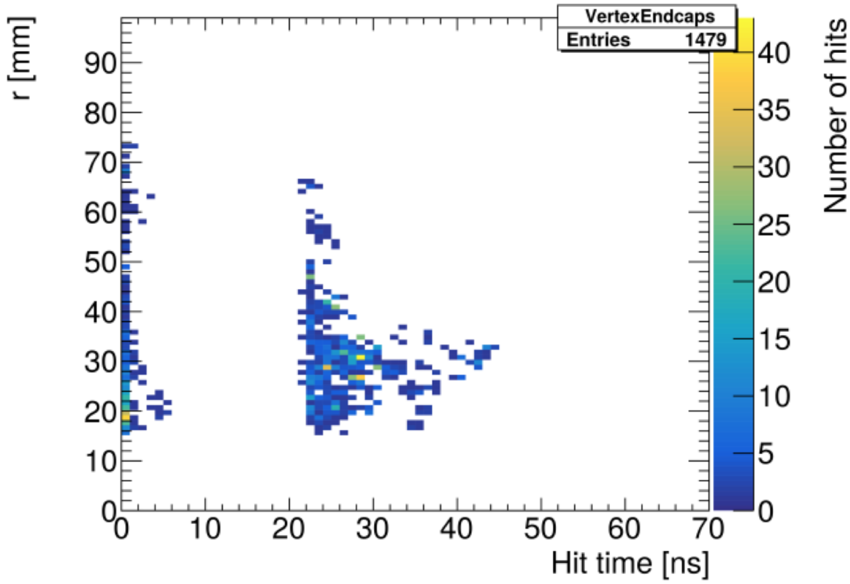

Figure 2: From Ref. [10]. The time distribution of beam background hits in the SiD Vertex Detector Endcap.

SiD is a compact detector based on a powerful silicon pixel vertex detector, silicon tracking, silicon-tungsten electromagnetic calorimetry (ECAL) and highly segmented hadronic calorimetry (HCAL). SiD also incorporates a 5T solenoid, iron flux return, and a muon identification system. The choice of silicon detectors for tracking and vertexing ensures that SiD is robust with respect to beam backgrounds or beam loss, provides superior charged-particle momentum resolution, and eliminates out-of-time tracks and backgrounds. The recent developments in fast-timing detectors could bring in improvements to the SiD layout, as described in Ref. [10]. Timing layers with resolutions at the level of the nanosecond could be used in the HCAL to help suppress backgrounds. Fig. 2 shows a clear distinction between the time of the collision hits and that of background hits.

Better time resolutions would instead make it possible to exploit time-of-flight (TOF) for low-momentum particle identification (PID) if timing layers were added to the tracking system or in between the tracker and the ECAL. Fig. 3 shows that, in SiD, a TOF system with time resolution of 10 ps allows for PID up to a momenta of a few GeV.

The ILD concept has been designed as a multi-purpose detector for optimal particle-flow (PFA) performance. Its tracking systems differs from the SiD one: a high-precision vertex detector is followed by a hybrid tracking system, realised as a combination of silicon tracking with a time-projection chamber (TPC). The complete system, along with a calorimeter, is located inside a 3.5 T solenoid.

Particle identification in the ILD can be carried out by the TPC using dE/dx information but studies have been conducted [11] on the possibility of improving PID via a TOF system. As a proof of concept a possible TOF estimator is computed, which uses the first ten calorimeter hits in the ECAL that are closest to the straight line, resulting from extrapolation of the particle's momentum into the calorimeter, assuming an individual time resolution of 100 ps per hit. Fig. 4 shows the complementary between dE/dx and TOF information at the ILD.

The momentum range in which the particle identification using TOF is effective depends on the time resolution. More detailed studies [12] show that smaller time resolutions do boost the PID reach in the low momentum regime, but the momentum range covered via TOF for PID remains

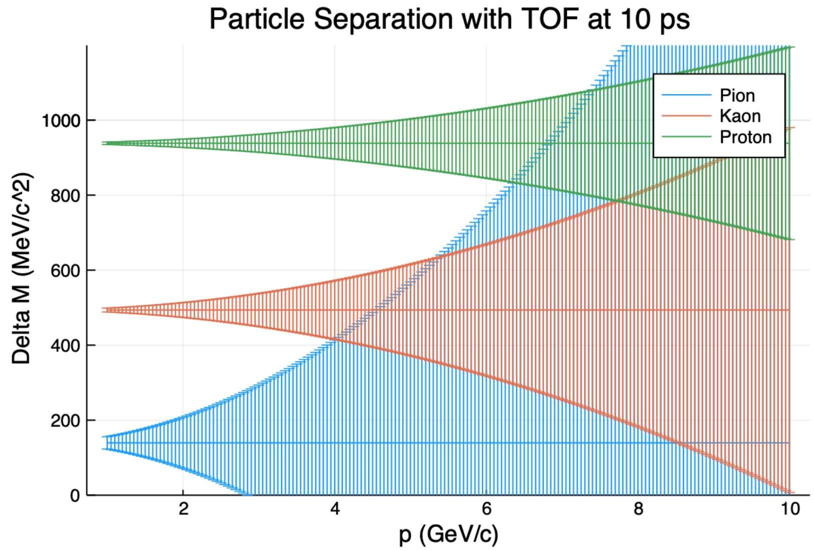

Figure 3: From Ref. [10]. Mass resolution for a time-of-flight system with a performance of 10 ps in SiD.

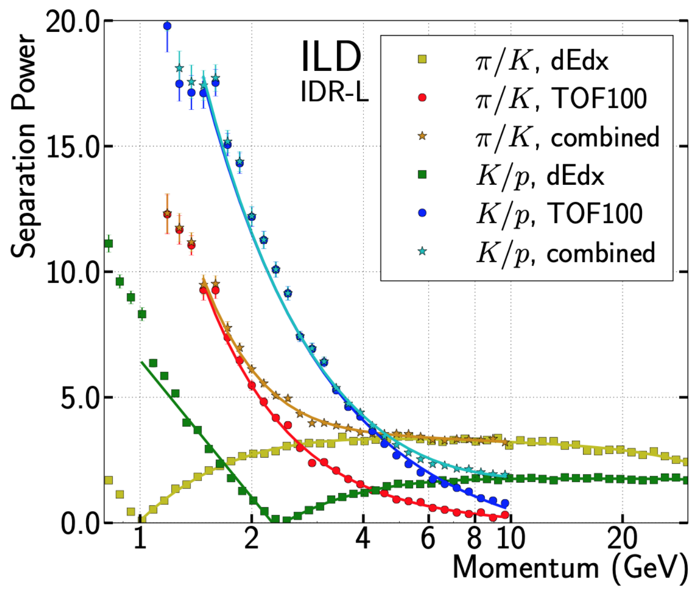

Figure 4: From Ref. [11]. Particle separation power for π/k and K/p based on the dE/dx measurement in the TPC and on a time-of-flight estimator from the first ten ECAL layers. The separation power obtained when the information from the two systems is combined is also shown.

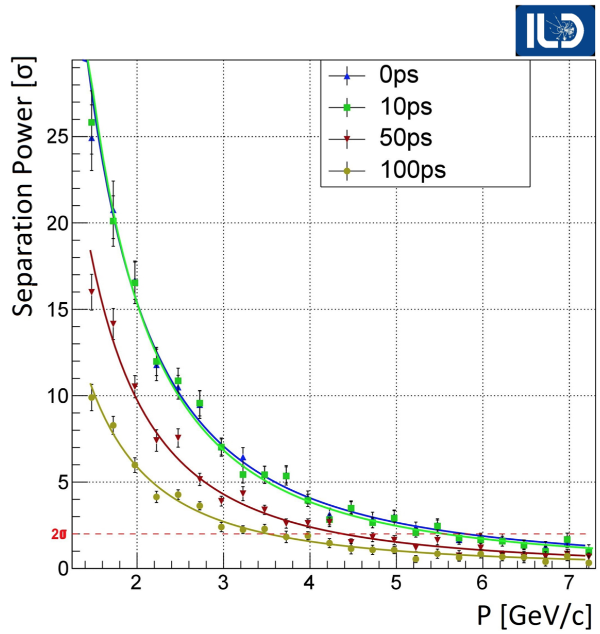

Figure 5: From Ref. [12]. Separation power between kaons and pions as a function of momentum assuming different time resolutions for a time-of-flight system in ILD.

limited, as one can see in Fig. 5. Dedicated PID detectors would have to be installed to discriminate pions from kaons at high momenta and more information about related studies can be found in [**?**].

The Compact Linear Collider (CLIC) [13, 14] is another proposed e+e- machine featuring a future multi-TeV collider. Two detector concepts are designed based on those studied for the ILC. The timing requirements at CLIC are driven by the levels to which the background degrades the physics performance of the detector. Assuming that the occupancies in the elements of the tracking detectors are sufficiently low that efficient track reconstruction is possible, there is unlikely to be a significant impact on the quality of the reconstructed tracks. Hence the main impact of the background will be on the reconstruction of jets. From detailed studies (see Section 2.5 in Ref. [13]) on the W-boson mass resolution in simulated $W \to qq$ decays, it was concluded that at CLIC the required hit-time resolution must be below 5 ns in the tracking and vertexing detectors and at most 1 ns in the calorimeters. This hit-time information is used during the reconstruction of particle-flow objects, which starts with track reconstruction by using only tracker hits within a 10 ns time window around the physics event and then combines them with information from calorimeter hits. As a result, all the particle-flow objects (charged and neutral) have sub-ns time resolution and this information can be used to remove particles from beam-induced background via both momentum and timing cuts as a function of the angular region and of the particle type.

Dedicated 4D tracking studies with ps-level resolution in some of the tracking layers have not yet been performed in CLIC. It has to be noted though that CLIC assumes to run at 380 GeV and above, thus the impact of fast timing in a TOF system is expected to have less added value for CLIC than for e^+e^- collisions at lower centre-of-mass energies.

1.3 Muon Collider

Hannsjörg Weber, Sergo Jindariani

Experiments at muon colliders have huge potential. A muon collider as a Higgs factory might allow to directly measure the mass and width of the Higgs boson at highest precision [15]. On the other hand, muon colliders have a potential to achieve collision energies of tens of TeV with a relatively small size for a collider ring, thus reaching way further than e^+e^- colliders and having a physics reach on-par with hadron colliders with hundreds of TeV in collision energy [16]. The current timeline to complete the accelerator R&D and be ready for the construction of a muon collider is estimated to be earliest in the latter part of the 2030s [17].

The major challenge for a muon collider experiment is that muons are unstable particles and naturally decay. The decaying muons within the colliding beams will create, for each beam crossing, a spray of hundreds of million particles entering a muon collider experiment. Out of those, an order of a million particles is charged. This multiplicity of particles entering the detector volume is expected after the muon collider experiment has already been shielded by so-called nozzles in the forward region, blocking the volume of $|\eta| \lesssim 2.5$. The background induced by these particles is commonly referred to as the beam-induced background (BIB) [18]. The BIB primarily consists of low energy photons and neutrons with a small fraction of charged hadrons, muons and electrons also present.

The presence of the BIB puts stringent requirements on a tracking detector. Firstly, the high number of particles entering the detector region leads to high levels of radiation and thus detectors need to be radiation hard, similarly to the detectors at hadron colliders. Secondly, hits produced by the BIB particles complicate data readout and make track reconstruction at the muon collider a very challenging task.

Yet, as the decay of muons is a stochastic process, several advantageous design aspects for tracking detectors can be thought of to suppress the impact of the BIB. Most of the BIB particles enter the detector from the two forward regions and do not originate in the collision area. Precise timing of detector hits would be able to reduce the BIB by a large fraction as we only need to consider hits consistent with the collision time. Furthermore, if timing of the hits can be correlated among adjacent layers of a tracking detector, a further filtering can be done by only considering hits consistent with being produced by the same particle. Initial studies indicate that single hit resolutions of 20-30 ps are sufficient to reduce the BIB to a manageable level. Additional suppression can be achieved if the tracker can obtain directional information, as for example is being done with the p_T modules of the CMS outer tracker upgrade for the HL-LHC [19]. Besides the requirements of precise timing and directionality, also a high spatial resolution is needed to achieve a low detector occupancy. Simulation studies show that small pixels at a size of about $(25\,\mu\mathrm{m})^2$ are needed at the innermost layers of a tracking detector while even at the outermost layers strips with length of at most few cm are required [20].

These requirements on small pixels/strips with precise timing and directional information will allow to not only handle the BIB, but will also enable a muon collider experiment to take high quality data for precision measurements and searches for new physics at highest energies [21]. Therefore, there is a high need of R&D efforts towards 4D (and 5D) tracking within the muon collider community.

1.4 Electron Ion Collider

Zhenyu Ye

The Electron-Ion Collider (EIC) [1] is a new accelerator facility to be built at Brookhaven National Laboratory in the United States. In 2031, the machine will begin colliding high-energy electron beams with high-energy proton and ion beams to study the spatial and spin structure of nucleons and nuclei. Due to the small *ep* and *eA* cross-sections, the collision rate at the EIC will be 500 kHz or less with a total particle production rate of about 4 million per second. Therefore, the requirement on the irradiation tolerance and occupancy of the detectors at the EIC will be considerably relaxed than those at the hadron colliders.

AC-coupled LGADs have been widely included in the submitted EIC detector proposals. In the barrel (endcap) region, precise timing and spatial information will be provided by single (double) layer of AC-LGADs for particle identification and track reconstruction, while in the far-forward (p/A-going) direction, AC-LGADs will be used to detect high-momentum hadrons near the beam line. These detectors need to provide a single hit timing resolution better than 30 *ps* and depending on the location a single hit spatial resolution between 15 to 150 μm. The detector designs need to incorporate low material budgets, e.g., $\sim 1\%\ X_0$ per layer in the barrel region. These impose a great challenge to the performance of AC-LGAD sensors, front-end readout ASIC, off-detector electronics, as well as the mechanical and cooling system design. A R&D project has been established to develop a common approach for these detectors so that they can share the same design to the extent possible.

[1] Science Requirements and Detector Concepts for the Electron-Ion Collider: EIC Yellow Report, BNL-220990-2021-FORE, JLAB-PHY-21-3198, LA-UR-21-20953, arXiv:2103.05419 (2021).

2 Sensor technologies

Simone Mazza, Ryan Heller, Ron Lipton, Gabriele Giacomini, Doug Berry, Jennifer Ott, Valentina Maria Martina Cairo

2.1 Advanced LGAD designs

LGADs, AC-LGADs, Trench-isolated LGADs, Buried Gain LGADs, Deep Junction LGADs, 3D

The most prominent class of 4D sensors proposed for future trackers are based on an evolution from LGAD sensors developed for the HL-LHC. LGADs are thin silicon sensors with modest intrinsic gain, and achieve 30 ps or better time resolution in mm scale pads. Standard LGADs, however, rely on Junction Termination Extensions to interrupt the gain layer between channels, which introduce inactive regions. As a result, LGADs cannot be simply miniaturized to a pitch appropriate for tracking.

Several sensor concepts have been proposed and demonstrated to make LGAD sensors suitable for tracking. Many of these fall in the category of AC-LGADs, which feature continuous gain layer, a resistive n+ surface layer, and AC-coupled readout electrodes. Because the gain layer is uninterrupted, AC-LGADs achieve a fill factor of 100%, and electrodes can be designed with smaller pitch and size than standard LGADs. A key feature of AC-LGADs is the signal sharing between electrodes, which can be used to obtain position measurements with resolution much smaller than (bin size)/$\sqrt{12}$. One major advantage of AC-LGADs is that they can obtain the spatial resolution necessary for future colliders with a coarser pitch and hence a reduced number of readout channels.

Recent test beam measurements have demonstrated that AC-LGADs can achieve simultaneous 30 ps and 5 µm resolution with strips of pitch 100-200 µm [22]. This spatial resolution represents a factor of 5-10 improvement beyond what would be obtained in binary readout, thanks to the sharing of signals between adjacent channels. Other studies have demonstrated similar performance [23] [24].

2.1.1 AC-coupled LGADs

Ryan: Move some of description from general section here, add some test beam results.

Simone: add some UCSC laser results and simulations, non conventional geometry

AC-LGADs have several parameters that can be tuned to optimize the sensor response to the specific application. The geometry of the electrodes in terms of pitch and pad dimension is the most important one, however also the N+ sheet resistivity and the dielectric thickness between N+ and electrodes influence the charge sharing mechanism. All of the AC-LGAD parameters affect the way the charge is shared, therefore it is necessary to balance the properties to achieve the best time and spatial resolution in respect of the channel density and occupancy. These parameters need to be studied with simulation softwares, such as TCAD Silvaco or Sentaurus, to have a good representation of the observed sensor performance. Simulations with TCAD software are important to compare with existing prototype data and to help in optimizing the design.

The top metal of the electrodes in AC-LGADs sits on the oxide layer with no underlying structure. Thanks to the simple layout it is possible to arrange the metal of the electrodes in any shape and size, allowing to optimize the geometry to tune the charge sharing to the specific application. For example circles and crosses instead of metal square could simplify and enhance the reconstruction process. Furthermore electrodes can be shaped to have different charge sharing in the X and Y direction (e.g. micro-strips) to optimize the channel density to the sensor resolution in both directions. A proof of principle of metal electrodes modification process, executed at BNL, was made [25]. The procedure was successful showing that the top geometry of AC-LGADs can be modified, a universal design can be then produced and etched to the specific application.

2.1.2 Buried Layer LGADs

Radiation campaigns showed that LGADs with deep and narrow gain layers are radiation harder than LGADs featuring shallower and broader gain layers. Gain layers are generally obtained by means of ion implantations which can implant boron at a maximum depth of about 2 μm using very high and not easily available implantation energies. Furthermore, deeper implants are generally broader than shallower implants. A way to circumvent the problem, at the expense of a complication in the process, is to implant the boron layer at low energy and then to bury it under a few microns of epitaxial layer, obtaining in this way a deep and narrow gain layer (if high thermal cycles are avoided in the subsequent process. The method can be applied to either standard DC-coupled LGADs or AC-LGADs. A first fabrication has been completed but suffered from a high leakage current due to a poor epitaxial deposition. Another fabrication is on-going.

2.1.3 Trench-insulated LGADs

A way to avoid AC-LGADs and still have a high fill-factor in fine-pitch devices is to use narrow trenches to separate the pixels (or strips). The deployment of such trenches all around the electrodes allows to get rid of the JTE, to bring the gain layer closer to the edge of the n-plus implants, and to bring the pixels close together. Dead areas of a few microns have been demonstrated in FBK productions.

2.1.4 Double Sided LGADs for 5D Tracking

The Double Sided LGAD (DS-LGAD) adds a readout layer to the p-side of the LGAD structure. This allows for double-sided readout with the p side reading out the slower-drifting holes. For a device with the bulk thickness large compared to the pixel pitch the p-side readout can function as a mini time projection chamber with the drift time providing information on the depth of origin of the charge cloud. The signal p-side collects two components, holes from the primary ionization followed by the larger number of holes generated at the gain layer. This provides a unique signature of the pattern of charge deposit within the device (figure AAAA). The fast rise signal can be read by a large area cathode, limiting the number of complex, power hungry fast amplifiers and digitizers. The p-side provides a large, slower signals that can be read out with electronics with lower complexity and power consumption.

The characteristics of the thick ($> 5 \times pitch$) DS-LGAD are sensitive to the interplay between the device thickness, gain layer location and doping, and the applied voltage. In a buried layer device the depth and doping of the gain layer sets the operating point and the drift field. These can be tuned to achieve the required characteristics. Diffusion width and time of arrival of the holes from gain layer amplification can then be used to provide excellent position and good track angle resolution. Operation will be a compromise as these thicker devices will have worse time resolution than thin LGADs and may be more sensitive to radiation effects on doping levels.

2.1.5 Deep-Junction LGADs

The "Deep-Junction LGAD" (DJ-LGAD) [26] is a new approach to the application of controlled impact-ionization gain within a silicon diode sensor. The term "deep-junction" arises from the use of a p-n semiconductor junction buried several microns below the surface of the device. The buried junction is formed by abutting thin, highly-doped p+ and n+ layers, with the doping density chosen to create electric fields large enough to generate impact ionization gain in the narrow buried junction region. Additionally, the doping densities chosen for the p+ and n+ layers are balanced so that when the sensor is fully depleted, the electric field outside of the junction region, while large enough to saturate the carrier drift velocity, is significantly less than that require to create impact ionization gain. This preserves the electrostatic stability at the segmented surface of the detector, thus in principle permitting the production of DC-coupled LGADs with arbitrarily fine granularity. No JTE structure is required for a DJ-LGAD array, as the buried gain layer ensures a uniform gain performance across channels. The DJ-LGAD approach is seen to hold significant promise towards the development of a highly-pixellated DC-coupled silicon diode sensor with substantial internal gain and precise temporal resolution.

2.1.6 Thin LGADs

Thin sensors can be a useful technology to apply in very high radiation environment [27, 28]. In the late years a saturation of the charge trapping effect in silicon was observed [29]. However at a fluence of $10^{17} - 10^{18}$ a standard 300 um silicon detector would still need several thousand volts to deplete. For a thin sensor instead the full depletion at very high fluence can happen at much lower voltages: 500 V of full depletion for a 50 um sensor at 10^{17}. The collected charge for thin sensors, however, would be too small to be efficiently detected by readout electronics. Thin LGADs can be used thanks to the intrinsic charge multiplication, it was shown that sufficient gain is observed until a few 10^{15} for time resolution measurements purposes but less gain is necessary for hit detection only. Furthermore at high fluences gain in the bulk "p" region of the sensor can be activated by increasing the bias voltage applied to the sensor. These statements gives an indication of the radiation hardness properties of thin LGADs even at extreme fluences for hit detection. An example of extreme fluence would be a tracking system very close to the interaction point in future hadron colliders.

2.2 3D

Timespot trench 3D sensors for timing

2.3 MAPS

Fine spatial resolution and course time resolution: CMOS MAPS. Coordinate with CMOS paper

Valentina: for Malta, there is public material here we can use as a reference (including a section on timing) https://twiki.cern.ch/twiki/bin/viewauth/Atlas/MaltaApprovedPlots

and also this CERN EP RD seminar: https://indico.cern.ch/event/1074066/2-measurement-results-from-fas

2.4 Comparison of sensor technologies

Tradeoffs for different sensors: high occupancy? material budget? rad hardness?

2.5 Induced Current Detectors

An induced current detector uses the same sensor as a traditional silicon detector but utilizes small pixel pitch and 3D integration (3DIC) techniques to create a low-capacitance pixel unit cell and readout chain. This not only limits the amount of noise in the system but also enables the detection of the induced current as described by the Schokley-Ramo theorem [30, 31]. The Schokley-Ramo current is the current induced at the readout electrode from mobile charge carriers within the sensor. It has a very fast rising edge ($\sim$ 15 ps) [32] and can be used to precisely timestamp track hits. The Schokley-Ramo current is dependent on the weighting field within the sensor and the depth of charge deposition. As a direct result, it has a complicated bi-polar signal shape that integrates to zero over the course of several nanoseconds. This signal combined with the drift current creates a pulse shape that is dependent on the charged particle's angle of incidence.

A detector that is sensitive to the effects of the Schokley-Ramo current has two critical features: precise ($\sim$ 15 ps) time resolution and angle of incidence information [33]. The precise time resolution is useful in many different collider experiments and can be used for either vertexing or particle identification via a time-of-flight (TOF) measurement. The angular information is a more novel feature but still useful feature. First it can be used to quickly identify particles with large transverse momentum (p_T) for an L1 trigger, as high-p_T particles have high angles of incidence. Second it can be used to greatly increase the speed of track reconstruction because the angular information greatly reduces the number of pixel hits that must be considered when track seeds are generated. These capabilities make it a very attractive detector technology for future collider experiments and requires the continued investment in advanced ASIC design and 3DIC techniques.

3 Electronics

While readout prototypes for the timing detectors at the HL-LHC upgrades have demonstrated performance in line with requirements, applying similar techniques in trackers presents several challenges. High granularity requirement of future trackers will require readout ASICs with smaller pixel sizes compared to present generation, maintaining power consumption levels similar to present designs without timing extraction. Accommodating the additional required electronics for timing extraction, i.e. Time to Digital Converters (TDCs) [34] and memories together with the typical pixel circuitry of present trackers, in pixels at pitches on the order of tens of microns will require the adoption of deeper low power and fast technology nodes beyond 65nm. The entire pixel electronics will need to be designed with low power techniques and with novel timing extraction architecture. In addition, the high luminosity of future hadron colliders will require trackers capable to survive in extreme radiation environments (accumulating a dose of up to 30 GRad and 10^{18} neutrons/cm^2)

Because of these aspects, state-of-the-art low power CMOS and Bi-CMOS technology targeted for the mmW communication industry are of particular interest. These includes FDSOI technologies which could potentially open a path to monolithic readouts at very fine pitch. These technologies are also of interest in other HEP applications for their demonstrated performance at deep cryogenic temperatures.

This might be suitable here

It is important to stress that the read-out philosophy of standard PIN silicon sensors and UFSD is different. In PIN sensors, the maximum current happens just after the passage of the particle while in UFSD the current increases for the duration of the electron drift time, then there is a plateau, and finally decreases. This peculiar signal shape limits the useful bandwidth of the amplifier. The amplifier bandwidth affects both noise and slope and, ideally, the higher BW the lower the jitter. However, the intrinsic time response of UFSD sensors sets the upper limit to the maximum reachable slope that the analog output can exhibit. As a consequence, the bandwidth should be chosen to be the minimum value that retains the intrinsic sensor speed while keeping the noise low. The bandwidth defines the signal shaping of the front-end and its optimum value for timing is obtained when the amplifier shaping time equals the sensor peaking time.

Useful text to incorporate?

Advances in detector technology and the direction of HEP experiments and applications require the development of new specialized readout electronics. Experimental demands include some combination of high rep rates (order of ns dead time), below 10 ps time of arrival (TOA) resolution, low power (between 0.1 mW and 1 mW per channel), and high dynamic range (for some specific application up to a few 1000s).

3.1 Current timing chips

brief discussion of ALTIROC, ETROC (Ryan), capabilities and limitations

3.2 FAST family of ASICs

Keep or remove?

In the past several years the FAST effort had the goal of designing an ASICs tailored to the read-out of Ultra-Fast Silicon Detector. TOFFEE [35], the first prototype, has been produced in 2016, FAST1 in 2018 [36], and FAST2 [37] in 2020. This family of ASICs aims to provide a 25 ps time resolution with rates up to 200 MHz and has been designed in a 110 nm CMOS commercial technology node. In every iteration of the production the architecture has been improved to optimize the chip performance. Starting from FAST2 a analog-only version of the chip have been produced. The next foreseen production is FAST3, which is based on the studies performed on FAST2 with expand linearity of the output dynamic range. In parallel to FAST3, the ASIC UFSD_ALCOR has been designed. It includes the optimized front-end stage used in FAST3_Analog, a discriminator stage, time to digital converter (TDC), and a digital control unit. Each channel can measure the Time of Arrivals (ToA) and Time of Threshold (ToT) of a pulse signal with a least significant bit of 25 ps. FAST3 and UFSD_ALCOR are almost completed and will be manufactured in the first half of 2022.

3.3 SiGe amplifiers

A possible path to achieve O(10 ps) time resolution is an integrated chip using Silicon Germanium (SiGe) technology. Using DoE SBIR funding, Anadyne, Inc. in collaboration with University of California Santa Cruz has developed a prototype SiGe front end readout chip optimized for low power and timing resolution, with 0.5 mW per channel (front end and discriminator) while retaining 10 ps of timing resolution for 5 fC of injected charge. In the process some insight was developed into the challenges and potential performance of SiGe front end ASICs for future R&D effort. The developed single pre-amplifier stage and what is effectively a Time Over Threshold (TOT) discriminator topology is suitable for low repetition rate and quiescent power and sub 10 ps timing resolution applications. Some practical considerations for selecting a process for future R&D include the size and power efficiency of the CMOS transistors for the back-end electronics and diminishing performance gains of higher speed SiGe transistors. The currently available SiGe processes offer 130 nm CMOS at a minimum. Transistors faster than 25 GHz have little signal to noise or power improvements to offer when designing readout systems for signals in the 1-2 GHz regime ultra-fast silicon detectors operate in. Moving to faster and smaller SiGe transistors may only introduce unnecessary design challenges such as poor transistor matching, low breakdown voltages, higher Vbe, etc. The current prototype is designed in a 10 GHz process. Significant R&D efforts would be required to determine how much timing resolution, power consumption and dead time performance could be improved by moving to a specific 20-30 GHz process.

3.4 Full digitization chip

University of California Santa Cruz is currently working with Nalu Scientific to design and fabricate a high channel density and scalable radiation-hard waveform digitization ASIC with embedded interface to advanced high-speed sensor arrays such as e.g. AC-LGADs. The chip is being fabricated with TSMC's 65nm technology using design principles consistent with radiation hardening and targets the following features: picosecond-level timing resolution; 10 Gs/s waveform digitization rate to allow pulse shape discrimination; moderate data buffering (256 samples/chnl); autonomous chip triggering, readout control, calibration and storage virtualization; on-chip feature extraction and multi-channel data fusion; reduced cost and increased reliability due to embedded controller (reduction of external logic). Existing readout approaches, such as AltiROC and the newer TimeSPOT1 , promise good-to-excellent timing resolution and channel density, and use a TDC-based measurement for signal arrival times and time-over-threshold (ToT) for an indirect estimate of integrated charge. However, these readout strategies will likely adversely impact the ability to provide sub-pixel spatial resolution and are typically have difficulty compensating for environmental factors such as pile-up, sensor aging, and radiation; timing precision can also be adversely impacted by factors such as timewalk, baseline wander and waveform shape variations. Here, instead, full waveform digitization will be used, which is expected to be more robust against a variety of adverse factors which can affect timing and spatial precision. The initial iteration of the readout chip (v1) was recently (Jan 2022) fabricated for 50 um AC-LGADs. Later versions of the chip will be designed for 20 um pixel arrays and also test the minimum pitch feasible for a single-channel readout using a one-to-one pixel-input channel mapping. The final version of the chip will feature a transimpedance amplifier input stage able to be fine-tuned (or tunable) in order to accommodate high-density sensor arrays using technologies other than AC-LGADs.

3.5 28nm CMOS technology TDC design

CERN's EP RD WP5: CMOS Technologies [38] survey has promoted the selection of 28nm CMOS node as the next step in microelectronics scaling for HEP designs. The choice was based on radiation-hardness studies [39], frequency and cost of MPW runs and strong presence on the market. Furthermore, the 28nm technology is at least twice as fast and allows circuit densities around 4-5 times higher than the previously employed 65nm node, making it a good candidate for design of high granularity 4D trackers. One of the critical circuit blocks necessary to enable 4D operation in trackers are low-power and compact Time-to-Digital Converters (TDC) capable of high time-measurement precision. SLAC has stated the design of TDCs in 28nm technology node with target time resolutions of 10-50ps. The plan is to submit the first prototype for fabrication at the end of this year.

3.6 Chips comparison

Write something about the different approach performances

4 Layout

A major next step towards 4D tracking at future hadron colliders is the study of how to best combine timing with spatial information. The fine spatial tracking resolution demand towards small pixel with low material budget and low power may make it impractical to instrument finest timing capabilities on all layers. On the other hand, 4D devices with still fine spatial granularity and integrated some coarse timing capabilities can potentially allow a versatile mixture of layers with different balance of spatial and timing resolution to serve an optimal overall 4D tracking for the wide range of applications. The addition of timing information to every pixel hit might not be the approach that leads to the best performance. Alternative approaches such as alternating spatial with timing layers, or 4D with 3D layers could help improve the overall physics performance.

Another aspect of detector layout is related to the physics drivers motivating its development. For example, improved and fast charged track reconstruction, heavy flavor (b/c) tagging, and particle-flow reconstruction under very high pileup density will require 4D information in the inner layers, whereas LLP and time-of-flight particle ID capabilities, including the possibility of strange-tagging [40–43], will benefit from 4D information in the outer layers. LLP applications would demand continuous timing coverage and could benefit from modest timing resolution in more layers without stretching timing dynamic range. Future e^+e^- collider vertex detector backgrounds are predominantly back-scattered bremsstrahlung particles from downstream magnets and collimators with $\sim$ns range delays. 4D tracking devices with fine spatial resolution and modest timing resolution in other layers could significantly enhance the overall performance.

Other key considerations are tracking material and pseudorapidity coverage. The additional material required to go from 3D to 4D tracking will have an impact on the track-time association efficiency and mis-association rate. Whereas a lower track-time efficiency will simply reduce the potential gains from timing information, the wrong assignment of times to tracks is particularly problematic as in this case the 4D reconstruction will perform worse than 3D. The impact of showering of particles within the tracking material might be partially mitigated with the use of advanced algorithms based on graph neural networks or other deep learning techniques but this will require a long term study. In the case of future lepton colliders, material in the tracking detector has to be minimized to not degrade p_t and impact parameter resolution, posing additional constrains on the incorporation timing information [**?**]

5 Key areas for future R&D

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Valentina: Maybe something of what is written above for ATLAS could go here? Or we can highlight there already that this is a key area for future R&D, making a sort of recommendation to the particle physics community.

6 Summary

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