Fermi National Accelerator Laboratory

Fermilab

PIP-II LLRF Station

Technical Requirements Specification

Document number: ED0013969

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Document Approval

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Stakeholder Reviews performed off-line using TRS Metadata sheets	Dataset in TC

Revision History

Revision	Date of Release	Description of Change
01-	10/21/2021	Initial Release for Review

Table of Contents

1. SCOPE

The LLRF system is organized into groups of up to four cavities controlled by one rack of electronics. The group of four cavities allows for an economy of scale in the hardware design while keeping cable runs as short as possible. Three or four such racks for the LLRF hardware along with two racks for the RFPI hardware, would constitute a complete 6 rack RF station that can control upto 12 or 16 cavities of multiple cryomodules.

The scope of this document is to cover the components of the modular 4 cavity LLRF rack, which is the building block for all the RF stations:

1. LLRF Controller Chassis – Qty 2,
2. Resonance Control Chassis – Qty 1,
3. 8-ch Downconverter Chassis – Qty 2
4. 4-ch Upconverter Chassis – Qty 1
5. Local Oscillator, Clock and Reference Distribution chassis – Qty 3
6. Power supply (up/down converters, Resonance control chassis) Qty 3
7. Field Control Firmware/Software
8. Temperature Control Chassis – Qty 2

The Resonance Control Chassis and the Field Control Firmware/Software will not be covered in this document as they are described in separate requirements documents.

2. ACRONYMS, TERMS, AND DEFINITIONS

SRF	Superconducting radiofrequency
LLRF	Low level RF
CW	Continuous-wave
MPS	Machine protection system
SSA	Solid State Amplifier
Output Noise Floor	Noise power level at the IF outputs in dBm/sqrt(Hz).
Linearity	Distortion of the downconverted RF signal at the IF output in percent (Vif_out/(Vrf_in - nom. Conv. Loss)).
Channel Isolation	Amount of downconverted RF signal from one channel to any other IF channel output in dB.

3. REFERENCED DOCUMENTS

[1]	ED0011278	Technical Requirements Specification -FPGA Board
[2]	ED0011279	Technical Requirements Specification – ADC DAC Mezzanine Board
[3]	ED0005793	Technical Requirements Specification – Controller Chassis
[4]	ED0013968	Technical Requirements Specification – Resonance Control Chassis

[5]	ED0005166	Technical Requirements Specification – 8-Channel Receiver
[6]	ED0005163	Technical Requirements Specification – 4-Channel Upconverter

4. ROLES AND RESPONSIBILITIES

4.1. Author(s)

Responsible for TRS preparation, including layout, proper format, requirement identification, requirement verification expectations, requirement traceability, and additional descriptive detail, as appropriate. The author is expected to engage subject matter experts as needed to ensure technical content is appropriately assessed and captured. The author is also expected to identify all applicable stakeholders to their noted requirement(s). In some cases, the author can also have the role of the document Owner.

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4.3. Reviewer

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4.4. Approver

The L2 Manager will evaluate the basis for requirements definition, ensure that requirements are properly articulated, and ensure that they align with higher level requirements specifications, as applicable. The L2M will ensure that CAMs, associated engineering staff, and other Systems Managers are properly engaged and notified of the document's technical implications. Only the System Manager responsible for the work product addressed in the specification is expected to provide approval. The Approver is an "Approver" in the Teamcenter workflow release.

4.5. Stakeholder

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Person(s) or Areas Responsible	Define Responsibility
Elvin Harms	PIP-II LLRF Project Manager
Curt Hovater	PIP -II LLRF Project Technical Coordination
Larry Doolittle	PIP -II LLRF Technical Lead
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Ahmed Syed	PIP-II LLRF Master Oscillator, LO Distribution
Ed Cullerton	PIP-II LLRF Down Converter, Up-Converter

5. REQUIREMENTS

5.1. System Definition

The components of the 4 cavity LLRF rack are shown in Figure 1.
Three configurations of the modular LLRF racks define all the RF stations for the full PIP-II Linac. The MEBT section with the RFQ, four buncher cavities and HWR,the first superconducting cryomodule in the Linac are all the RF components within the first frequency group of 162.5 MHz. They can be accommodated within the first RF station as shown in Figure. 2. The two 325 MHz SSR1 cryomodules with 8 cavities each are controlled by RF Station 2 as shown in Figure 3. The third configuration of RF stations applies to the remaining cryomodules in the Linac and is shown in Figure 4. Since the SSR2, LB650 and HB650 cryomodules have 5, 4 and 6 cavities each, an RF station could control cavities from multiple cryomodules as long as they are within the same frequency group.

PIP-II LLRF 4-Cavity Control Rack Station
Ed Cullerton
6/22/2018

Figure 1

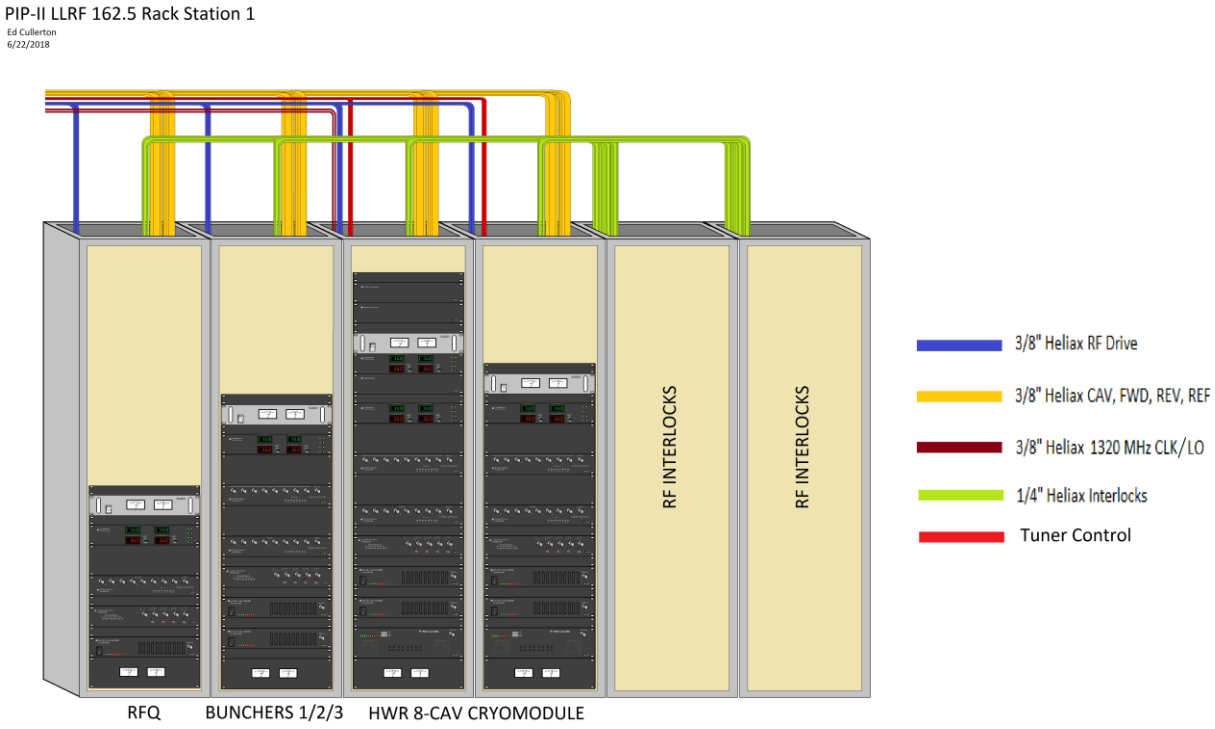

Figure 2

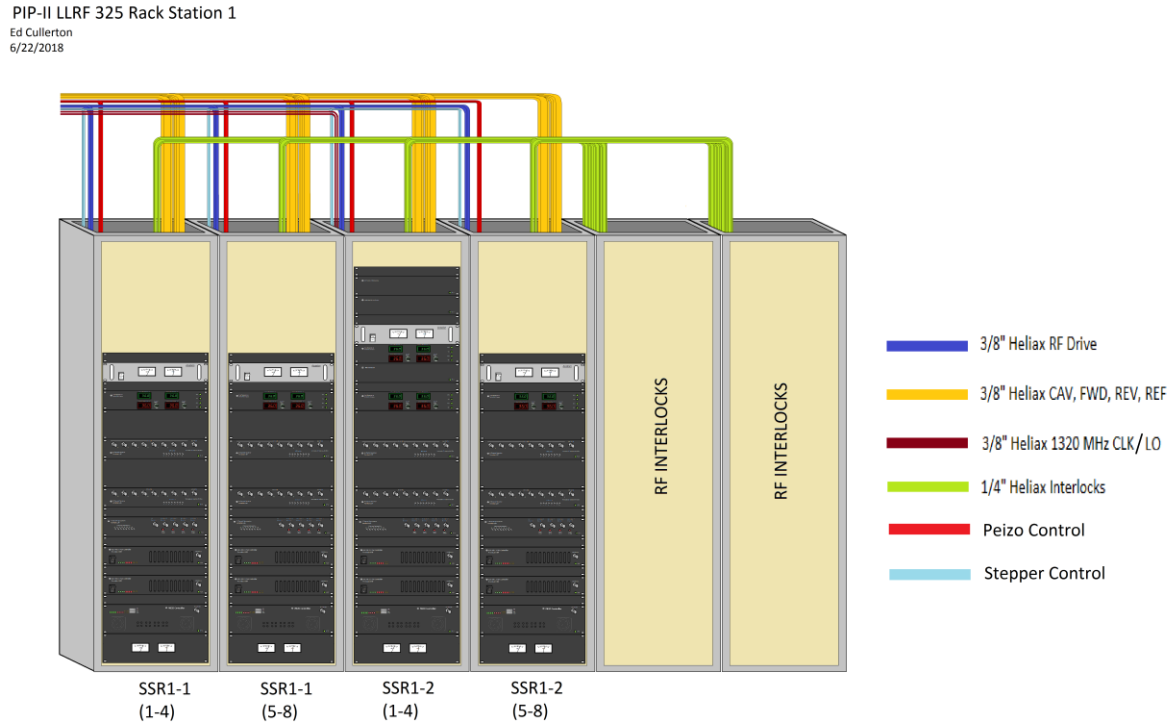

Figure 3

Figure 4

5.1.1. Background

The block diagram as shown in Figure 5 below defines the PIP-II LLRF architecture.
The rack hardware includes the LO, FPGA clock, and phase reference distribution chassis' which are used to distribute RF signals throughout a LLRF Rack Station. A LLRF Rack Station consists of multiple four-cavity control racks and typically controls 12 to 16 cavities. A description of each module is provided in the following sections.

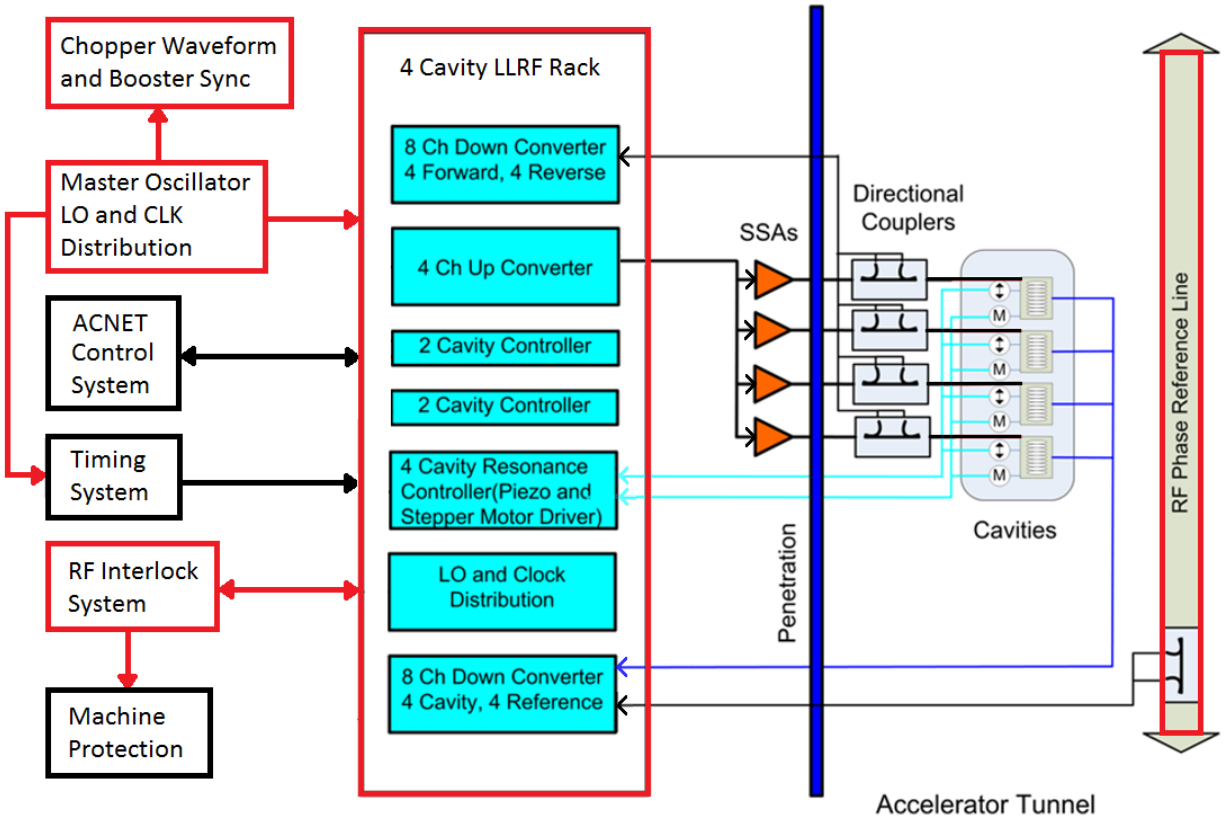

Figure 5

5.1.2. High Level Operations Concepts/Scenarios

5.1.2.1. Downconverter Chassis (DC)

The 8-channel downconverter is used in the LLRF system to convert RF signals to IF signals used in digital signal processing. The downconverter will have as inputs of cavity probe RF signals, forward power to the cavity RF signals, reflected power from the cavity RF signals, and a phase reference signal. These signals will be downconverted to 20 MHz IF signals and sent to the LLRF controller. The channel to channel isolation shall be better than 80 dB. The channel to channel isolation will be measured by injecting a signal into a RF input and measuring the signal output at all other IF outputs. The 20 MHz IF output shall have a non-linearity less than 1% up to +6 dBm. There shall be an IF monitor of each IF output to the front panel of the chassis.

A block diagram of the downconverter is shown in Figure 6. The selection of components was based on the qualities listed in Table 1.

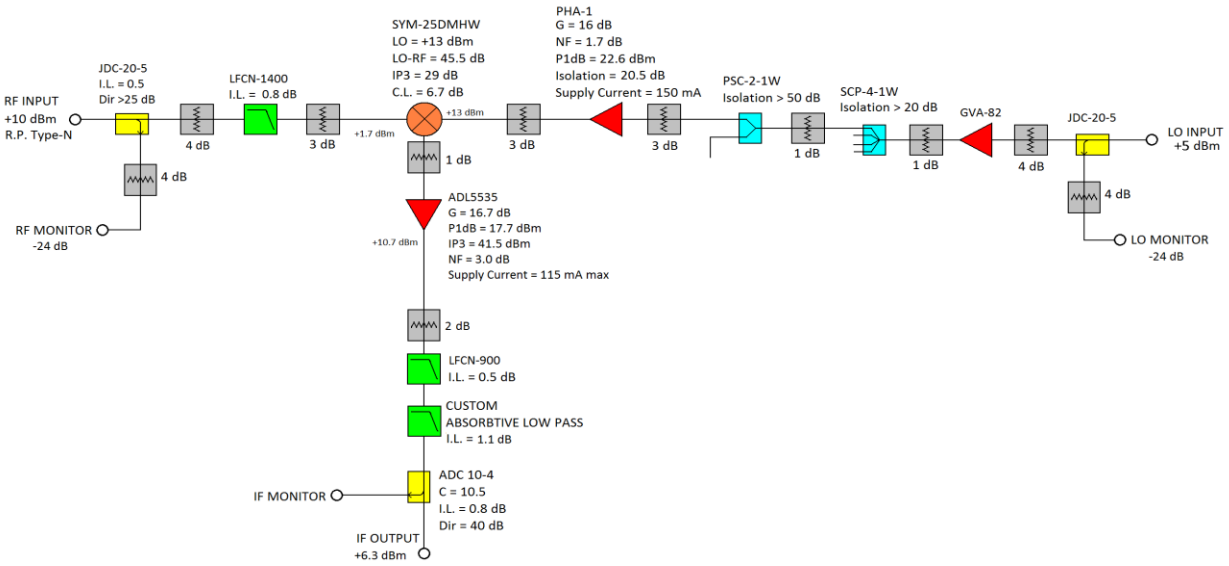

Figure 6 Block diagram of the downconverter board.

Table 1 Component qualities of the board.

Component	Manufacturer	Model	Desired Qualities
Mixer	Mini-Circuits	SYM-25DMHW	high IP3 / high RF-LO isolation.
RF input monitor coupler	Mini-Circuits	JDC-20-5	high directivity / isolation
IF amplifier	Analog Devices	ADL5535	high IP3 / low gain / low noise figure
LO amplifier	Mini-circuits	PHA-1	high IP3 / moderate gain / low noise fig
LO distribution splitter	Mini-circuits	PSC-2-1W	high isolation
LO distribution splitter	Mini-circuits	SCP-4-1W	high isolation
IF output monitor coupler	Mini-circuits	ADC 10-4	High directivity / isolation @ 20 MHz

Downconverter Technical Requirements

Table 2 162.5 MHz Down-Converter Requirements

Parameter	Value
RF signal input frequency (nom.)	162.5MHz
IF output frequency (nom.)	20 MHz
LO input frequency (nom.)	182.5 MHz
LO input signal level (nom.)	+5dBm
Number of RF inputs and IF outputs	8
Full scale RF Input signal level	+ 10 dBm

Full scale IF Output signal level	+ 5 dBm (+/- 1dB)
Output Linearity	+/- 1%
Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

Table 3 325 MHz Down-Converter Requirements

Parameter	**Value**
RF signal input frequency (nom.)	325MHz
IF output frequency (nom.)	20 MHz
LO input frequency (nom.)	345 MHz
LO input signal level (nom.)	+5dBm
Number of RF inputs and IF outputs	8
Full scale RF Input signal level	+ 10 dBm
Full scale IF Output signal level	+ 5 dBm (+/- 1dB)
Output Linearity	+/- 1%
Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

Table 4 650MHz Down-Converter Requirements

Parameter	**Value**
RF signal input frequency (nom.)	650MHz
IF output frequency (nom.)	20 MHz
LO input frequency (nom.)	670 MHz
LO input signal level (nom.)	+5dBm
Number of RF inputs and IF outputs	8
Full scale RF Input signal level	+ 10 dBm
Full scale IF Output signal level	+ 5 dBm (+/- 1dB)
Output Linearity	+/- 1%

Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

5.1.2.2. Upconverter Chassis (UC)

The 8-channel downconverter is used in the LLRF system to convert RF signals to IF signals used in digital signal processing. The downconverter will have as inputs of cavity probe RF signals, forward power to the cavity RF signals, reflected power from the cavity RF signals, and a phase reference signal. These signals will be downconverted to 20 MHz IF signals and sent to the LLRF controller. The channel to channel isolation shall be better than 80 dB. The channel to channel isolation will be measured by injecting a signal into a RF input and measuring the signal output at all other IF outputs. The 20 MHz IF output shall have a non-linearity less than 1% up to +6 dBm. There shall be an IF monitor of each IF output to the front panel of the chassis.

A block diagram of the upconverter board is shown in figure 5. The selection of critical components was based on the component qualities listed in Table 5.

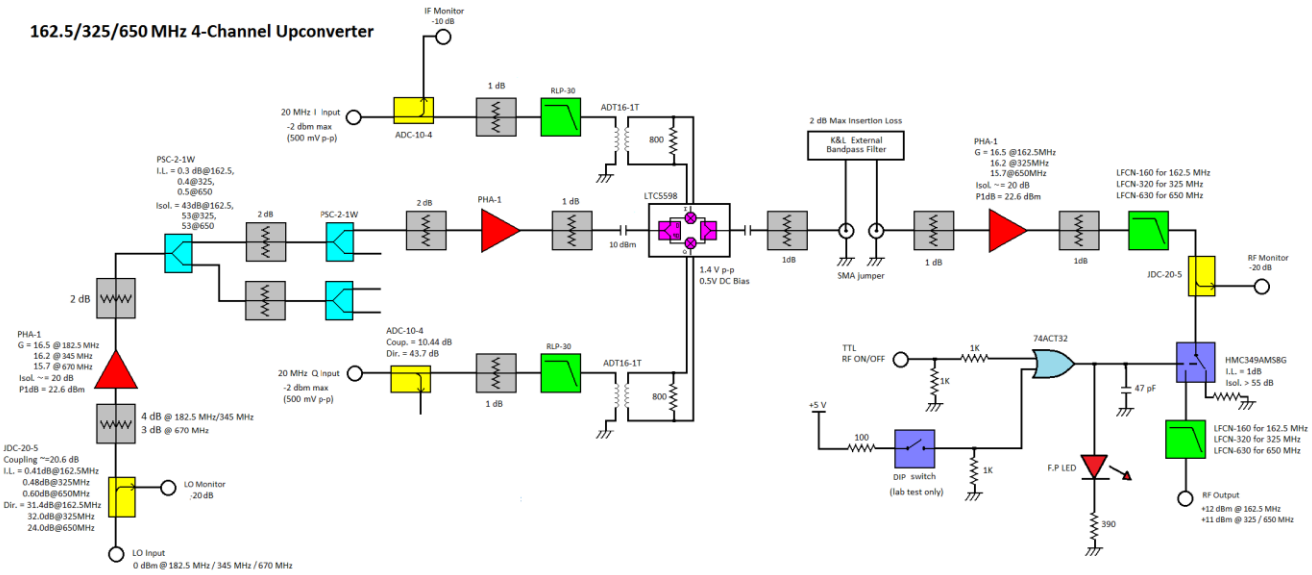

Figure 7 Block diagram of the upconverter board.

Upconverter Technical Requirements Summary Tables

Table 5 162.5 MHz Up-Converter Requirements

Parameter	Value
IF signal input frequency (nom.)	20 MHz
RF output frequency (nom.)	162.5 MHz
LO input frequency (nom.)	182.5 MHz

LO input signal level (nom.)	0 dBm
Number of RF outputs	4
Full Scale IF I/Q input signal level (nom.)	-2 dBm each
Full scale RF Output signal level (min.)	+ 10 dBm (+/- 1dB)
Output Linearity	+/- 1%
Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

Table 6 325MHz Up-Converter Requirements

Parameter	**Value**
IF signal input frequency (nom.)	20 MHz
RF output frequency (nom.)	325 MHz
LO input frequency (nom.)	345 MHz
LO input signal level (nom.)	0 dBm
Number of RF outputs	4
Full Scale IF I/Q input signal level (nom.)	-2 dBm each
Full scale RF Output signal level (min.)	+ 10 dBm (+/- 1dB)
Output Linearity	+/- 1%
Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

Table 7 650 MHz Up-Converter Requirements

Parameter	**Value**
IF signal input frequency (nom.)	20 MHz
RF output frequency (nom.)	650 MHz
LO input frequency (nom.)	670 MHz
LO input signal level (nom.)	0 dBm
Number of RF outputs	4

Full Scale IF I/Q input signal level (nom.)	-2 dBm each
Full scale RF Output signal level (min.)	+ 10 dBm (+/- 1dB)
Output Linearity	+/- 1%
Channel-to-Channel Crosstalk	< -80dB
Residual Phase Noise (1Hz-100kHz BW)	< 2 mdeg rms
Residual Amp. Noise (1Hz-100kHz BW)	< 0.02% rms

5.1.2.3. LLRF Controller Chassis

The Controller Chassis is the central component of the Station control rack as it is responsible for supervisory control, cavity RF field control, frequency error signal generation for the Resonance Controller Chassis, the main DAQ process and the interface to the control system . Each chassis controls two cavities. This document covers the technical requirements of the Controller Chassis.
The RF signal processing is all done at an intermediate frequency of 20 MHz with inputs from the phase reference line, cavity probe, forward and reverse power, all downconverted from the various RF frequencies by the downconverter chassis. Internally the IF signals are digitized by 16 bit 125 MHz ADCs connected to an FPGA where the digitized IF signals are downconverted to baseband A 20 MHz IF QAM cavity drive signal is returned to the RF frequency by the Upconverter chassis. In a Station Rack two Controller Chassis are combined with two eight channel Downconverter Chassis, one four channel Upconverter Chassis, one four cavity Resonance Control Chassis and power supplies.

Chassis

The chassis shall be 3 RU, designed for mounting in a 19” rack based on EIA-310. Example rack dimensions can be seen in the figure below.

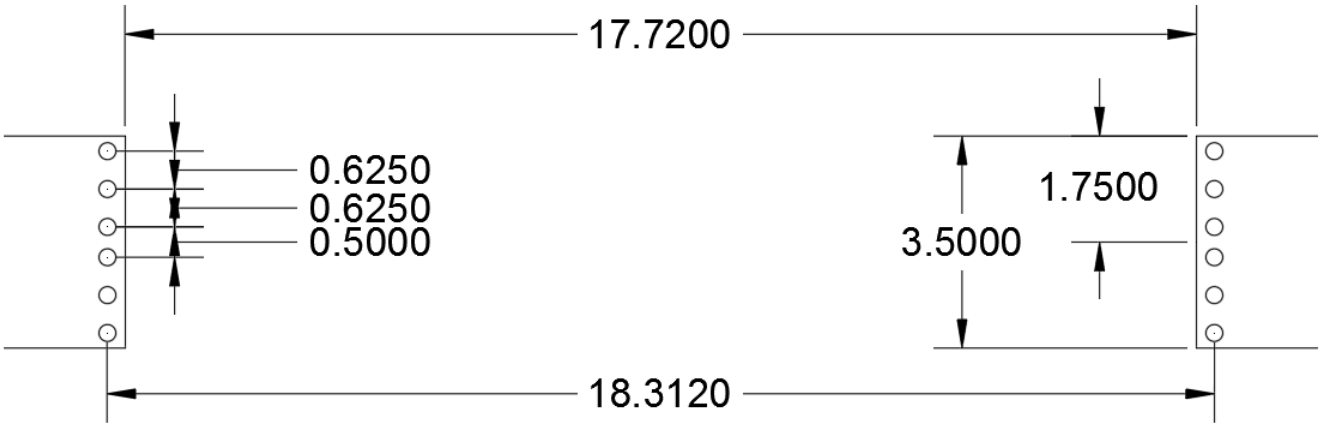

Figure 9 Example 2RU EIA-310 19” rack dimensions

The chassis shall fit entirely within a 3RU vertical envelope.
The chassis shall not mechanically interfere with adjacent equipment.
The chassis shall be able to be installed in a rack with adjacent spaces filled without the use of additional tools or a specialized procedure.
The chassis shall have a depth no greater than 14”.

The chassis shall be able to be easily disassembled.
The top of the chassis shall be able to be removed for easy access inside for debugging.
The chassis shall be sturdy enough to handle transport shocks and not require special handling when being moved.
Status LEDs shall be visible from the front of the chassis
All signal inputs and outputs and controller digital and analog I/O shall be on the rear of the chassis

External Connections

Table 8

Name	Qty	Description	Connector	
ADC Inputs	8	RF inputs to digitizer board	SMA female	
DAC Outputs	4	RF outputs from digitizer board	SMA female	
Clock Input	1	LO input to digitizer board	SMA female	
Triggers	6	Triggers to controller board	SMA female	
Clock Monitor	1	Front-panel clock monitor	SMA female	
Front-panel Trigger	1	Front-panel trigger	SMA female	
High-speed Links	3	QSFP connections for digital, high-speed communication links	QSFP	
Copper Ethernet	1	Ethernet connection to controls networks	8P8C modular jack	
GPIO	4	GPIO from controller board and digitizer board	SMA female	
Power	1	Chassis power	Souria UT00104PH	

5.2. Requirements

5.2.1. Performance

As outlined in the Physics requirement “Linac Requirements LCLS-II-2.4-PR-0041-R2” LLRF system is being designed to the following RF parameters.

Table 9 Physics Requirements

Parameter	Symbol		
RF frequencies	*fRF*	162.5,325,650	MHz
Average RF gradient HWR cavities	*Eacc*	9.7	MV/m
Average RF gradient SSR1 cavities	*Eacc*	10.0	MV/m
Average RF gradient SSR2 cavities	*Eacc*	11.4	MV/m
Peak current in linac	*Iav*	2.0	mA
Mean cavity quality factor (loaded)	*QL*	4x107	
Amplitude Stability - Cavity		0.065	%rms
Phase Stability - Cavity		0.065	deg
Energy Stability - Linac		0.01	%

5.2.1.1. Downconverter

Table 10 Downconverter Requirements

Requirement #	Requirement Statement
T- ED0013969-A001	The RF input frequencies shall be 162.5 MHz, 325 MHz and 650 MHz respectively
T- ED0013969-A002	The IF output frequency shall be 20 MHz
T- ED0013969-A003	The LO input frequencies shall be 182.5 MHz, 345 MHz and 670 MHz respectively
T- ED0013969-A004	The LO input signal level shall be +5 dBm (+/- 1 dB)
T- ED0013969-A005	There number of RF inputs and IF outputs shall be 8 per downconverter chassis
T- ED0013969-A006	The full scale RF input signal level shall be +10dBm
T- ED0013969-A007	The output linearity shall be better than +/- 1%
T- ED0013969-A008	The channel to channel crosstalk shall be < -80 dB
T- ED0013969-A009	The residual phase noise (1Hz – 100kHz BW) shall be < 2 mdeg rms
T- ED0013969-A010	The residual amplitude noise (1Hz – 100kHz BW) shall be < 0.02 % rms

5.2.1.2. Upconverter

Table 11 Upconverter Requirements

Requirement #	Requirement Statement
T- ED0013969-B001	The RF output frequencies shall be 162.5 MHz, 325 MHz and 650 MHz respectively
T- ED0013969-B002	The IF input frequency shall be 20 MHz
T- ED0013969-B003	The LO input frequencies shall be 182.5 MHz, 345 MHz and 670 MHz respectively
T- ED0013969-B004	The LO input signal level shall be 0 dBm
T- ED0013969-B005	There number of RF outputs shall be 4 per upconverter chassis

T- ED0013969-B006	The full scale RF output signal level shall be +10dBm (+/- 1dB)
T- ED0013969-B007	The full scale IF I/Q input signal level shall be -2dBm each
T- ED0013969-B008	The channel to channel crosstalk shall be < -80 dB
T- ED0013969-B009	The residual phase noise (1Hz – 100kHz BW) shall be < 2 mdeg rms
T- ED0013969-B010	The residual amplitude noise (1Hz – 100kHz BW) shall be < 0.02 % rms
T- ED0013969-B011	The output linearity shall be better than +/- 1%

5.2.1.3. LLRF Controller

Table 12 LLRF Controller Requirements

Requirement #	Requirement Statement
T- ED0013969-C001	The controller board receives a 0 dBm 1320 MHz Local oscillator RF signal and divides this signal down to generate all required clock signals for the ADCs, DACs and FPGA.
T- ED0013969-C002	The controller board shall be FMC specification compliant. If full compliance is not possible, it shall be explicitly mentioned on the board silkscreen.
T- ED0013969-C003	The board shall provide various onboard power supplies which are derived from 12V and 3.3V supplies available via FMC connector.
T- ED0013969-C004	The board shall have some spare analog and digital IOs for in-field expansion.
T- ED0013969-C005	The board shall support field expandable protocols like SPI / I2C / PMOD.
T- ED0013969-C006	The board shall have supervisory electronics for on-board health monitoring.
T- ED0013969-C007	Shall provide 2 channels of DAC and 2 channels of ADC for utility usage if needed.
T- ED0013969-C008	Housekeeping information on temperature and supply voltages shall be available.
T- ED0013969-C009	Board identification shall be available digitally.
T- ED0013969-C010	Monitoring points and indicators are located on the front panel of the chassis.

T- ED0013969-C011	All the monitoring points (for analog/RF signals) shall have 50Ω SMA connectors and are terminated in a 50Ω load when not in use.
T- ED0013969-C012	Power to the FPGA board is supplied through FMC connectors from the carrier board.
T- ED0013969-C013	The PCB layout is done using “best layout practices” to keep crosstalk and coupling to a minimum
T- ED0013969-C014	(8) RF signal inputs are available designed to take in <95 MHz IF, +10 dBm maximum power on SMA headers
T- ED0013969-C015	(4) RF signal outputs are available, designed for a +0dBm maximum output power on SMA
T- ED0013969-C016	A clock input is available, designed to take in a 1320 MHz, +2.5 dBm maximum power on an SMA header.
T- ED0013969-C017	A clock output is available, with a 800 mVp-p signal on an SMA header.
T- ED0013969-C018	Shall have 16 GPIO routed from the controller card to 100 mil headers.
T- ED0013969-C019	The board shall provide eight ADC channels with sixteen-bit resolution.
T- ED0013969-C020	Each ADC channel shall have an analog input bandwidth of 650 MHz. This shall allow the board to be used for other beam line instrumentation as well. The bandwidth of the analog input signal shall be reduced to the Nyquist bandwidth using a suitable low pass filter.
T- ED0013969-C021	Each analog input shall have a range up to +6dBm. Analog inputs shall be capable of handling Full power IF signal (+10 dBm) from the down converter without any permanent damage.
T- ED0013969-C022	The normalized noise power density of ADC channel shall be better than -150 dBFS /Hz.
T- ED0013969-C023	The channel to channel cross talk shall be better than -90 dB at 20 MHz
T- ED0013969-C024	The ADC INL shall be better than ± 6 LSB and the DNL shall be better than ± 1 LSB based on datasheet values.

T- ED0013969-C025	The ADC reference shall have noise figure better than 1 µV integral noise over 0.1 Hz to 10 MHz bandwidth.
T- ED0013969-C026	The power supply noise rejection ratio for Analog section and digital section shall be better than 80 dB. The noise in the ADC power supplies shall be low enough to ensure the required noise floor specification.
T- ED0013969-C027	Each ADC channel shall be capable of operating in excess of 95 MHz sampling speed. The actual sampling speed will be a sub-multiple of 1320 MHz clock.
T- ED0013969-C028	It shall be possible to adjust the relative phase of ADC Data Clock and Frame clock signals using SPI.
T- ED0013969-C029	The ADC data output shall be in multilane LVDS format so as to keep the speed below the FPGA IO speed limit.
T- ED0013969-C030	It shall be possible to generate test patterns on ADC data lines for testing of the downstream hardware.
T- ED0013969-C031	It shall be possible to configure the ADC using SPI running at, speed up to 25 MHz. It shall be possible to read and write the control registers of the ADC.
T- ED0013969-C032	It shall be possible to reset and power down the ADC using external pins. It shall be possible to power down individual ADC channel using SPI.
T- ED0013969-C033	The ADC shall remain in power down mode at turn on. It shall power up only when enabled via external pin.
T- ED0013969-C034	The SPI programming interface shall remain quiet during data acquisitions.
T- ED0013969-C035	The ADC calibration data shall be stored on board using an EEPROM. The ADC ID shall be read and compared with the ID stored in the calibration data.
T- ED0013969-C036	The critical RF lines shall use NP0 capacitors for minimizing microphonics.
T- ED0013969-C037	The Controller board shall provide four channels of DAC having fourteen-bit resolution.

T- ED0013969-C038	Each DAC channel shall support update rates in excess of 190 MSPS. The actual clock speed will be a sub-multiple of 1320 MHz clock.
T- ED0013969-C039	Each analog output shall have a range up to -2 dBm.
T- ED0013969-C040	The DAC INL shall be better than ± 4 LSB and the DNL shall be better than ± 2 LSB as defined in datasheet.
T- ED0013969-C041	The channel to channel cross talk shall be better than -80 dB.
T- ED0013969-C042	The power supply noise rejection ratio for Analog section and digital section shall have more than 80 dB. The noise in the DAC power supplies shall be less than 100 µV in 100 kHz bandwidth.
T- ED0013969-C043	It shall be possible to adjust the relative phase of data clock and main clock with respect to the actual data arrival using SPI.
T- ED0013969-C044	It shall be possible to configure the DAC using SPI interface running at, speed up to 25 MHz. It shall be possible to read and write the control registers of the DAC.
T- ED0013969-C045	It shall be possible to reset and power down the DAC using external pins. It shall be possible to power down individual DAC channel using SPI.
T- ED0013969-C046	The DAC shall remain in power down mode at turn on. It shall power up only when enabled via external pin.
T- ED0013969-C047	The programming interface shall remain quiet during DAC operation.
T- ED0013969-C048	The clock distribution system shall have a RMS jitter of less than 125 fs in a 1 kHz bandwidth.
T- ED0013969-C049	The output clock duty cycle shall be nominal 50% to ensure proper operation of sample and hold stage.
T- ED0013969-C050	It shall provide two differential clocks for ADCs, two differential clocks for DACs and two differential clocks for FPGA board. It shall provide clocks that are a sub-multiple of the input clock.

T- ED0013969-C051	The input clock health shall be monitored and the clock generator outputs shall be enabled only if the input clock amplitude is healthy (-6 dB).
T- ED0013969-C052	The clock division ratio shall be configured using SPI. It shall support clock divider range from 1:8 (odd / even) and 2:64 (even only) on all channels using SPI.
T- ED0013969-C053	It shall support LVDS and LVPECL modes on all outputs. It is preferred if LVCMOS modes is also supported on a few pins. The individual output clock type shall be programmable via SPI.
T- ED0013969-C054	All unused clock lines shall be properly terminated as per the default power-on mode for the particular channel. Any unused clock lines shall be disabled using SPI.
T- ED0013969-C055	It shall be possible to configure the clock generator using SPI running at, speed up to 25 MHz. It shall be possible to read and write the control registers of the clock chip.
T- ED0013969-C056	It shall be possible to reset and power down the clock generator via external pins. It shall be possible to power down individual clock outputs using SPI.
T- ED0013969-C057	The clock driver shall remain in power down mode at turn on. It shall power up only when enabled.
T- ED0013969-C058	The programming interface shall remain quiet during data acquisitions.
T- ED0013969-C059	The chip ID shall be read and compared with the ID stored in the calibration data.
T- ED0013969-C060	The critical RF lines shall use NP0 capacitors for minimizing microphonics.

5.2.2. Physical Characteristics

Table 13 Physical Characteristics Requirements

Requirement #	Requirement Statement

T- ED0013969-D001	The chassis modules shall be designed to be installed in standard 19” wide racks. The chassis shall be 3 RU, designed for mounting in a 19” rack based on EIA-310.
T- ED0013969-D002	The chassis shall have a depth no greater than 14”. The chassis shall be able to be easily disassembled. The top of the chassis shall be able to be removed for easy access inside for debugging.
T- ED0013969-D003	All chassis RF cables shall be selected based on performance characteristics at 1.3 GHz. All station signal runs shall be designed to be as short as reasonably possible.

5.2.2.1. LLRF Rack Specifications

Following are the rack requirements for LLRF near each penetration

- Downconverters Area Temperature Maximum and Tolerance: 35 Degree C Max with stability of +/-2 Degree C
- RF Station/Resonance/Interlocks/ Area Max Temperature with Tolerance: 35 Degree C max +/-5 Degree C (note can have temperature gradient from bottom to top of 10C max)
- Rack heat load from LLRF: Total 250 Watts (PRC area 35 Watts)
- Acoustic Noise: 60 dBA max
- Electrical Service: Two 20A breakers each with power strips
- AC outlet at the bottom of the rack (front and rear) for test equipment
- Fiber Patch Panel Near the top of the rack
- Max cable length for quantity 6, 3/8 inch heliax from penetration opening to inside of LLRF rack is approximately 30 feet. The cables should enter the rack from sides near the base of the rack.

5.2.3. Reliability, Maintainability, and Availability

Table 14 Reliability, Maintainability, and Availability Requirements

Requirement #	Requirement Statement
T- ED0013969-E001	All printed circuit boards (PCBs) shall meet IPC2221B standard. All wiring and chassis design shall meet UL61010 standard.
T- ED0013969-E002	All station chassis modules shall have unique serial numbers.
T- ED0013969-E003	All station complex subsystem components shall have model, revision and design IDs on them (PCB boards, chassis).

5.2.4. Environmental Conditions

Table 15 Environmental Conditions Requirements

Requirement #	Requirement Statement
T- ED0013969-F001	The station chassis modules shall be able to operate over the temperature range of the PIP-II gallery

5.2.5. Transportability

Table 16 Transportability Requirements

Requirement #	Requirement Statement
T- ED0013969-G001	The station internal chassis connections shall be designed to withstand normal transport and handling acceleration and loads.
T- ED0013969-G002	The chassis shall be sturdy enough to handle transport shocks and not require special handling when being moved.

5.2.6. Software

Table 17 Software Requirements

Requirement #	Requirement Statement
T- ED0013969-H001	The station software application shall have an EPICS interface and communication link with IOC.
T- ED0013969-H002	The software shall provide status indicators for communication link between station hardware and station application on EPICS main page.
T- ED0013969-H003	The software shall provide control to enable/ disable waveforms for all input and output channels.

EPICS will access the registers of the RF Station FPGA using a specialized message based network protocol. The protocol will use a UDP/IP connection. EPICS will send requests to read or write registers controlling the basic system parameters such as phase and frequency, or to get diagnostic information. In addition to registers containing single values, the software will be able to request time stamped buffers of data required for Beam Synchronous Acquisition (BSA).

5.2.6.1. EPICS software

The higher level software will be based on the Experimental Physics and Industrial Control System (EPICS) toolkit. There will be one EPICS IOC instance running for each cryomodule. Where possible, JLab's existing EPICS software for SRF control will be adapted to the PIP-II standard EPCIS Base and naming conventions. It will provide distributed soft real time control at a scale and speed aimed at

operators coordinating LLRF settings and monitoring systems across the facility. Any hard real time functionality will be implemented in firmware, as will state machines to the extent possible. Some processes may be automated in EPICS, but in general processes at the facility level will be High Level Applications in Python or Matlab, using EPICS PVs to communicate.

5.2.6.2. User Interface

The UI software will be the PIP-II standard for EPICS, currently EDM. Screens will be available to control the system at several granularities from facility wide to cavity level. The alarm status infrastructure will propagate error indicators to the facility level, and allow users to click on alarm indicators to drill down to alarm details.

5.2.7. Safety

All modules will be closed so that there is no exposure to shock hazards. Output connectors will not have exposed contacts. Standard electrical safety guidelines shall be followed. Standard ergonomic practices shall be followed for equipment layout. In order to reduce the voltage to ground present in the system, the drive to the Piezo will be differential with a +-50V range. A differential drive will also greatly reduce the effect of ground bounce in the accelerator and EMI both transmitted and received by cabling. The module will be closed so that there is no exposure to shock hazards. Output connectors (1.5) will not have exposed contacts. LOTO procedures will be followed for any connect/disconnect of cables.

The system shall abide by all Fermilab ES&H (FESHM) and all Fermilab Radiological Control Manual (FRCM) requirements including but not limited to:

Electrical Safety
• FESHM Chapter 9110 Electrical Utilization Equipment Safety
•
• FESHM Chapter 9190 Grounding Requirements for Electrical Distribution and Utilization Equipment
Radiation Safety
• FRCM Chapter 8 ALARA Management of Accelerator Radiation Shielding
• FRCM Chapter 10 Radiation Safety Interlock Systems
• FRCM Chapter 11 Environmental Radiation Monitoring and Control
General Safety
• FESHM Chapter 2000 Planning for Safe Operations

Any changes in the applicability or adherence to these standards and requirements require the approval and authorization of the PIP-II Technical Director or designee.

In addition, the following codes and standards in their latest edition shall be applied to the engineering, design, fabrication, assembly and tests of the given system:

NFPA 70 – National Electrical Code
IEC Standards for Electrical Components

In cases where International Codes and Standards are used the system shall follow FESHM Chapter 2110 Ensuring Equivalent Safety Performance when Using International Codes and Standards and requires the approval and authorization of the PIP-II Technical Director or designee.

Additional Safety Requirements that are not listed in the general list above shall be included in the Requirements table in the Functional Requirements section.

5.3. Design and Construction Standards

UL61010 - Laboratory equipment
UL60950 - Computing/Telecommunication Equipment
ASHRAE - Datacenter Standards
IPC-JSTD-001 – Soldering
IPC2221 – PCB spacing and design
IPC-A-600 -- PCB acceptance and testing
IPC-A-610 -- Electronics assembly

6. VERIFICATION

Each chassis module will be tested for each requirement, according to the steps described in the meta data sheet accompanying this TRS.

7. QUALITY ASSURANCE PROVISIONS

- All parts required for the various chassis modules will be procured using Fermilab standard procurement process.
- Visual inspection of all circuit boards will be completed prior to building chassis modules.

Quality control plan is very important document that ensures production quality. To maintain the quality of production following steps will be incorporated for the production process.
1. Inspection of the raw material and components, rejection, and replacement,
2. Appropriate Storage
3. Physical inspection at every stage of sub systems assembly
4. Physical and electrical testing for quality check
5. Qualification of complete chassis (each chassis) for vibration. Wenzel included details about vibration testing.
    a. IEC60068-2-27 (Shock): General test for robustness, handling, and transport for land-based items
    b. IEC60068-2-64 (Vibration)
6. Burn in/ Stability tests: 168 hours at room temperature or 48 hrs. at +35 degree C ambient temperature
7. EMI/EMC qualification as per the standards:

a. IEC61204: P/S stabilized low voltage at CW operation
b. IEC61204-3: Emission & Immunity
c. IEC-61010-1 safety rules for the electric appliances of measurement regulations and laboratory.

8. Functional testing after all the qualification tests

APPENDIX A – *(NOTES, BACKGROUND, DIAGRAMS, CALCULATIONS, ETC.)*

The architecture of an example controller chassis using an SOC FPGA with adequate logic resources memory and I/O is shown in Figure 10. .

Table 18

Device Feature	Specifications	Number of Channels
High Speed ADC	16-bit, 125 MSPS	16
High Speed DAC	14-bit, 125 MSPS	8
Low speed DAC	16-bit, 200 kSPS	4
FPGA	ARRIA10	660k LE
Processor	Dual Core ARM	1.6 GHz
DDR4 (Processor)	32-bit, 2400 MT/s	4 GB
DDR4 (FPGA)	32-bit, 2400 MT/s	4 GB
Software/Configuration	eMMC/EPCQ	32 GB/512MB
18x19 multipliers	Fixed Point	3,376
Variable-precision DSP blocks	SP Floating Point	1,688
Digital Inputs (Triggers)	TTL, 50 Ω	8
Digital Outputs	TTL, 50 Ω	16
Gbit Ethernet	RJ45	2
High Speed Xcvrs	QSFP, 4x10 Gbps	3
USB	2.0, 3.0	1x, 1x

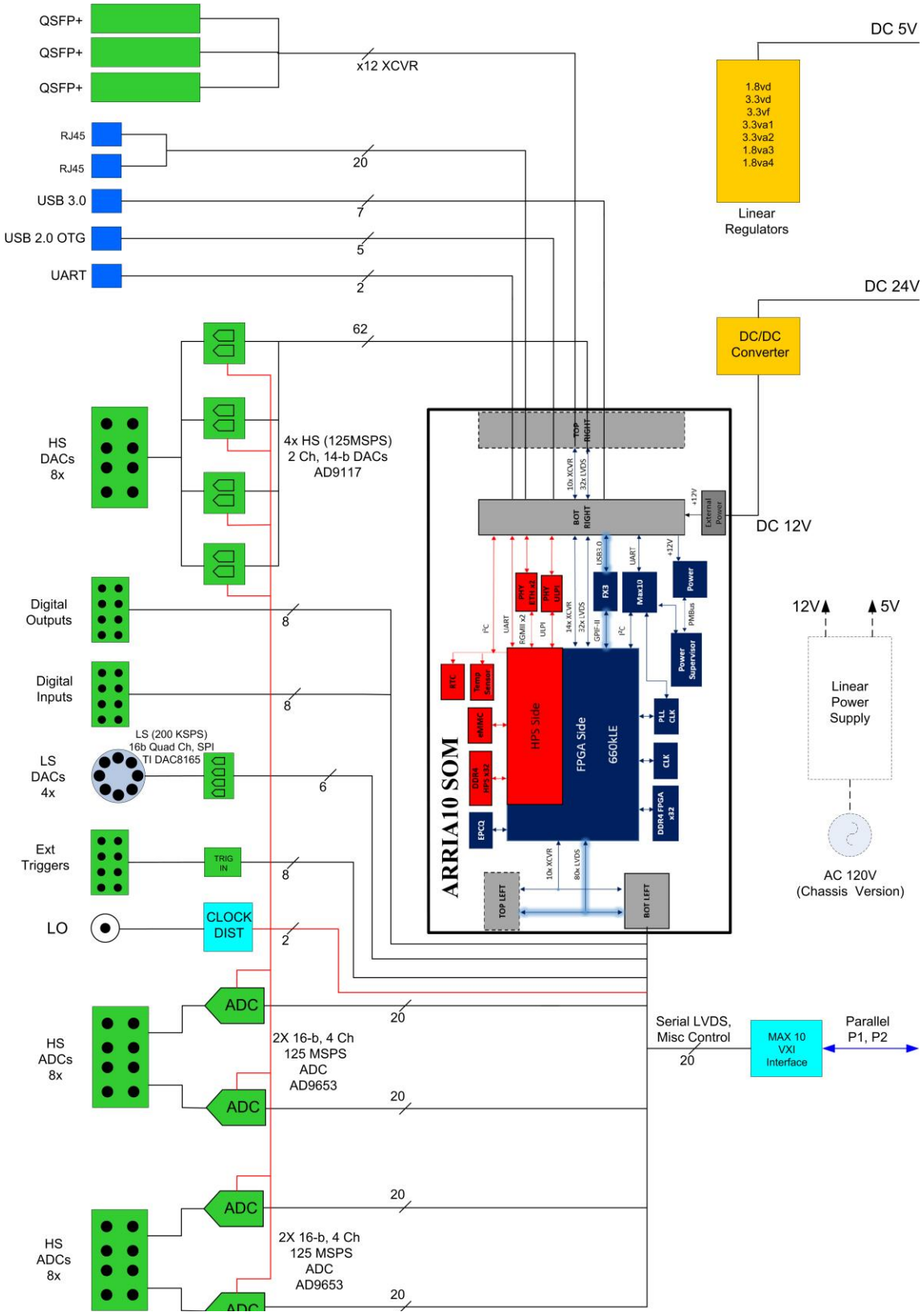
QSFP+
QSFP+
QSFP+
x12 XCVR
RJ45
RJ45
20
USB 3.0
7
USB 2.0 OTG
5
UART
2
62
HS DACs 8x
4x HS (125MSPS) 2 Ch, 14-b DACs AD9117
Digital Outputs
8
Digital Inputs
8
LS (200 KSPS) 16b Quad Ch, SPI TI DAC8165
LS DACs 4x
6
Ext Triggers
TRIG IN
8
LO
CLOCK DIST
2
ADC
20
HS ADCs 8x
2X 16-b, 4 Ch 125 MSPS ADC AD9653
ADC
20
ADC
20
HS ADCs 8x
2X 16-b, 4 Ch 125 MSPS ADC AD9653
ADC
20
DC 5V
1.8vd
3.3vd
3.3vf
3.3va1
3.3va2
1.8va3
1.8va4
Linear Regulators
DC 24V
DC/DC Converter
DC 12V
ARRIA10 SOM
HPS Side
FPGA Side
660kLE
TOP RIGHT
BOT RIGHT
TOP LEFT
BOT LEFT
12V
5V
Linear Power Supply
AC 120V (Chassis Version)
Serial LVDS, Misc Control
20
MAX 10 VXI Interface
Parallel P1, P2

Figure 10