Proof of Concept prototype structure

Wojciech CICHALEWSKI on behalf of DMCS team

About Me:

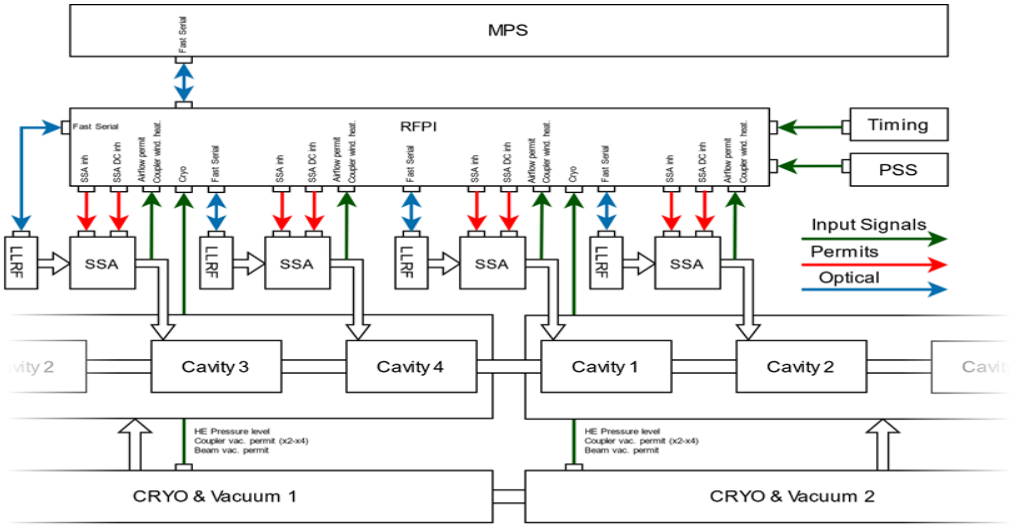
Wojciech CICHALEWSKI
Ph.D. in Electrical Engineering

- Role:
  - TUL in-kind for PIP-II technical coordinator,
  - Local RFPI project Manager.

- Relevant Experience:
  - LLRF: FLASH, E-XFEL, ESS-ERIC (elliptical cavities), PolFEL
  - Technical coordinator of the DMCS - TUL accelerator related projects as LLRF Group leader (2010 – present)
  - DESY: Automation and software engineer in LLRF system development (2002-2019),
  - ESS-ERIC: PEG project „LLRF systems” manager deputy, System engineer – local LLRF system test-stand preparation, operation and updates (2016-present).

The RFPI system design - requirements

Signal Name	Quantity
Field Emission Probe (FEP)	1 per cavity/coupler
Coupler Bias Current (A)	1 per cavity/coupler
Coupler Bias Voltage (V)	1 per cavity/coupler
RF antenna (NIRP)	1 per cavity/coupler + 1 per CRYOMODULE
Cryo (He Pressure & Level) Permit	1 per CRYOMODULE
Coupler Airflow Permit	1 per cavity/coupler
Coupler Vacuum Permit	1 per cavity/coupler
Beam Vacuum Permit	1 per CRYOMODULE
Personnel Safety Permit	1 per cavity/coupler
Coupler Temperature Probe RTD 1	1 per cavity/coupler
Coupler Temperature Probe RTD 2	1 per cavity/coupler
LLRF Ready (RF level status, Ready status, quench)	1 per cavity/coupler
SSA Ready	1 per cavity/coupler
SSA Permit Out	1 per cavity/coupler
SSA DC Permit Out	1 per cavity/coupler
LLRF Permit Out	1 per cavity/coupler
MPS Permit Out	1 per cavity/coupler



	Output Permits from RFPI (LB/HB)			
Inputs to RFPI	LLRF permit	SSA Permit	SSA_DC Permit	MPS
FEP	x			x
RF antenna (NIRP)	x	x		x
Personnel Safety Permit	x	x		x
Vacuum Status	x	x		x
Coupler Vacuum Permit (Multipacting)				x
He Level & Pressure (Cryo)	x	x		x
Temperature Sensors (RTD 1& 2)	x	x		x
Coupler Airflow Sensor	x	x		x
HV Coupler Bias voltage	x	x		x
HV Coupler Bias current	x	x		x
SSA Ready	x			x

The RFPI system design - requirements

Source	Signal	Function	Specifications
FEP	analog	limit for couple field emissions	TTL into 50 ohms
Stray RF Detection (NIRP)	analog RF/162.5-1300 MHz	Limit for non-ionizing radiation	Sine, 0 dBm into 50 ohms
Personnel Safety Permit	contact switch	Personnel safety system permit	Permit drops when metal contact switch is open
Vacuum Status	Broadband RF	Vacuum permit	Permit drops when metal contact switch is open
Coupler Vacuum gauge	contact switch	Vacuum permit	Permit drops when metal contact switch is open
Cryogenics Status	contact switch	Cryogenics permit	Permit drops when metal contact switch is open
Temperature Sensors (RTD 1 & 2)	Analog	Window temperature	0-10V
Coupler Airflow Sensor	contact switch	Coupler airflow permit	Permit drops when metal contact switch is open
HV Coupler Bias voltage	analog	Limit for power supply levels	0-10V signal
HV Coupler Bias current	analog	Limit for power supply levels	0-10V signal
SSA Ready	digital	HLRF permit	TTL into 50 ohms
LLRF Status	digital	LLRF system permit	High-speed serial link

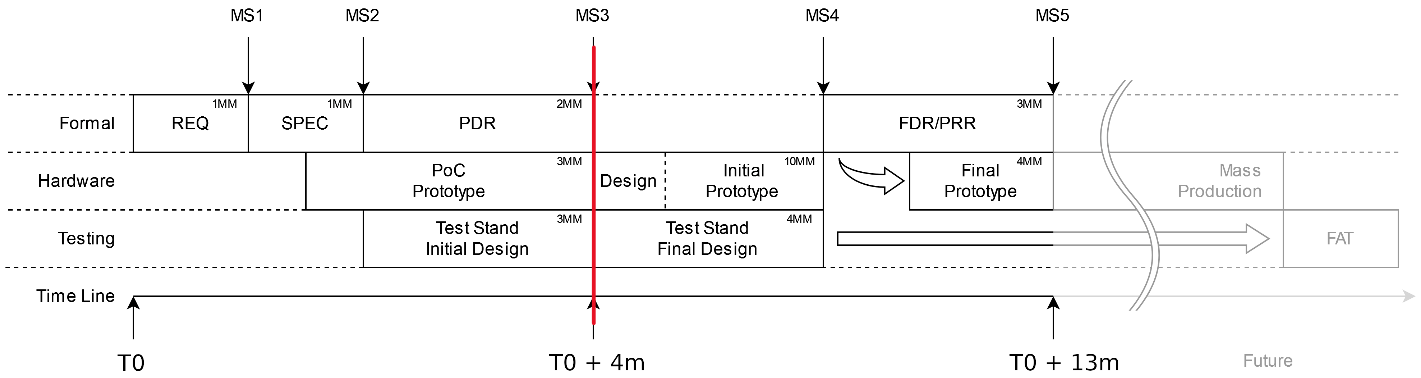
Destination	Signal	Function	Specifications
SSA	digital output	Permit	TTL into 50 ohms
SSA DC	digital output	Permit	TTL into 50 ohms
LLRF System	digital output	Permit	TTL into 50 ohms
MPS System	digital output	Permit	TTL into 50 ohms

RFPI system design flow

New design of the RFPI system.

Three system prototypes version before mass production:

- Proof of Concept prototype,
- Initial Prototype,
- Final Prototype,



The Proof of Concept prototype

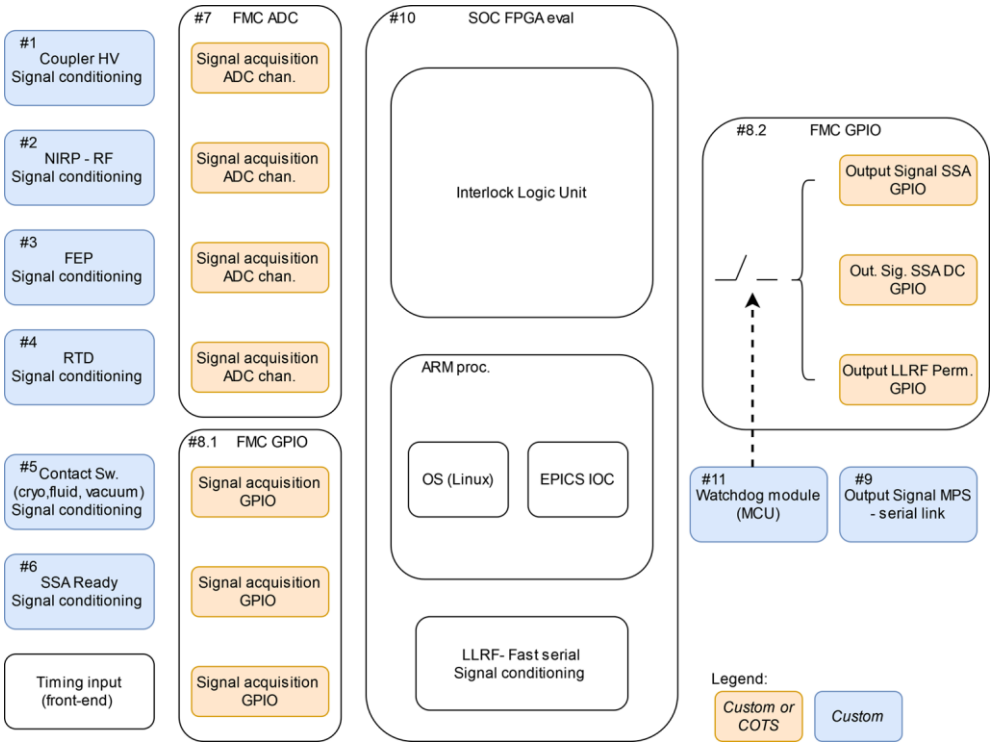
The **proof-of-concept prototype goal** is to **create and test basic building blocks** of the **RFPI target** system.

PoC **scope (**according **to SOW)**:

- Design and Production of Test Board for each type of external interface present in the system.
- Design and Production of Test Board for selected internal features, which will be identified as requiring detailed verification.
- Implementation of dedicated system logic (e.g. firmware blocks) to interface with the Test Boards.
- Preparation of dedicated test and measurement plans for each element of the PoC.
- Execution of measurement plans to verify electrical properties, delays, and limitations of each element.

The PoC structure

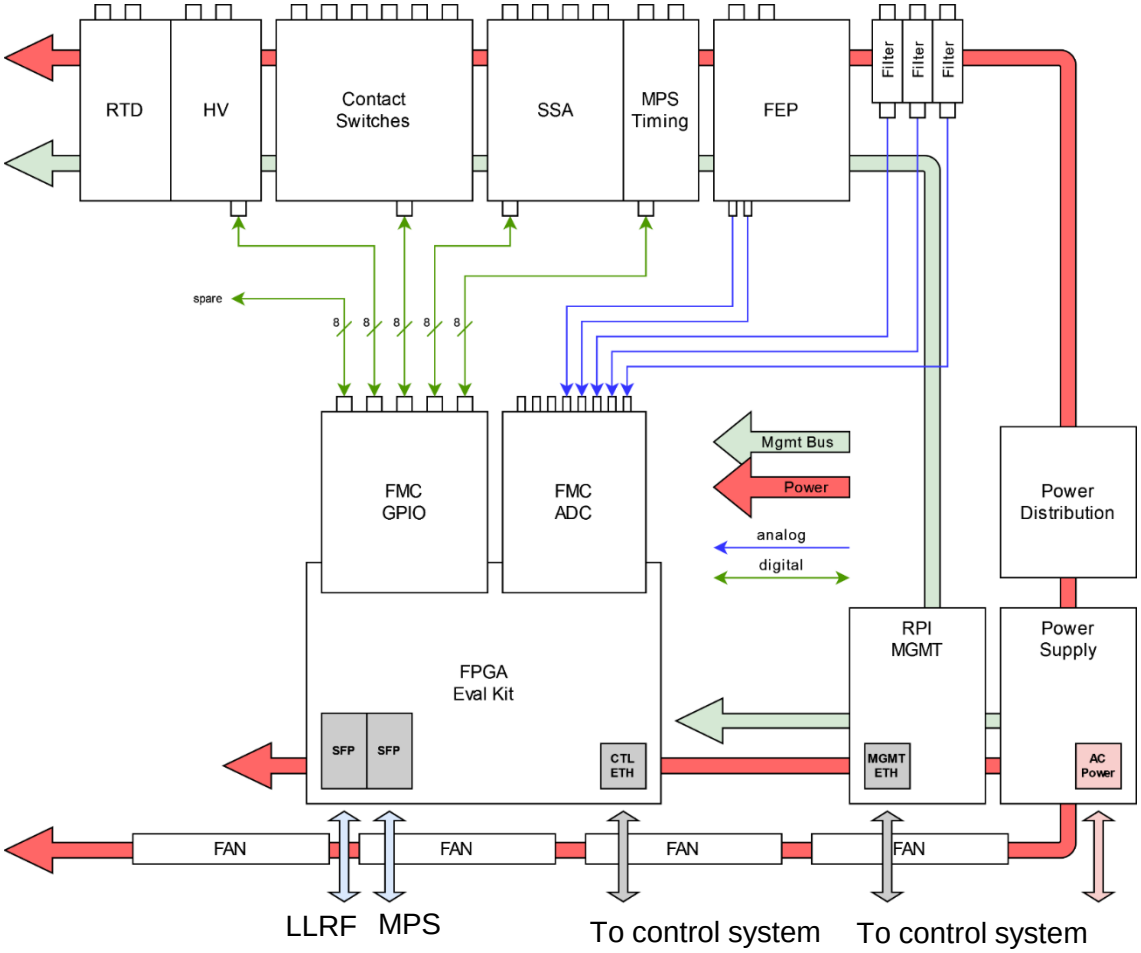
- Main logic realized by the reprogrammable logic unit (FPGA unit),
- Modular system design to allow flexibility of functionality and signals quantity configuration,
- Dedicated signal conditioning modules for each logical signal type,
- Integrated management and diagnostics for system reliability monitoring and instant malfunction diagnosis,

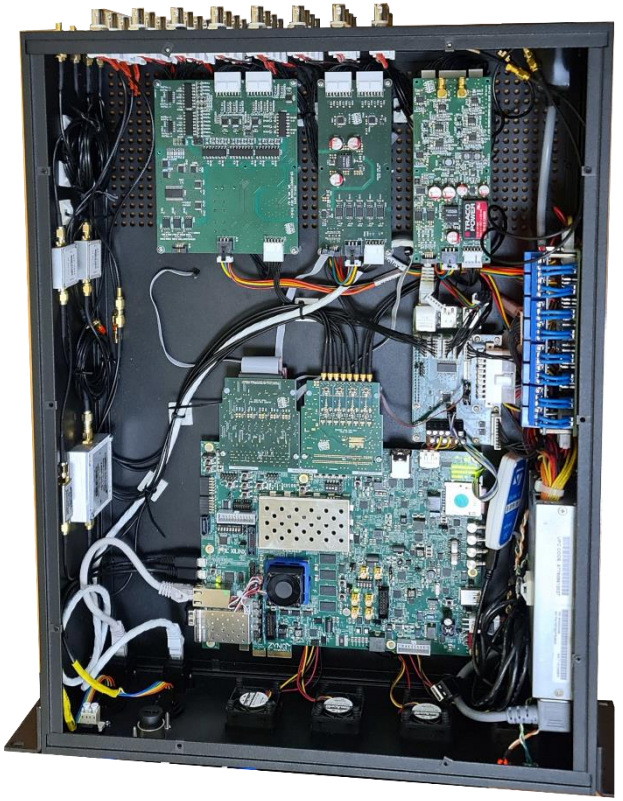


PoC design goals

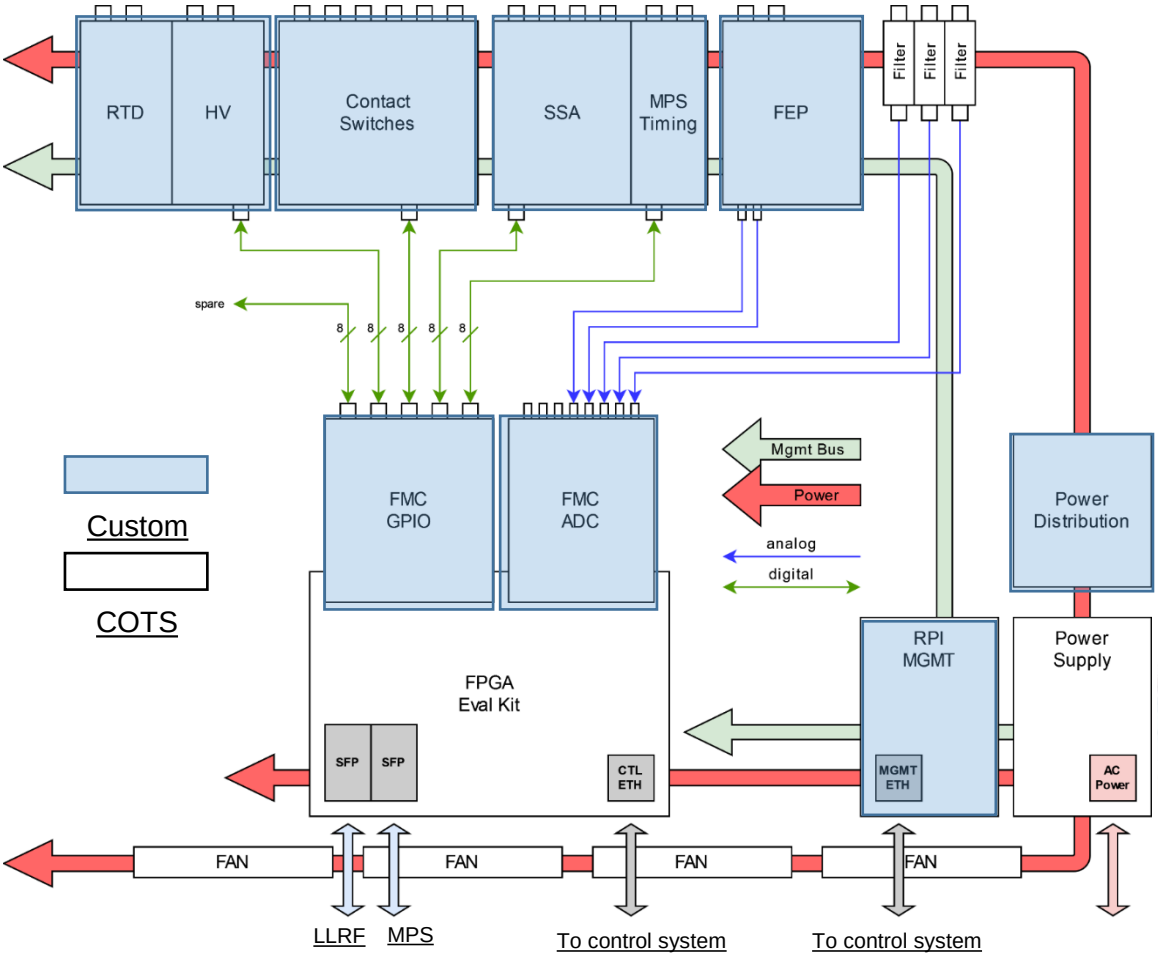
- Propose new RFPI design based on the reconfigurable logic device (FPGA/SoC) for safety algorithm realization,
- Include representation of each identified signal type,
- Verification of the design correctness and performance for each input/output (to be handled in the RFPI final version),
- Not full-scale system design prototype,
- Prototype build from the custom designed and produced hardware/software modules and COTS,
- Close integration of diagnostics features (temperature, voltages, current measurements, watchdog protection to block main logic unit output) and management features (individual modules power management, watchdog protection, remote debugging and programming of the main logic chip - with provided JTAG interface),
- Minimise workload needed for integration with the existing/planned PIP-II infrastructure on the firmware and software level – follow provided naming conventions, frameworks, programming rules and guidelines.

The PoC hardware overview





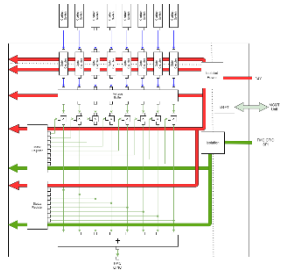
The PoC hardware overview



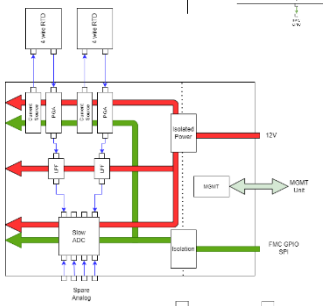
The PoC hardware overview

- **NIRP input signal conditioning module,**
  - ***Details: Grzegorz Jabłoński***
    „Signal Conditioning: NIRP sub-module”

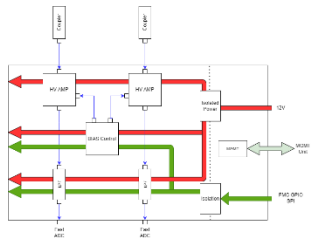
- **Contact Switches input signal conditioning module,**
  - ***Details: P. Marciniak & B. Pękosławski***
    „HW for signal conditioning: Contact Switches”



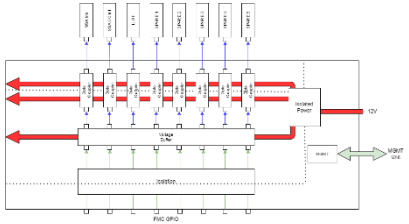
- **RTD and coupler high voltage monitoring input signal conditioning module,**
  - ***Details: P. Marciniak & B. Pękosławski***
    „HW for signal conditioning: RTD”



- **Field Emission Probe (FEP) input signal conditioning module**
  - ***Details: P. Marciniak & B. Pękosławski***
    „HW for signal conditioning: Contact Switches”

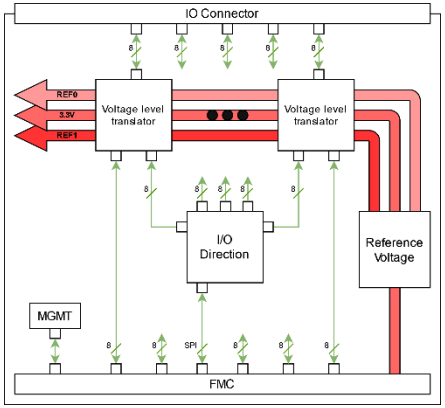


- **Solid State Amplifier (SSA) output signals conditioning module**
  - ***Details: P. Marciniak & B. Pękosławski***
    „HW for signal conditioning: SSA and HV”

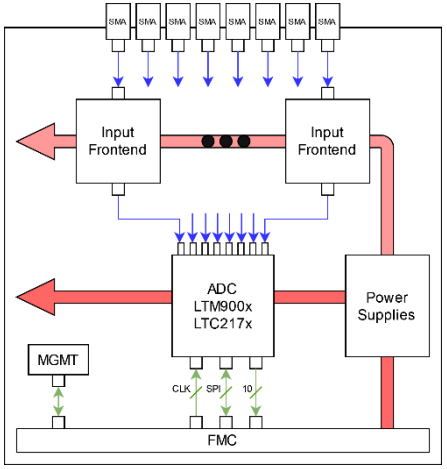


The PoC hardware overview

- **FMC GPIO**
  - ***Details: Piotr Amrozik „Main logic realization/execution HW”***



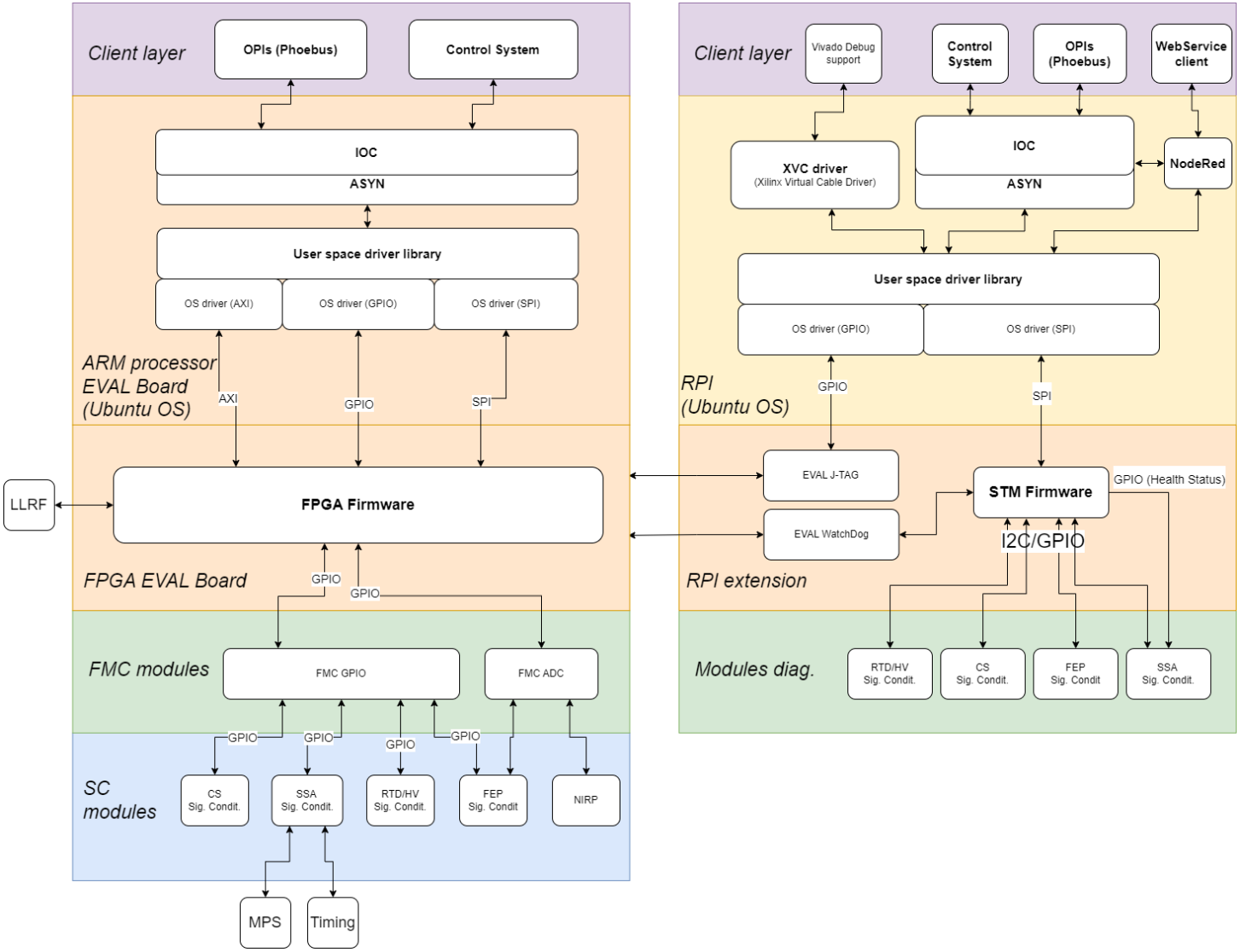
- **FMC fast ADC,**
  - ***Details: Piotr Amrozik „Main logic realization/execution HW”***



The PoC software overview

- The RFPI prototype software divided in two main blocks:
  - SW/FW for the main logic unit and peripherals interface and management,
  - SW/FW for diagnostics and management subsystem.
- Software structure unified (as much as possible) for both parts,
- Firmware developed for the Xilinx Zynq Ultrascale FPGA (ZU7EV-2FFVC1156), based on the delivered by manufacturer interface protocol (Advanced eXtensible Interface - AXI),
- Firmware for the STM chip to manage I2C communication with the sensors and actuators on the various modules,
- The Ubuntu OS chosen as feasible for both platforms (Xilinx board and Raspberry Pi),
- The EPICS control system chosen for both implementations – to be consistent with the overall linac infrastructure.

The PoC software overview

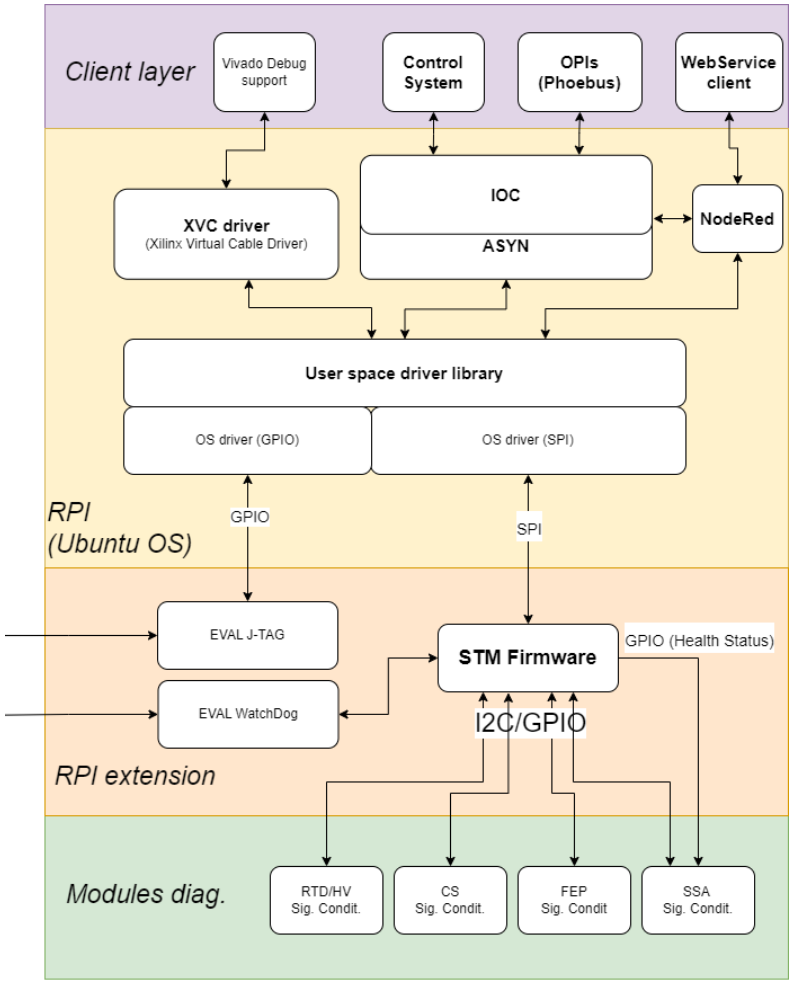


The PoC software overview – management and diagnostics

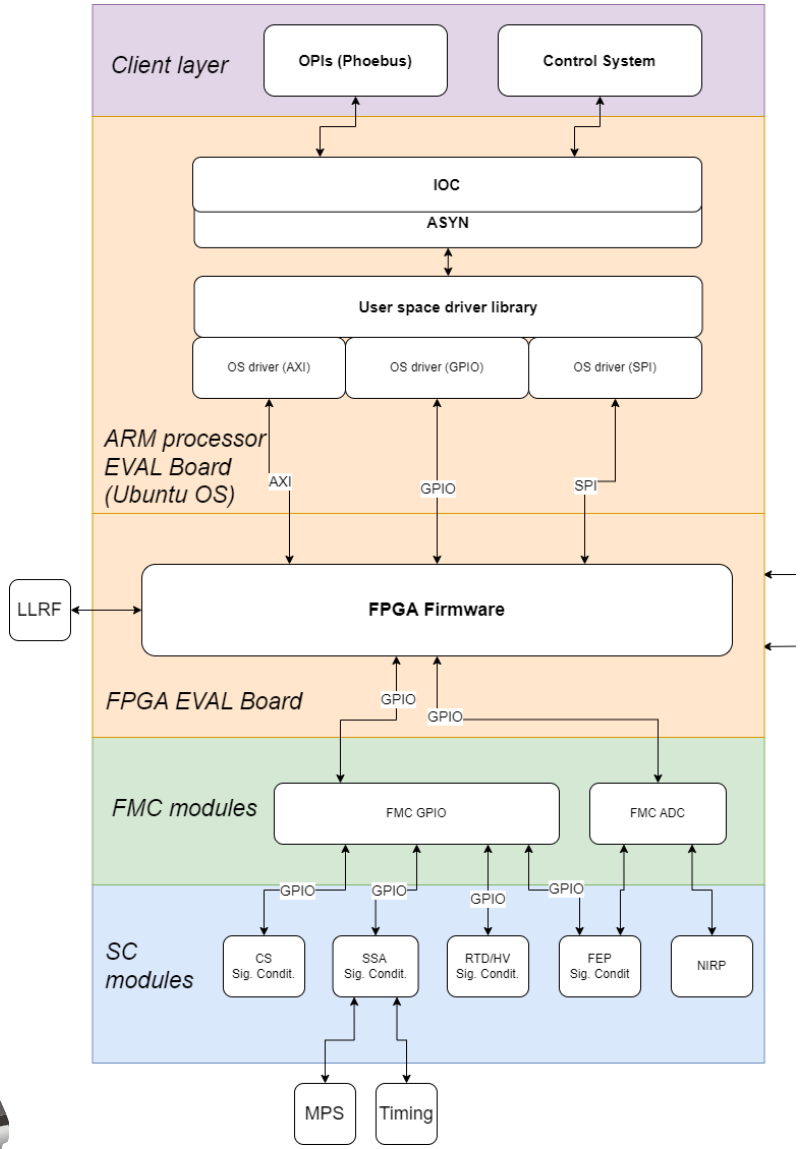
- STM chip firmware:
  - Read/write sensors data,
  - Provide watch-dog functionality
  - Health Status signal,
  - Fans management,
  - Relay switches control.

- OS level software:
  - provided OS driver used for GPIO communication,
  - provided OS driver used for SPI communication,
  - User space library developed for interfacing hardware, accompanied with command line tools,
  - EPICS layer IOC incorporating ASYN driver,
  - OPI under development using Phoebus or/and CSS,
  - Alternative NodeRed implementation for the cross-verification purposes.

- ***Details: Wojciech Tylman „SW for the management and watchdog”***



The PoC software overview



- FPGA firmware:
  - Read/write signals from the FMC modules (from S.C. modules),
  - Provide main RF and SSA output blocking functionality,
  - Health Status signal verification,
  - Communication with LLRF, MPS systems
- OS level software:
  - provided AXI driver,
  - provided OS driver used for GPIO communication,
  - provided OS driver used for SPI communication,
  - User space library developed for interfacing hardware, accompanied with command line tools,
  - EPICS layer IOC incorporating ASYN driver,
  - OPI under development using Phoebus or/and CSS,
- ***Details: Rafał Kiełbik „SW for the main functionality”***

The PoC status and path forward

- Status:
  - All hardware modules designed, verified and produced,
  - Hardware platform integrated and running,
  - Individual HW modules tested and verified,
  - Weak points of the design of each module has been identified and recognized – to be corrected on the HW and/or FW/SW level,
  - FW/SW initial version of the management & diagnostics ready including STM firmware, user library and EPICS IOC,
  - FW for the main logic partially prepared and verified – for dedicated modules operation and data acquisition.

- Path forward:
  - FW/SW work on the design integration (with tight cooperation with the LLRF collaboration team),
  - Clarification and implementation of missing interfaces (Timing, MPS, LLRF),
  - Integrated PoC tests in laboratory,
  - PoC tests @ PIP-II TestStand (Q1-Q2.2023),
  - Engineering specification document preparation,
  - Full scale system design with full custom electronics.

Summary

- The proof-of-concept prototype is the first stage of the new RFPI system design (before full scale and final prototypes),
- The hardware and software structure of this RFPI prototype has been proposed and accepted,
- Majority of the hardware modules has been developed, designed and produced locally (by DMCS),
- Produced modules has been tested individually,
- System have been integrated and prepared for testing,
- Software for main modules and the diagnostics and management has been proposed and is under development,
- Tests at the PIP-II modules test facility are planed (Q1 2023),
- Lesson learned from the PoC evaluation will be used for the full-scale system design/preparation.

Thank You