POC Hardware

Wojciech Jałmużna

About Us

Wojciech Jałmużna

Ph.D. in Electrical Engineering

- Role
  - RFPI project contractor
  - FPGA/software engineer
  - Hardware Designer
- Relevant experience
  - FLASH/XFEL LLRF Systems (2003-2012): HW/FW designer
  - Various electronics systems for HEP (2012-2018): HW/FW designer
  - ESS-ERIC: FPGA/software engineer (since 2018)
  - POLFEL LLRF and Piezo Control: HW/FW designer

Agenda

- The main requirements
- The PoC version specification and scope
- The functionality and design details
- Implementation
- Test results discussion
- Full scale design plans
- Summary

The main requirements

Critical points for complex hardware systems

- Reliability
- Scalability
- Maintainability
- Long Life time/ Long Support
- Ease of use

Some (or even all of the points) are covered by many industrial/scientific modular hardware standards such as:

- ATCA
- uTCA
- etc.

They usually have quite high overhead and/or entry threshold. During the discussions with FNAL team we concluded that custom box implementation can fulfil requirements of the final system

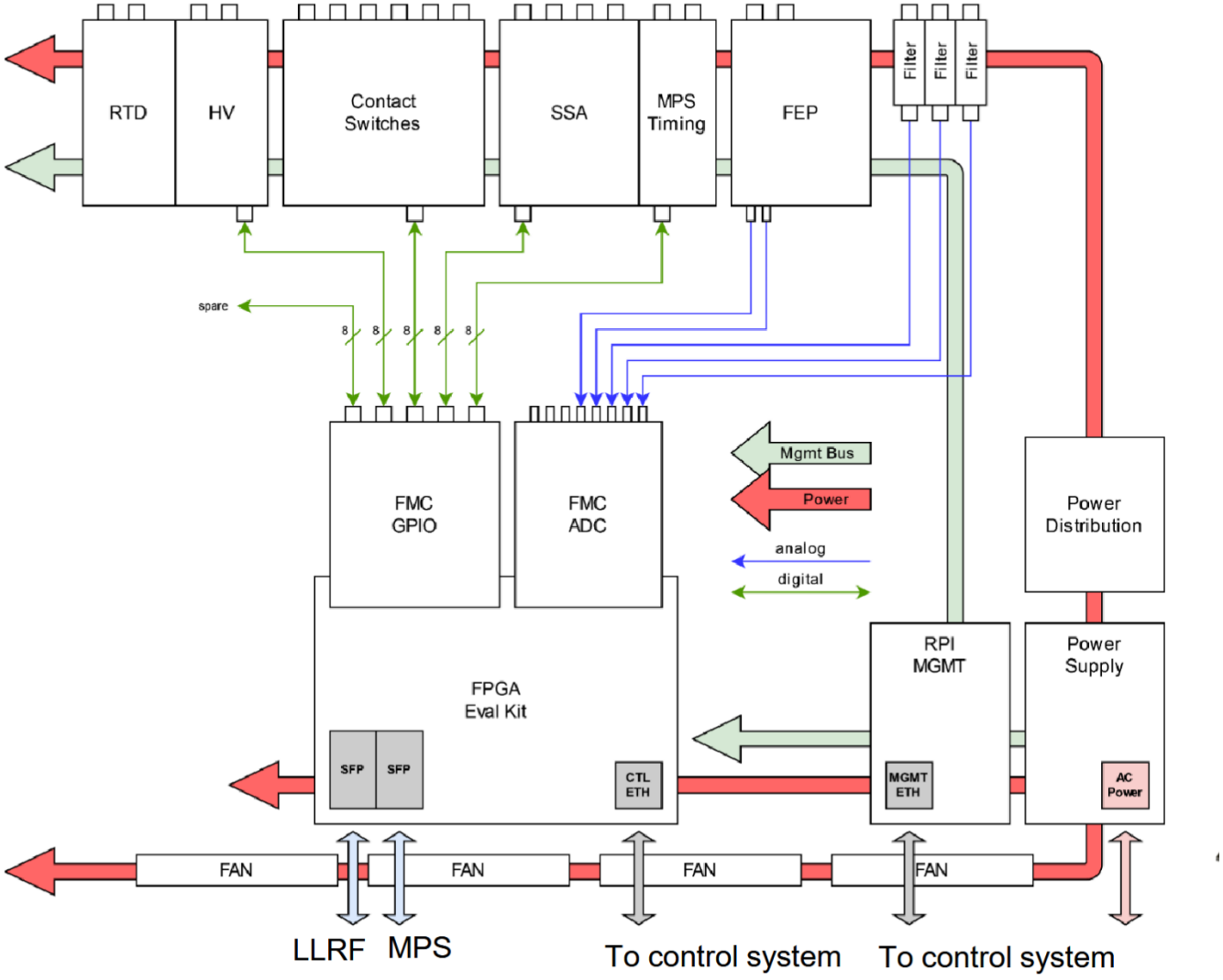
The PoC version specification and scope

- Most important part of POC is to check:
  - analog front-ends
  - data flow concept
  - integration of various parts on all levels
  - hardware/software workflows
- There was no focus to include final number of channels
- We decided to use as many off-the-shelf components as possible
- Since the system will work in distributed environment with many connections, we tried to provide electrically isolated interfaces to the outside

The PoC version specification and scope

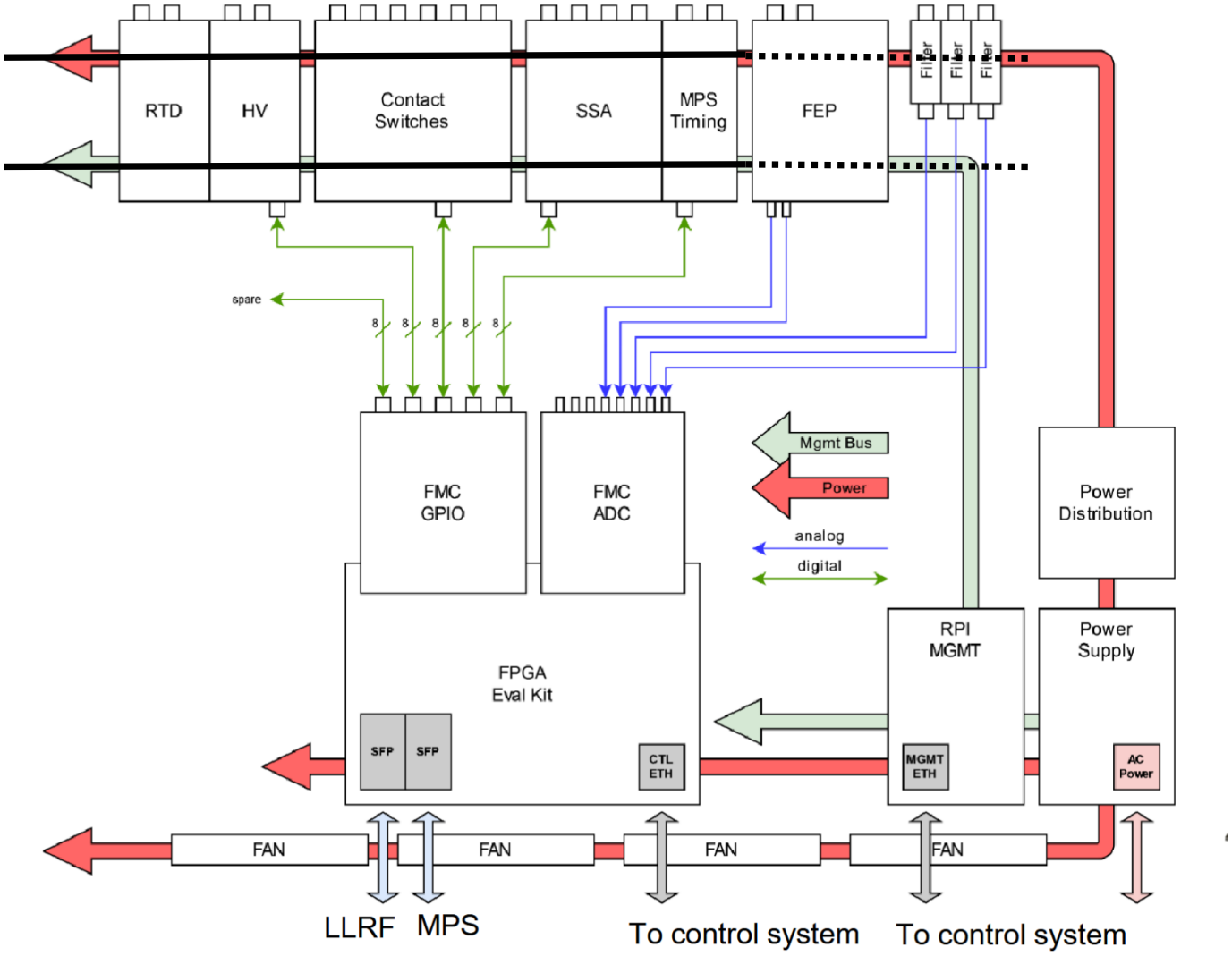
- System is designed as modular as possible
  - Distributed/parallel design efforts/reduced time to lab
- Custom Modules as simple as possible
  - Not more than 8 layers
  - Preferred component size is 0603+. In some cases 0402 were used, but in general avoided
  - rapid prototyping
    - Fast manufacturing of PCB
    - In-House assembly

The functionality and design details



The functionality and design details

Isolation lines



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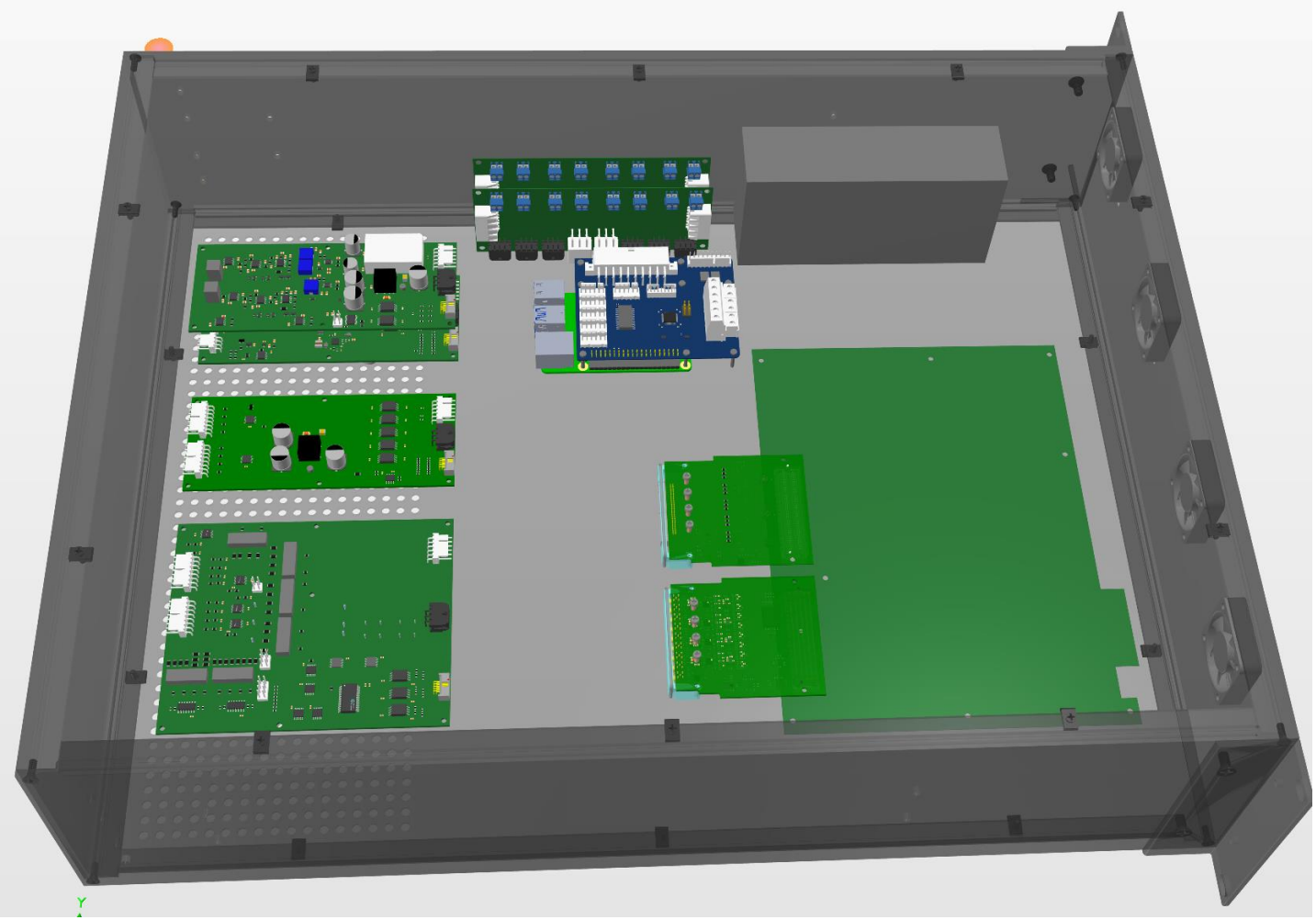

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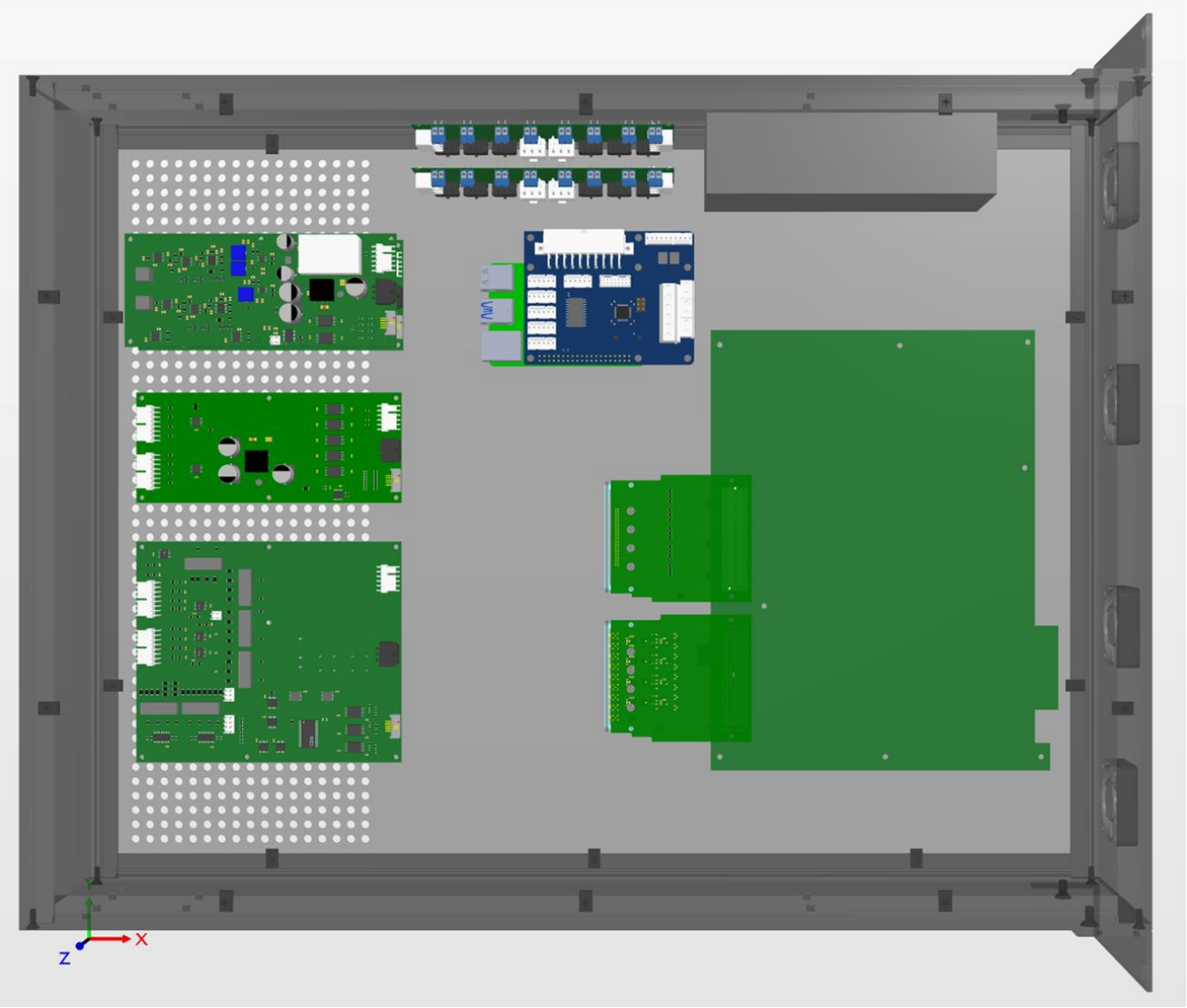
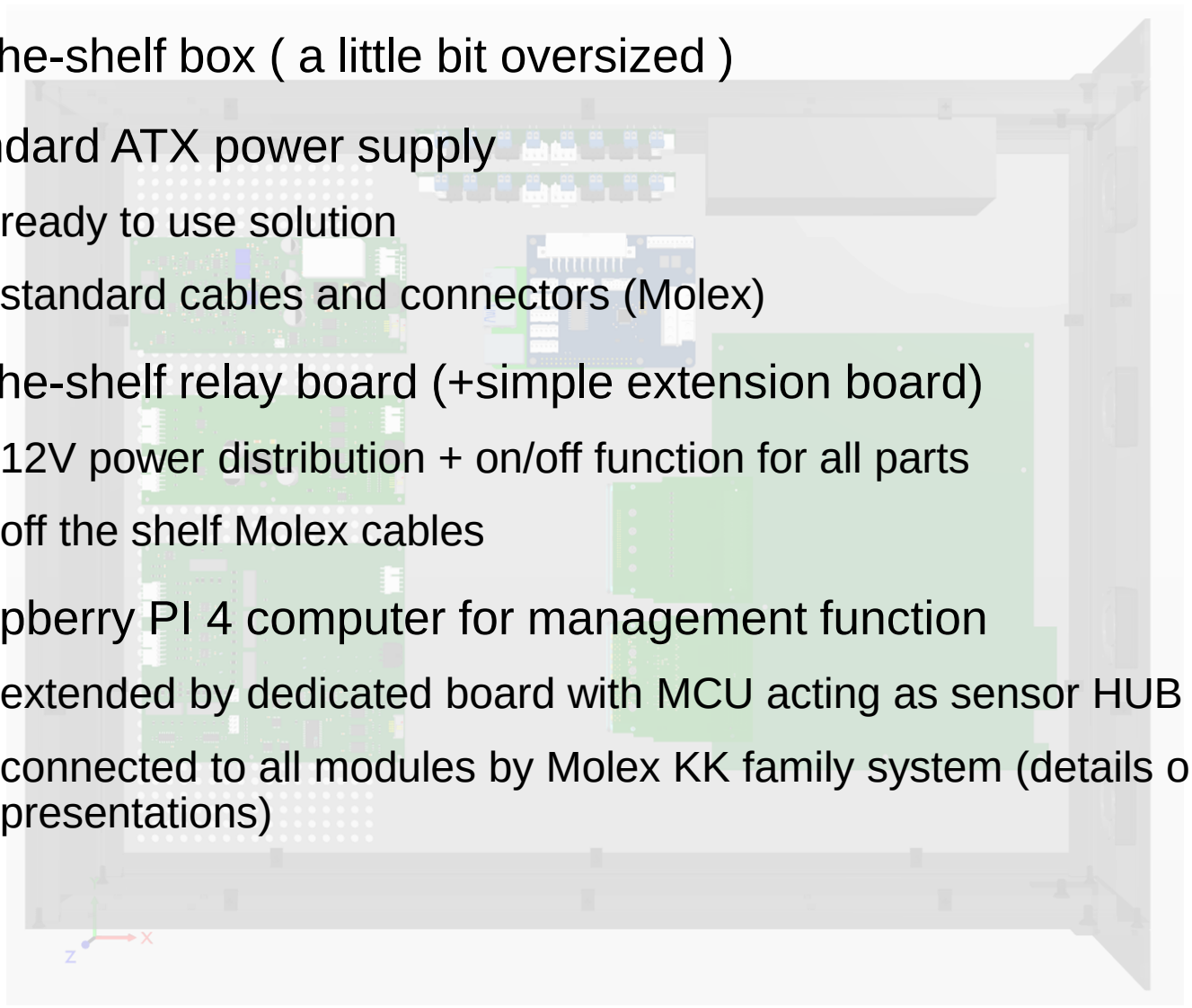


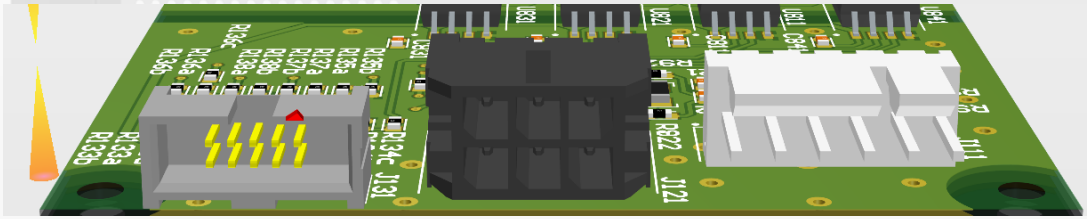
Implementation

- off-the-shelf box (a little bit oversized)
- standard ATX power supply
  - ready to use solution
  - standard cables and connectors (Molex)
- off-the-shelf relay board (+simple extension board)
  - 12V power distribution + on/off function for all parts
  - off the shelf Molex cables
- Raspberry PI 4 computer for management function
  - extended by dedicated board with MCU acting as sensor HUB
  - connected to all modules by Molex KK family system (details on next presentations)



Implementation

- Xilinx ZCU106 Eval kit
  - selection based on available FMC slots and their pinouts
- FMC modules
  - GPIO to provide FPGA->Logic interface in the box
  - ADC to provide digitizing possibilities for analog parts
- Signal Conditioning Boards
  - described on separate presentations
  - 2 form factors – standard electrical interface
  - Molex KK connectors for back panel connection
  - Flat Ribbon Cable (25 mil pitch) for GPIO connection

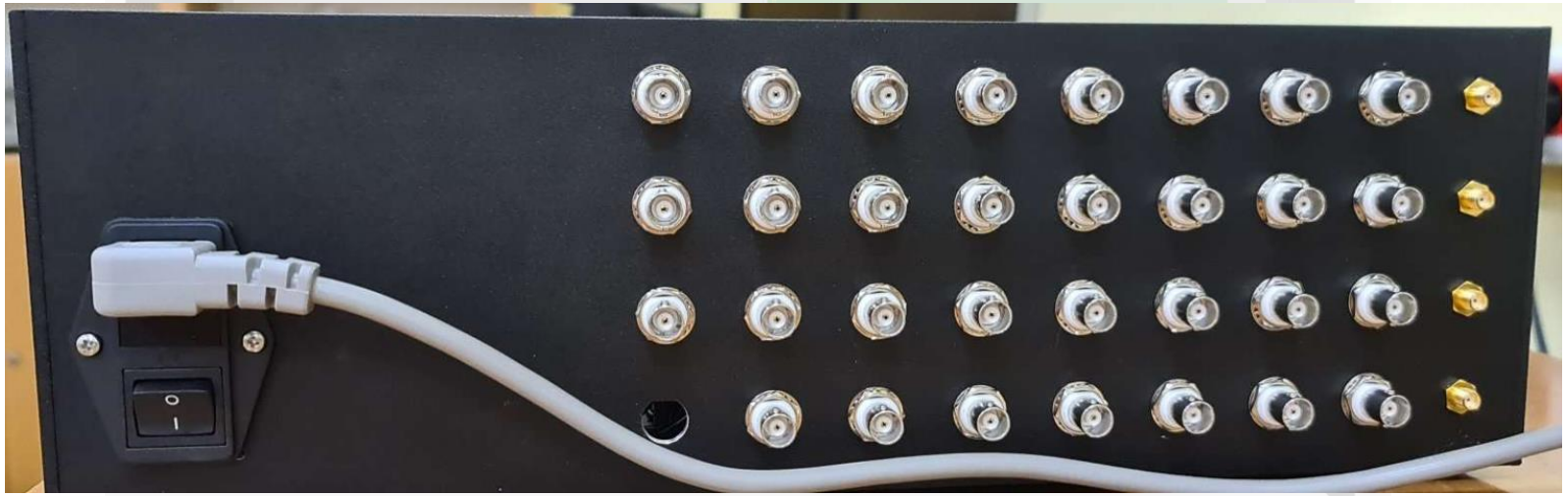


Implementation

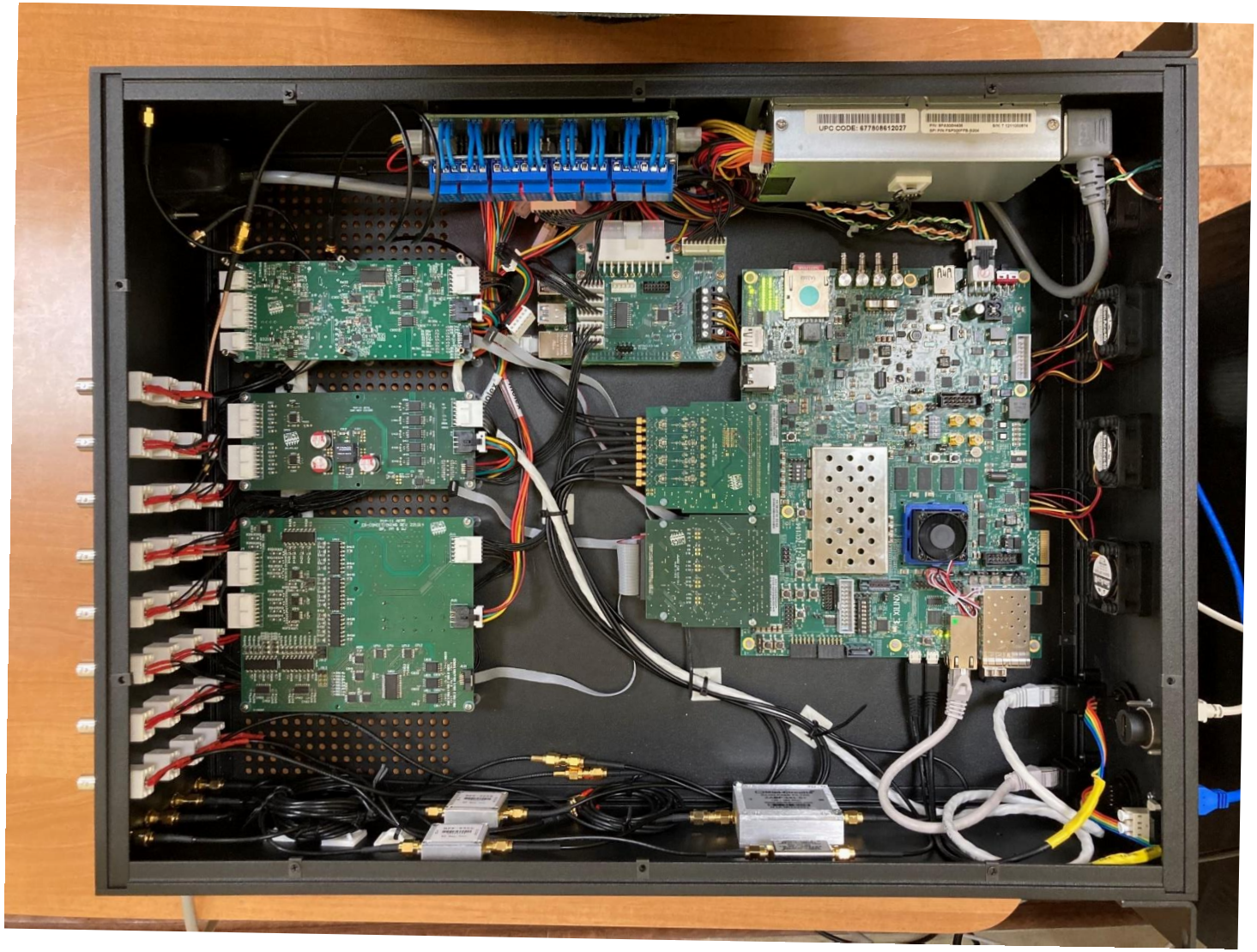
- RF Filters
- Front Panel Interfaces
  - PC connectors patched to the panel (USB/ETH/HDMI_
  - Fiber Links patched to the panel

Implementation

- RF Filters
- Back Panel Interfaces
  - Final connectors for the system not decided yet
  - Back Panel used as patch panel for interfaces
  - For now all interfaces using BNC (+SMA for RF)

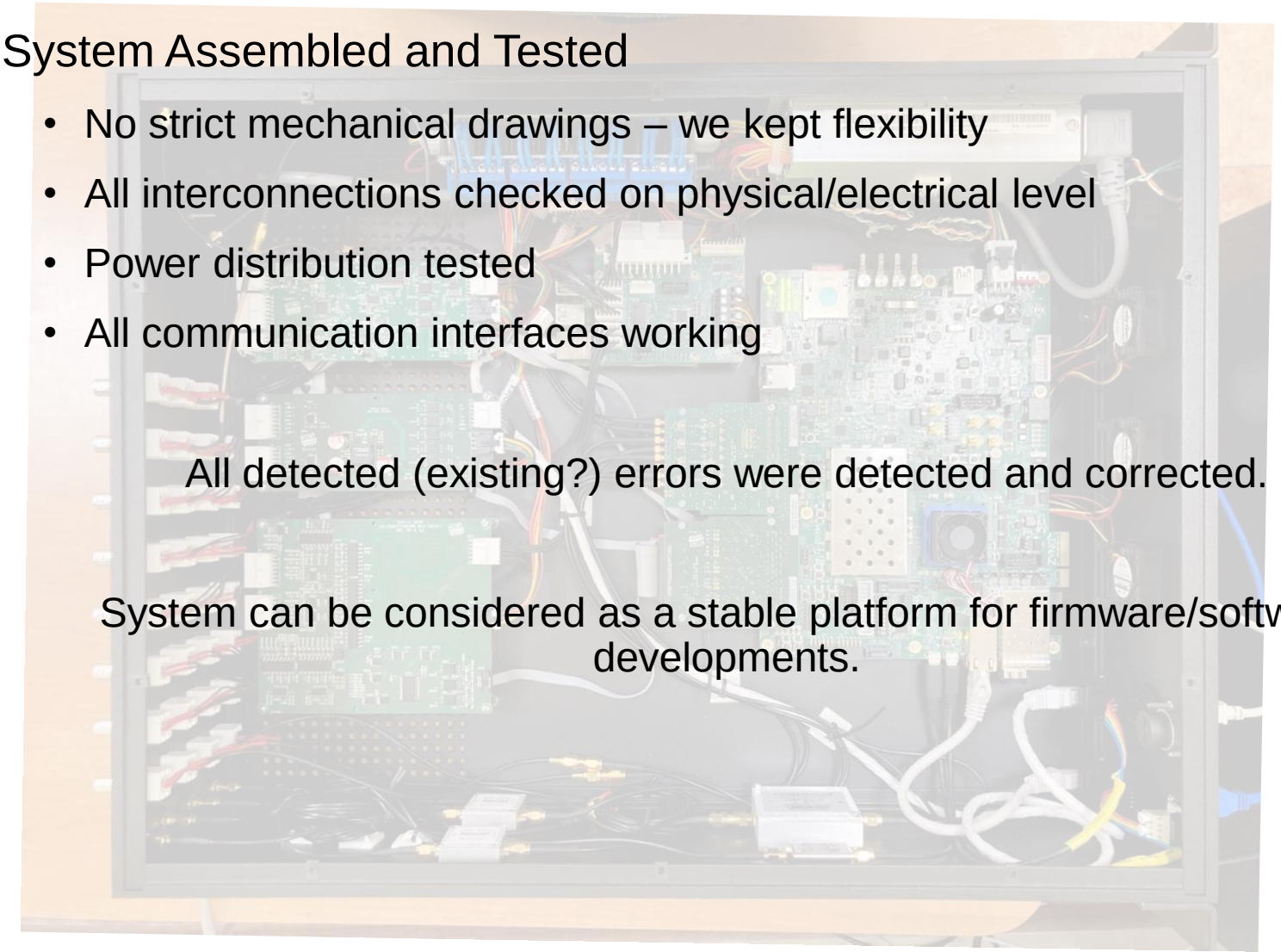


Implementation



Test results discussion

- System Assembled and Tested
  - No strict mechanical drawings – we kept flexibility
  - All interconnections checked on physical/electrical level
  - Power distribution tested
  - All communication interfaces working



All detected (existing?) errors were detected and corrected.

System can be considered as a stable platform for firmware/software developments.

Full scale design plans

Assuming we do not go into industrial standard and stay with the box solution

- We want to stick to Xilinx Family
- We want to keep mgmt./diag separated from main function
  - Raspberry PI seems nice choice for management
- We want to keep system modular

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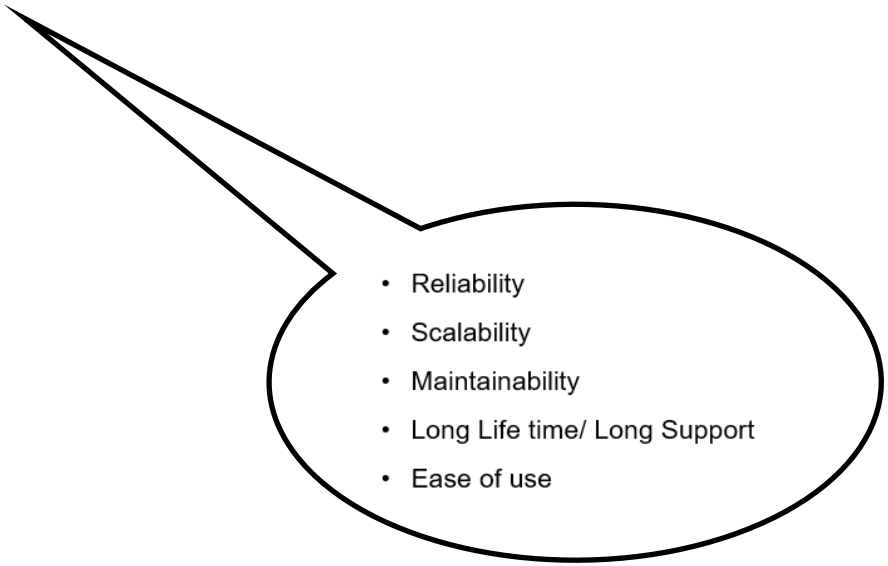

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  - Raspberry PI seems nice choice for management
- We want to keep system modular
- Complex cabling is not nice and limiting
  - Creates mess
  - Limits number of interconnections
  - Kills maintainability
  - Adds modules not fully related to main system function

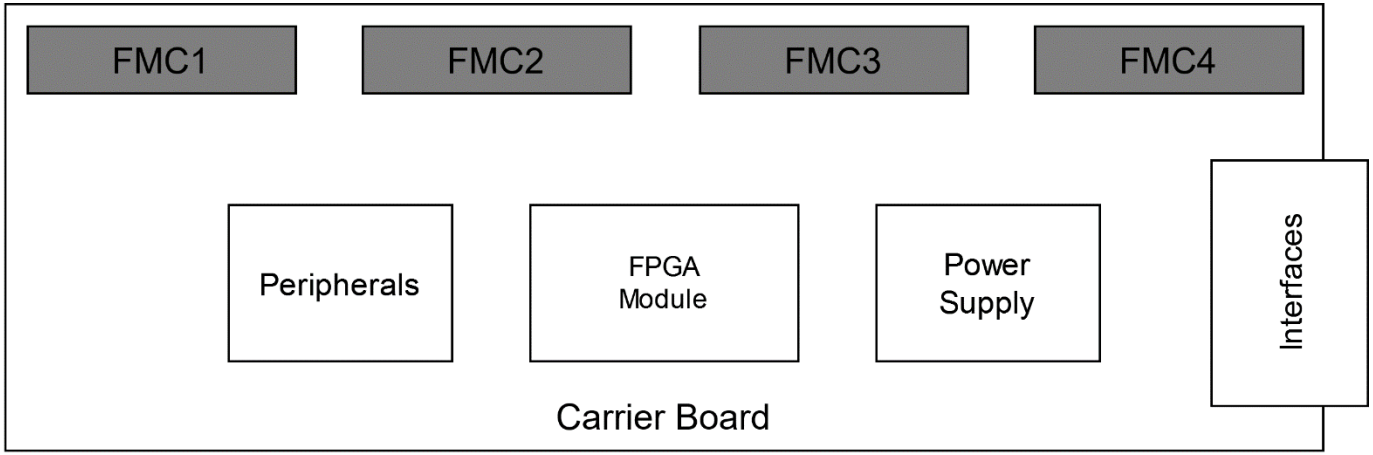
Full scale design plans

Final Solution Possibilities:

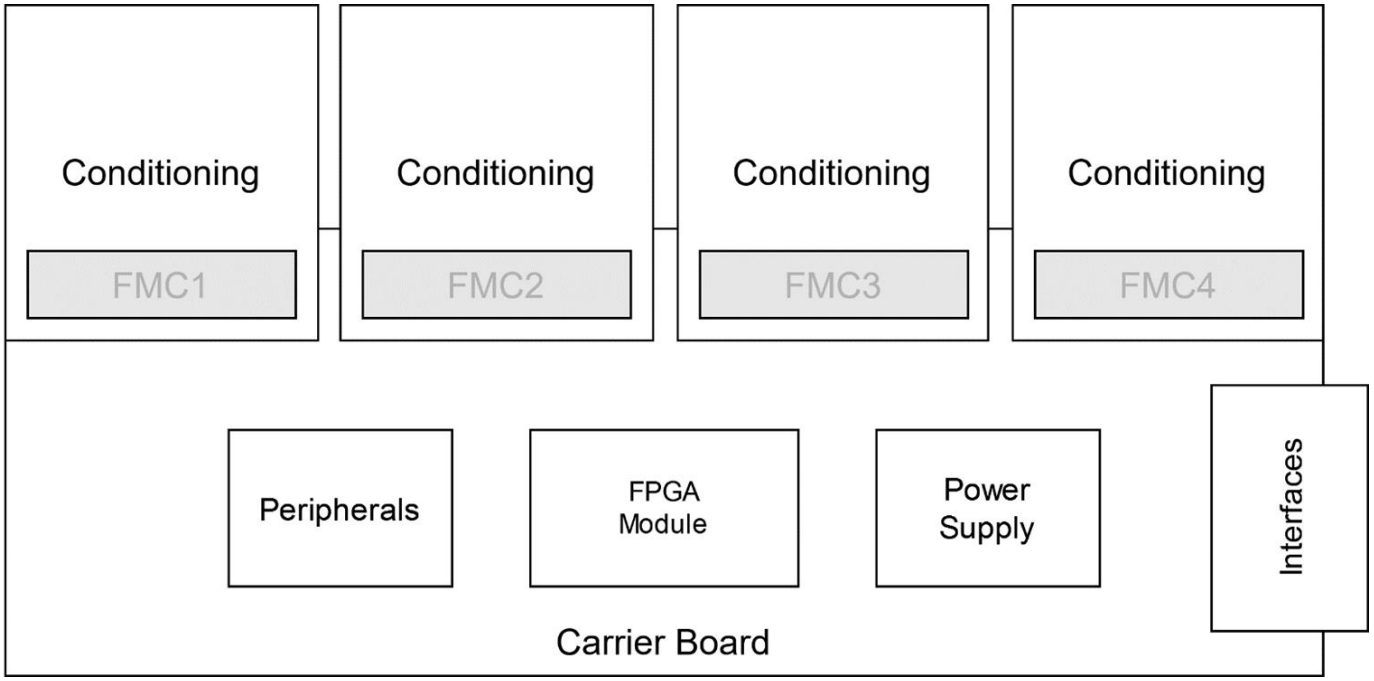
- Xilinx FPGA Module (off-the-shelf, for example Xilinx Kria)
- Custom Carrier Board treated as base for pluggable modules
- Conditioning modules in standardized form factor (for example FMC)
  - Electrical specification kept (limited number of IOs but still more than now)
  - Mechanical Specification treated only as guidelines
  - ADVANTAGE: modules can be tested and developed using any FMC carrier
- Size of the box matches the system
- We keep “patch panel” option

Some Mechanical Details must be clarified before making final proposal

Full scale design plans



Full scale design plans



Summary

- Prototype Version of RFPI Box has been designed and manufactured
- Hardware Layer was tested, all detected problems were solved
- Test FW/SW has been implemented (covered by next presentations)
- General Conclusions move us towards final shape of the system

Thank you !