# Signal Conditioning: Contact Switches sub-module

Bartosz Pękosławski & Paweł Marciniak

# About us

## Bartosz PĘKOSŁAWSKI

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - Projects on machine vibration monitoring – hardware engineer (2006 – 2011)
  - TULCOEMPA – hardware designer (2011 – 2015)
  - SPParTAN – hardware designer (2019 – 2022)
  - FOSREM – hardware designer (2021 – present)

## Paweł MARCINIAK

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - INNOREH – software designer (2017 – 2021)
  - SPParTAN – firmware designer (2019 – 2022)
  - ITER – hardware engineer (2021 – 2022)
  - FOSREM – hardware designer (2021 – present)

# Agenda

- The contact switches module requirements
- The PoC version specification and scope
- The sub-module design details
- Implementation
- Test results discussion
- Full scale design plans
- Summary

# The contact switches sub-module requirements

- The contact switches signals group:

| Signal Name | Peripheral Need | IO Pins per Peripheral | IO Pins Per RFPI | Signal Type | Quantity | I/O | RFPI Response Time | Impedance | Signal Range | Cable Type |
|---|---|---|---|---|---|---|---|---|---|---|
| He Pressure and Level (Cryo) | IO | 1 | 2 | Contact (Switch) | 1 per CRYOMODULE | Input | <10 µs | 100 mΩ (NC) | 12 V, >100 mA excitation | Shielded Twisted Pair |
| Coupler Window Cooling Airflow Permit (Fluid) | IO | 1 | 4 | Contact (Switch) | 1 per cavity/coupler | Input | <1 ms | 100 mΩ (NC) | 5 V, > 10 mA excitation | Shielded Twisted Pair |
| Coupler Vacuum Permit (Vaccum) | IO | 1 | 4 | Contact (Switch) | 1 per cavity/coupler | Input | <10 µs | 100 mΩ (NC) | 5 V, > 10 mA excitation | Shielded Twisted Pair |
| Beam Vacuum Permit (Beam) | IO | 1 | 2 | Contact (Switch) | 1 per CRYOMODULE | Input | <10 µs | 100 mΩ (NC) | 12 V, >100 mA excitation | Shielded Twisted Pair |
| Personal Safety Permit (PS) | IO | 1 | 4 | Contact (Switch) | 1 per cavity/coupler | Input | <1ms | 100 mΩ (NC) | 24 V, >8 mA excitation | Shielded Twisted Pair |

# The PoC version specification and scope

- The contact switches signals group:
  - Cryo (x1), 12 VDC, 100-120 mA
  - Fluid (x2), 12 VDC, 40-43 mA
  - Vacuum (x2), 12 VDC, 40-43 mA
  - Beam (x1), 12VDC, 100-120 mA
  - PS (x2), 24 VDC, 8.5 mA

- Cable diagnostics (detection of short-circuits and open-circuits)
- Possible interconection with slave board (common power supply) with additional input channels
- Hardware configurable CS type (NO or NC) for each channel
- Maskable each CS input
- Fault signal latched at every input (common RESET signal controlled by SPI)

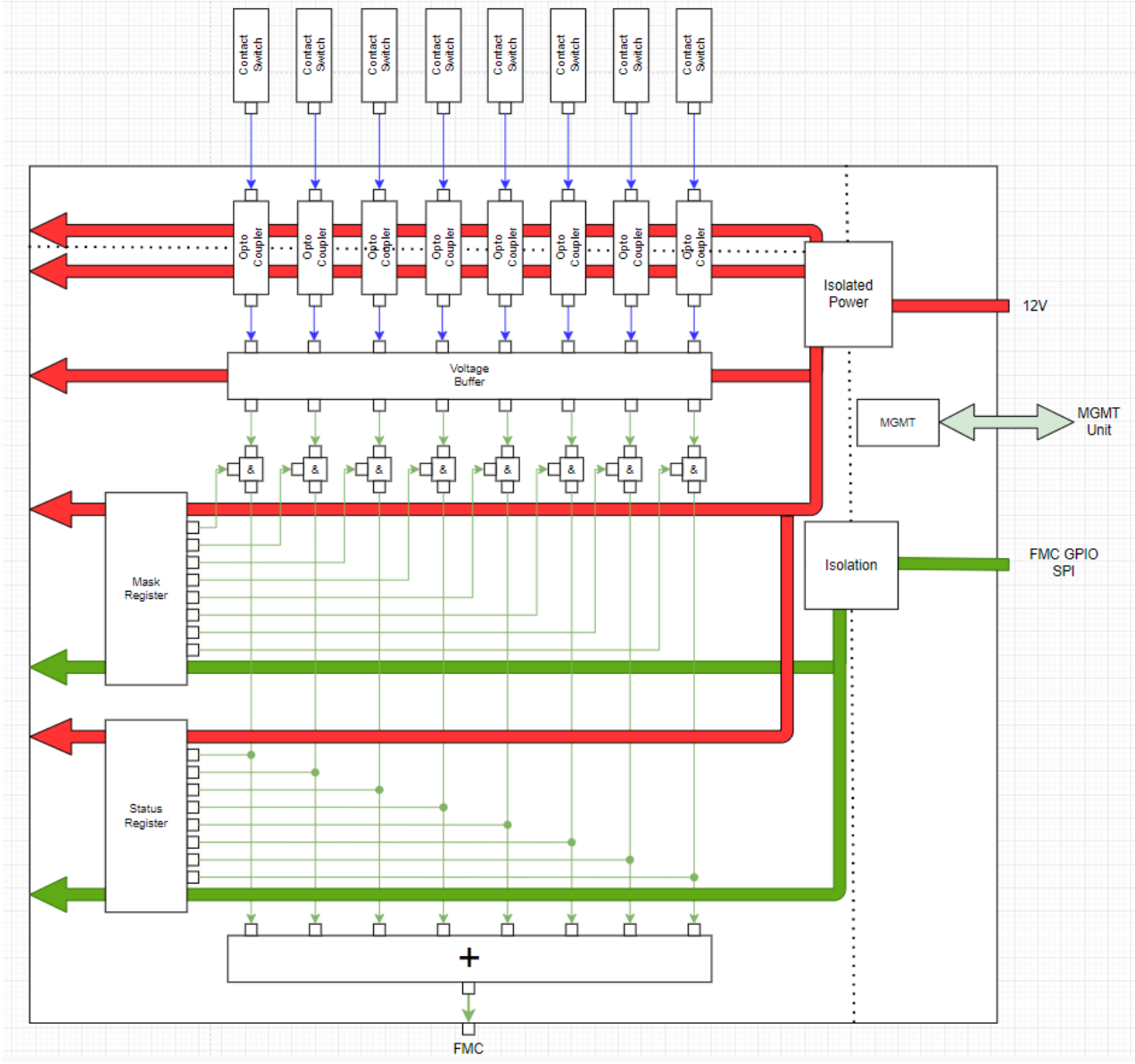
# The PoC version specification and scope

Management Block:

- I²C communication with Raspberry PI
- Current measurement
- Temperature and humidity measurements

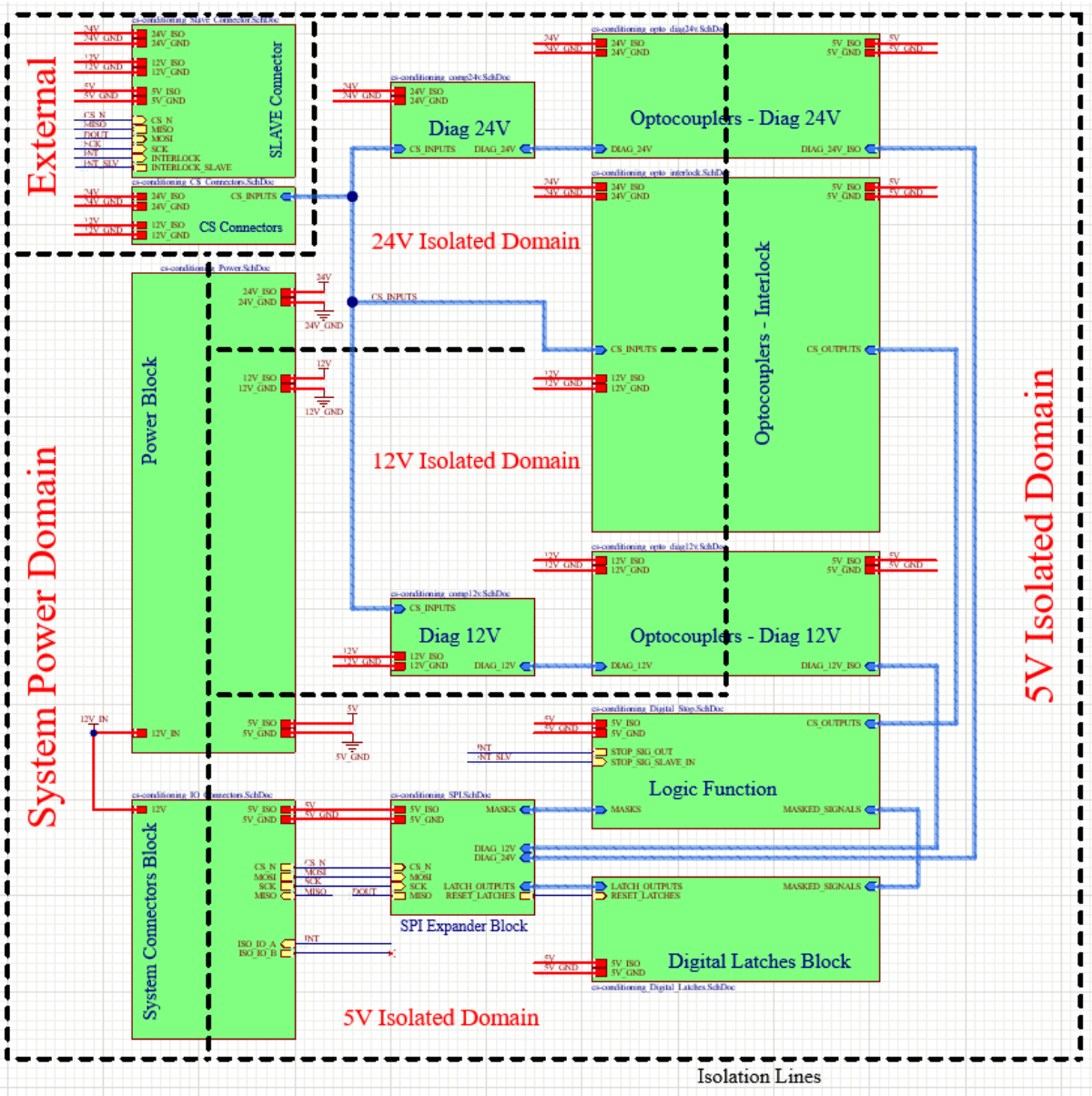

# The sub-module design details

## Conceptual diagram



# The sub-module design details

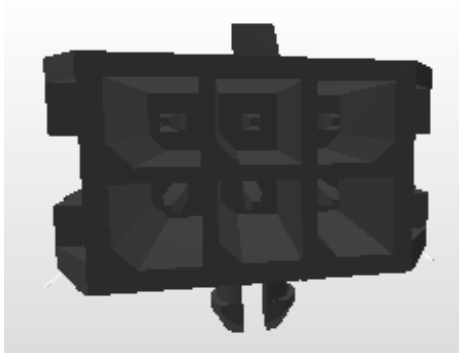
Block diagram



# The sub-module design details

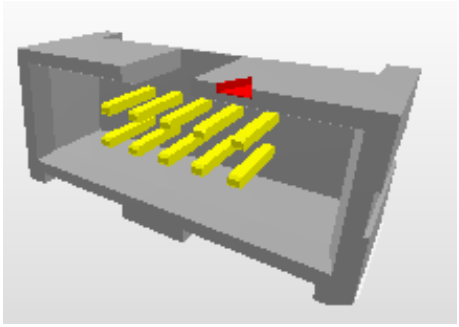
## System Connectors Block

- Power Connector (12 V)



- MGMT Connector ($I^2C$) and sensors

- FMC GPIO Connector (SPI)

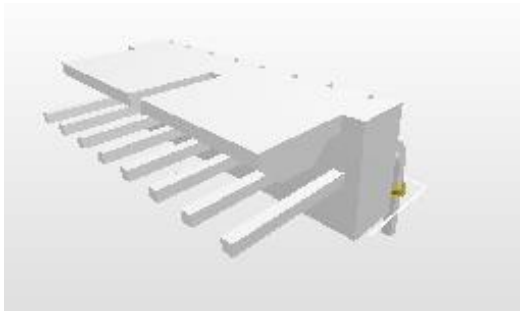


- Isolation of GPIO and SPI signals based on MAX22245BAWA+ and MAX22246CAWA+ digital isolators (2 channels, 7 ns delay, up to 25 / 200 Mbps, 868 $V_{RMS}$ continous / 5 $kV_{RMS}$ 60s / 12.8 $kV_{RMS}$ surge galvanic isolation)

# The sub-module design details

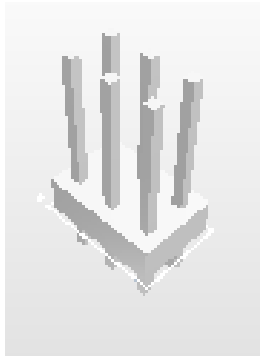
## CS Connectors

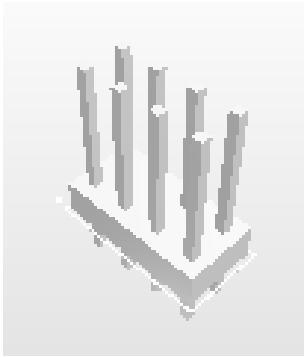
- Two 8-pin connectors (universal) for interconnecting with front panel connectors



## Slave Connectors

- Three connectors for interconnecting with slave board





# The sub-module design details

## Power Block

- 12V → 5V SMPC module Traco Power TRS 2-1211 (isolated, 9-18 V input, max. 2 W output power, 80% efficiency, 1.6 kV isolation)
- 12V → 12V SMPC module Traco Power TEN 30-1212 (isolated, 9-18 V input, max. 30 W output power, 89% efficiency, 1.6 kV isolation)
- 12V → 24V SMPC module Traco Power TRS 2-1215 (isolated, 9-18 V input, max. 2 W output power, 83% efficiency, 1.6 kV isolation)
- EN 55032 class A external filters at the inputs for radiated and conducted emission

# The sub-module design details

## SPI Expander Block

- MAX7301 serial-interfaced I/O expander with 28 configurable (logic input or logic output) ports

## Digital Latches Block

- CD4043 3-state R/S latches (quad, R dominates, minimum pulse width 160 ns)

## Logic Function Block

- 74ACT08 AND gates (quad 2-input, 5.5-8.5 ns propagation delay) for signal and mask
- 74AHCT32 OR gates (quad 2-input, 1-10 ns propagation delay) for masked signals

# The sub-module design details

## Optocouplers – Diagnostics (12 V) Block

- LTV-847S-BC optocoupler (CTR 130-400%, 4 μs typical response time), 9-11 mA LED current, CE output configuration, OC and SC outputs tighed together (single fault signal for each input)

## Optocouplers – Diagnostics (24 V) Block

- LTV-847S-BC optocoupler (CTR 130-400%, 4 μs typical response time), 9-10 mA LED current, CE output configuration, OC and SC outputs tighed together (single fault signal for each input)

## Optocouplers – Interlock Block

- LTV-847S-BC optocoupler (CTR 130-400%, 4 μs typical response time), 9 mA LED current, CE output configuration

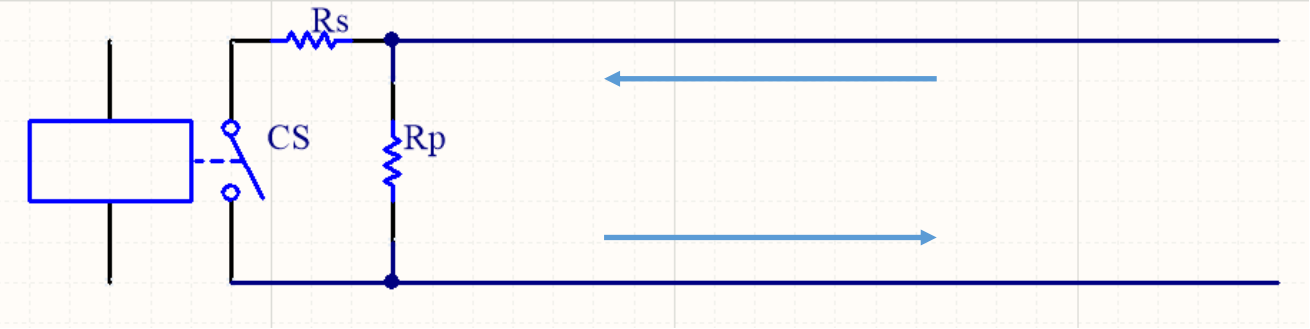
# The sub-module design details

## Diag 12 V Block

- LM2901PT voltage comparators (quad, 2-36 V supply voltage range, open-drain , < 1 μs response) with resistor voltage dividers for reference

## Diag 24 V Block

- LM2901PT voltage comparators (quad, 2-36 V supply voltage range, open-drain, < 1 μs response) with resistor voltage dividers for reference

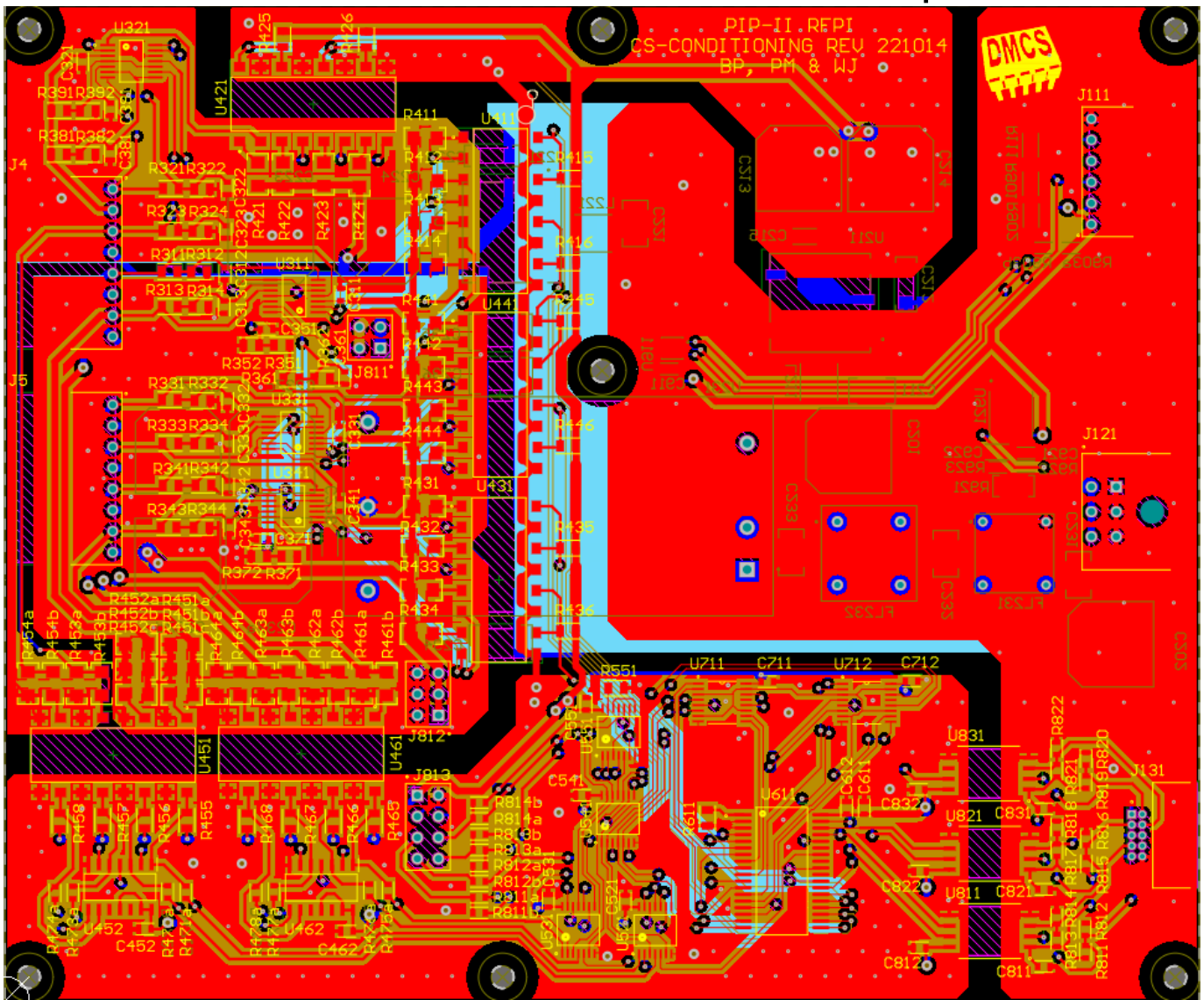


# The sub-module design details

| Signal Name | Cable resistance | Rs | Rp | Rd | Rpd | V (CS closed) | V (CS open) | V (cable shorted) | V (cable open) |
|---|---|---|---|---|---|---|---|---|---|
| Cryo, Beam | 0 | 5 | 1000 | 750 | 75 | 8.2 | 0.77 | 12 | 0 |
| | 18 | | | | | 6.9 | 0.75 | 10.2 | 0 |
| Vacuum, Fluid | 0 | 47 | 3300 | 1000 | 300 | 10.0 | 0.78 | 12 | 0 |
| | 18 | | | | | 9.4 | 0.78 | 11.3 | 0 |
| PS | 0 | 470 | 22000 | 2200 | 976000 | 19.8 | 2.18 | 24 | 0 |
| | 18 | | | | | 19.7 | 2.17 | 23.8 | 0 |

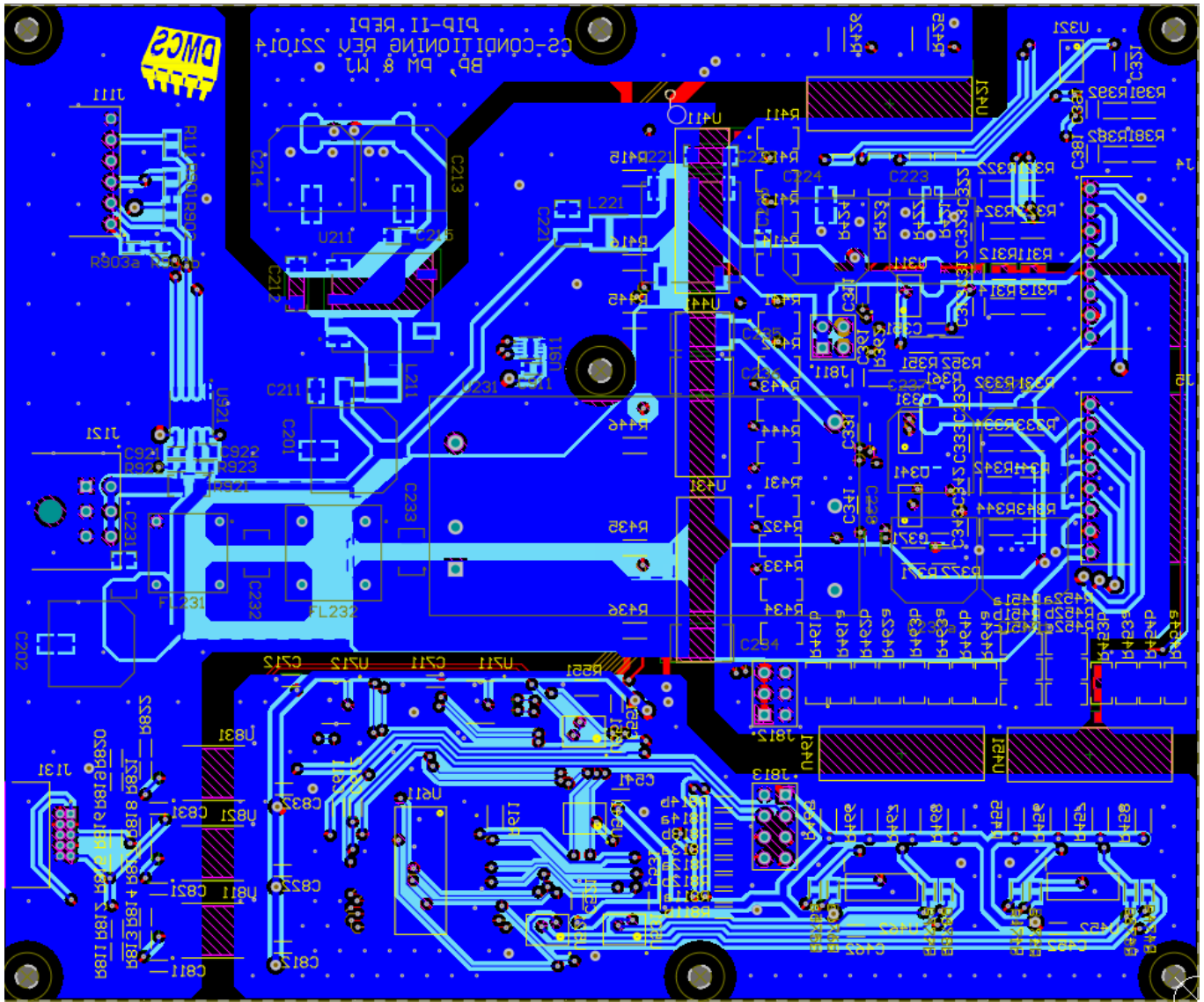
# Implementation

4-layer PCB, dimensions: 144 mm x 120 mm – top



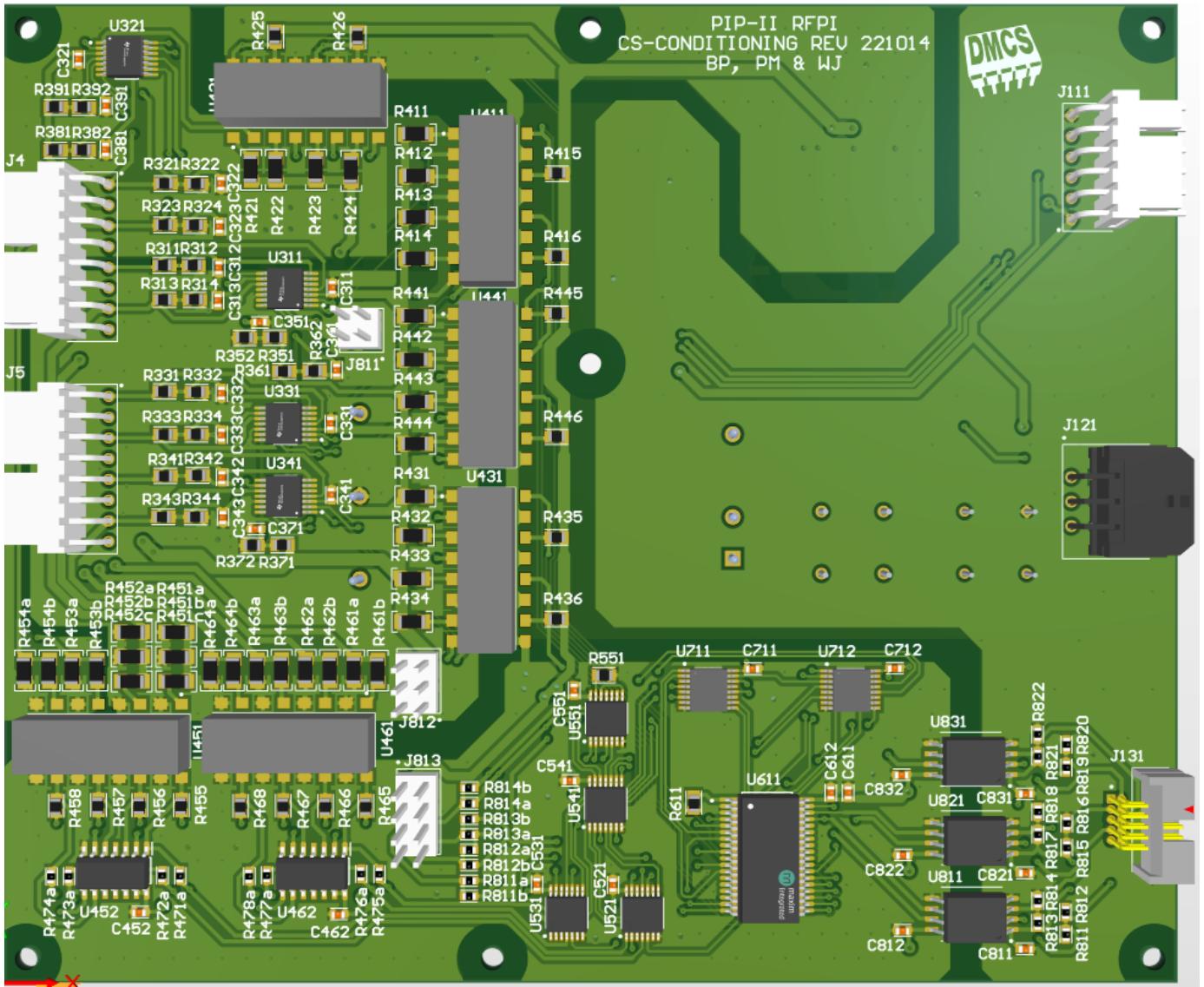
# Implementation

4-layer PCB, dimensions: 144 mm x 120 mm – bottom



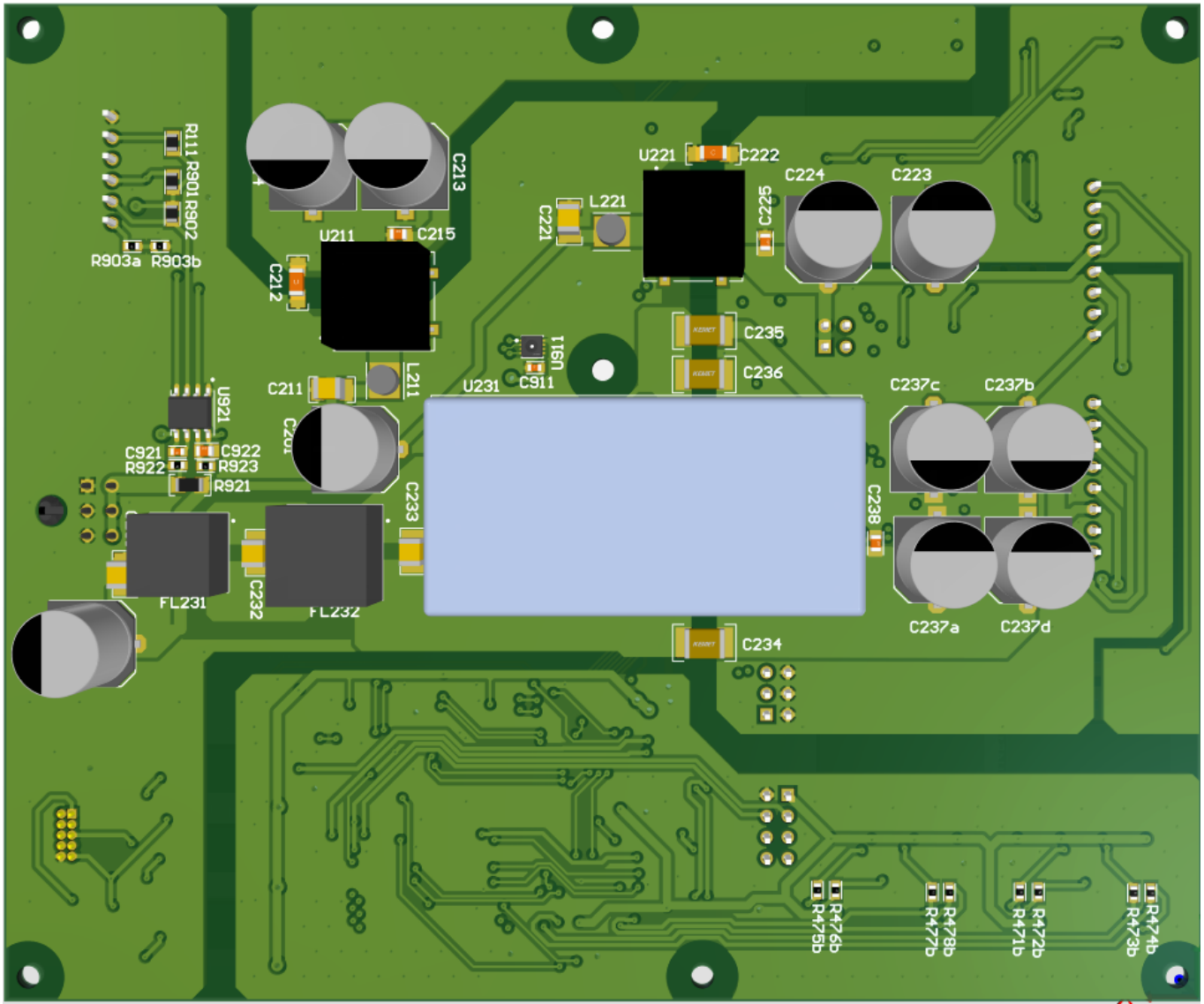
# Implementation

## 3D model – top



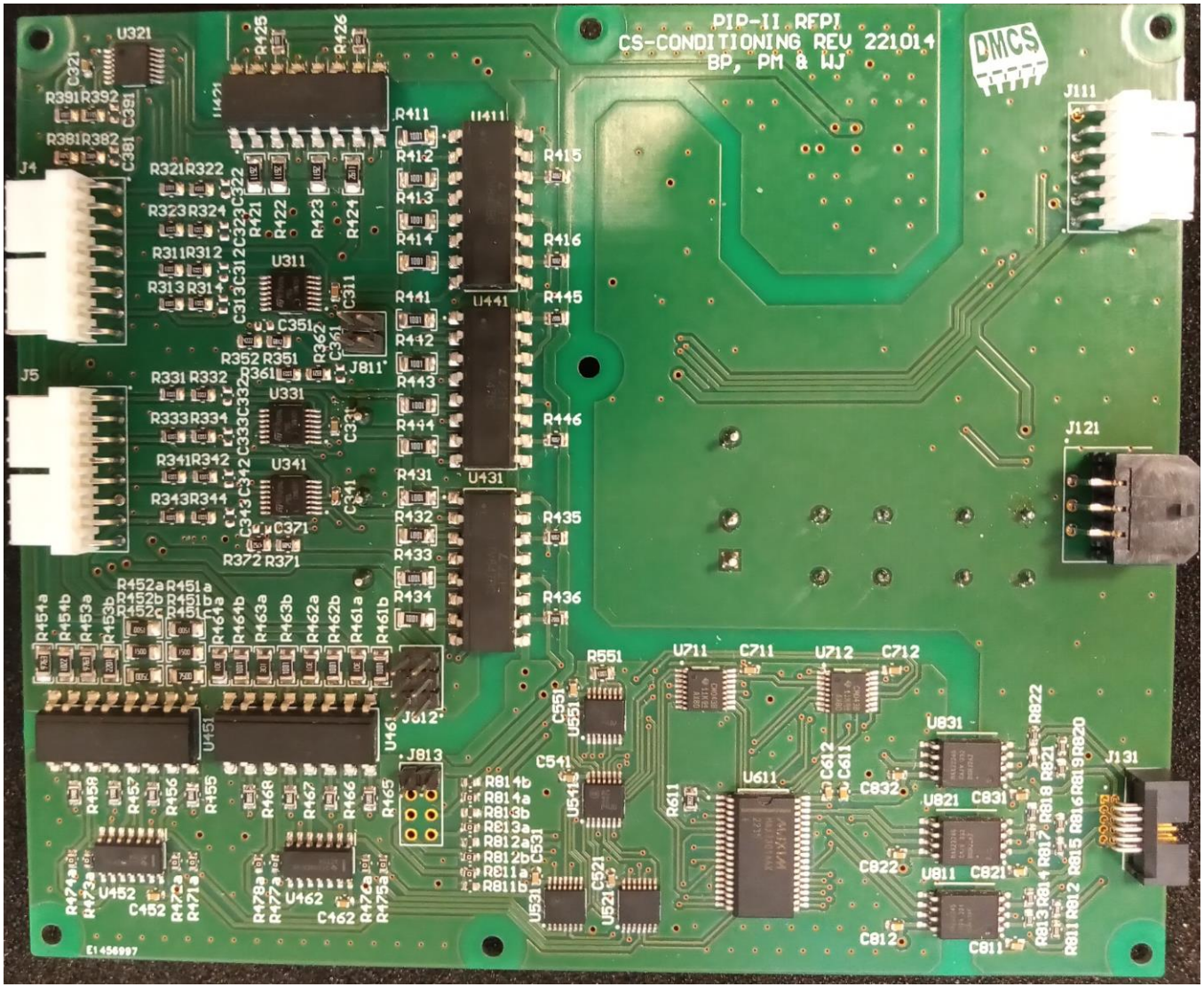
# Implementation

## 3D model bottom



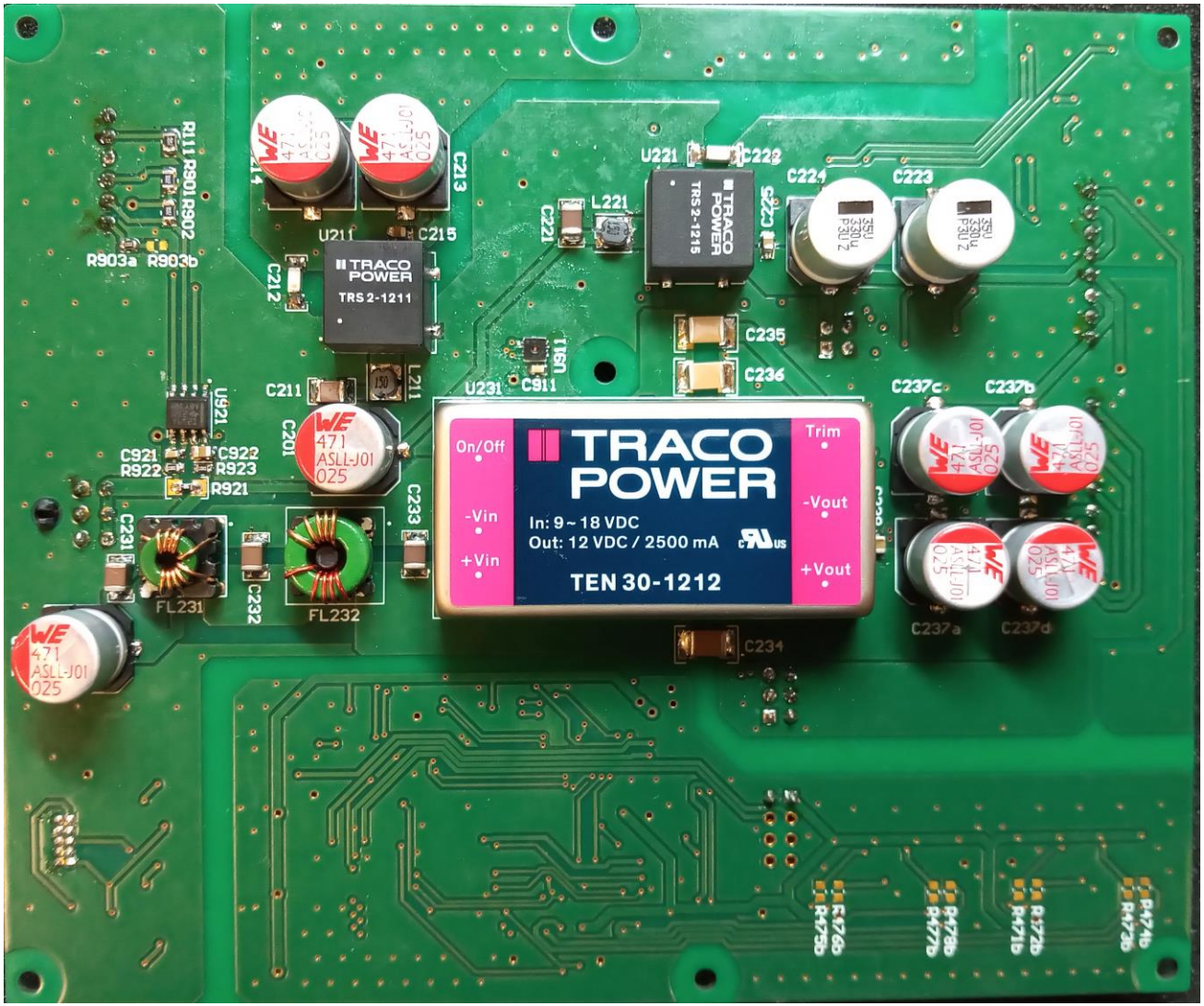
# Implementation

## Real view - top



# Implementation

## Real view - bottom

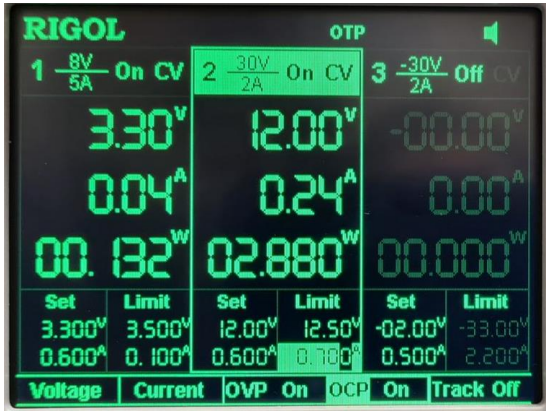


# Test results discussion

- Detection of soldering faults (partially manual soldering)
  - Short circuits
  - Damaged tracks
  - Missing or broken connections
- Operation of the power supply block (correct voltage levels)
- Operation of the main logic (delay between closing CS and interlock output signal)
- Cable diagnostics operation
- $I^2C$ communication with temperature and supply current sensors

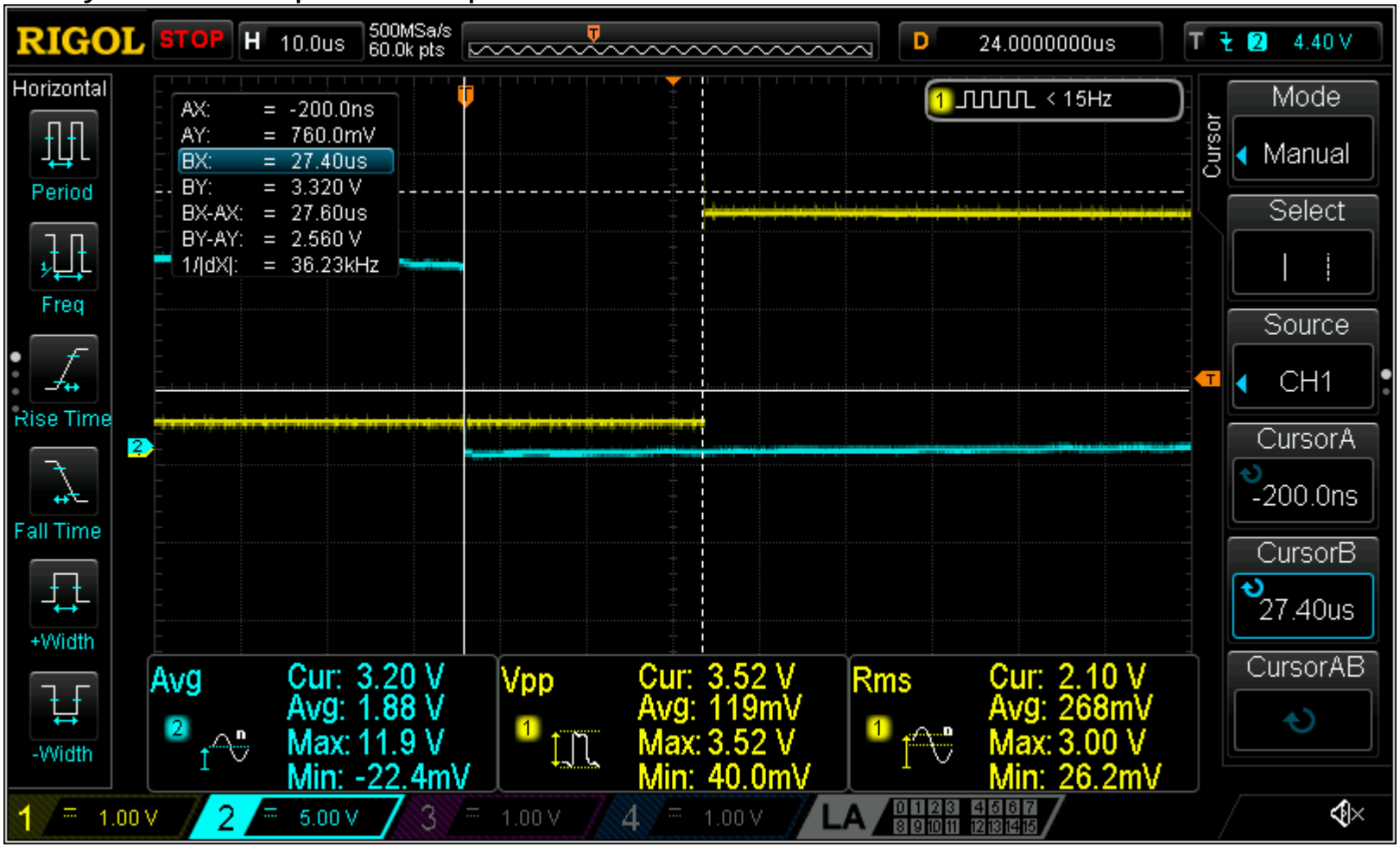
# Test results discussion

- **Detection of soldering faults, e.g. short circuits, damaged tracks, missing or broken connections**
  - No errors were detected on the basis of the vision analysis.
- **Operation of the main power block (correct voltage levels)**
  - The power block works properly
  - Current consumptions are as expected (aprox. 40 mA for 3.3 V voltage domain, and 0.9 A for 12 V voltage domain when fully loaded (all inputs closed))




# Test results discussion

- Operation of the main logic (delay between closing CS and interlock output signal) – delays from 11.0 μs to 27.6 μs



# Test results discussion

- **Cable diagnostics operation**

Correct operation of diagnostics comparators
(except for OC diagnostics for 24 V domain → interchanged comparator inputs by mistake)

Wrong output signal of optocouplers
(~OC NAND ~SC logics needed instead of ~OC NOR ~SC → output phototransistors need to be connected in series instead of paralel connection)

# Test results discussion

- **I²C communication with temperature and supply current sensors**
  - As part of the tests, the correctness of I²C communication with two sensors was checked:
    - STH31 - Connection with the temperature sensor was established and correct temperature was read.
    - INA219 – Connection with the sensor was established.

# Full scale design plans

- The presented solution can be partially adopted in the final design
- Minimization of the delay between input and output is needed in the final design
- 8 redundant channels are needed in the final design

- Changes in schematic diagrams (duplication of some blocks; replacement of some optocouplers or adjusting their loads)
- PCB project redesign

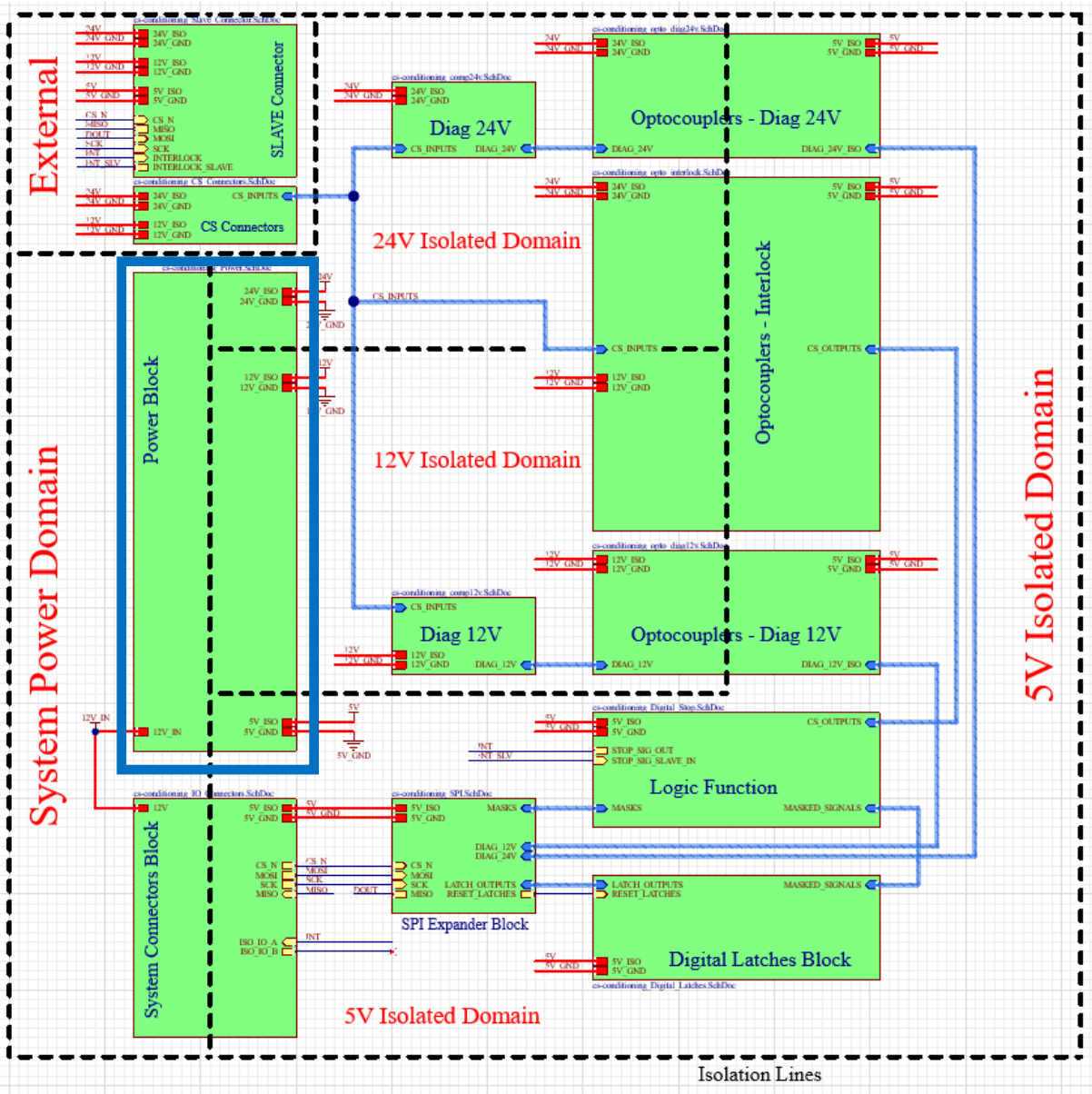
# Summary

- Requirements
  - 8 channels per module
  - Response time less then 1 µs
- PoC, implementation and verification
  - PCB supporting 8 channels and additional slave board with 8 channels
  - Cable diagnostics function
  - 4-layer PCB with hardware configurable CS type (NO or NC) and CS presence
  - Correct operation of the main power block
  - Operation of cable diagnostics function to be easily repaired
  - Correct but too slow interlock logic function
- Full scale design plans
  - Extending the solution to 16 channels (master and slave board or a single PCB)

# Thank You

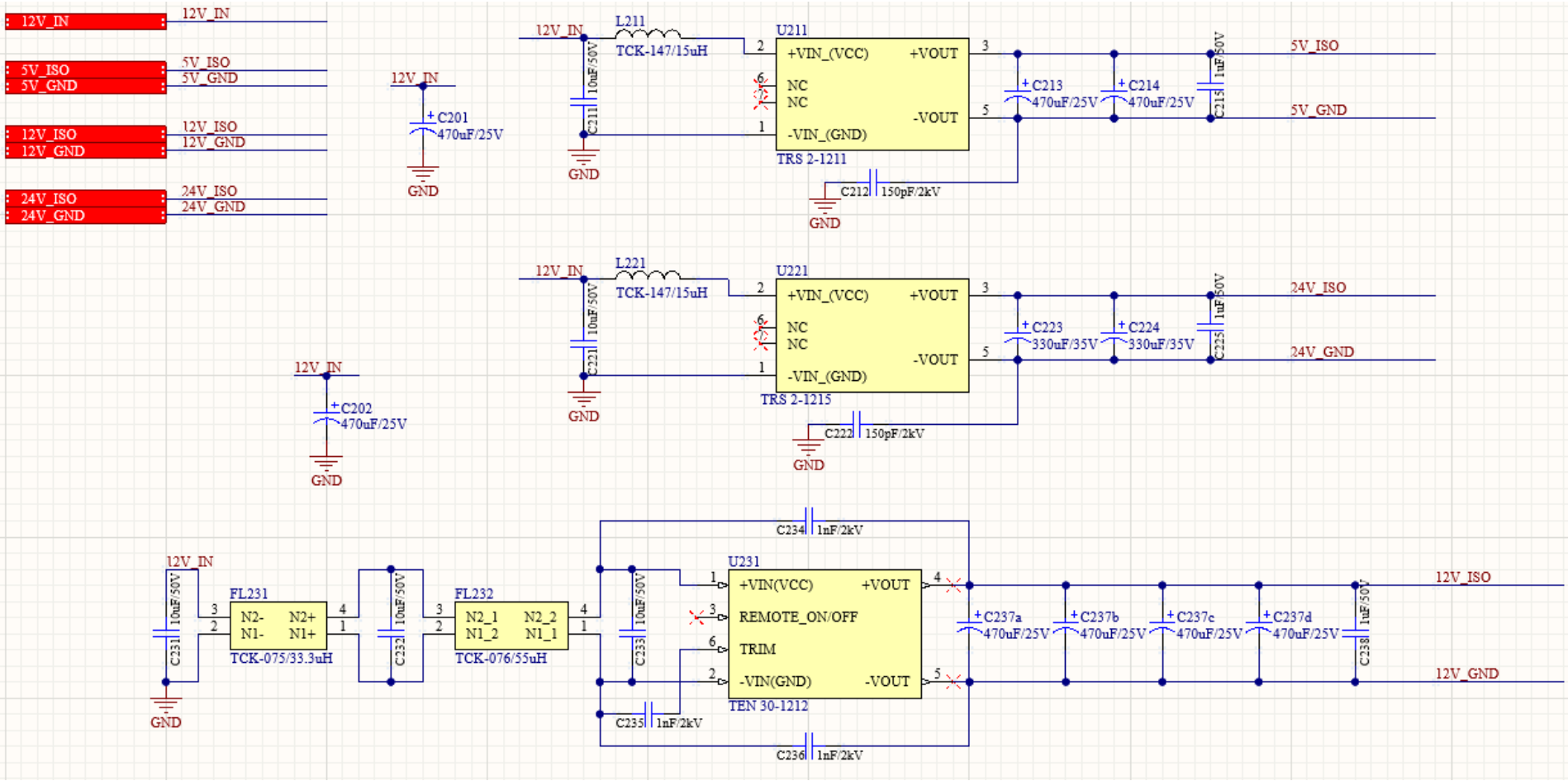
# The sub-module design details

- Power Block



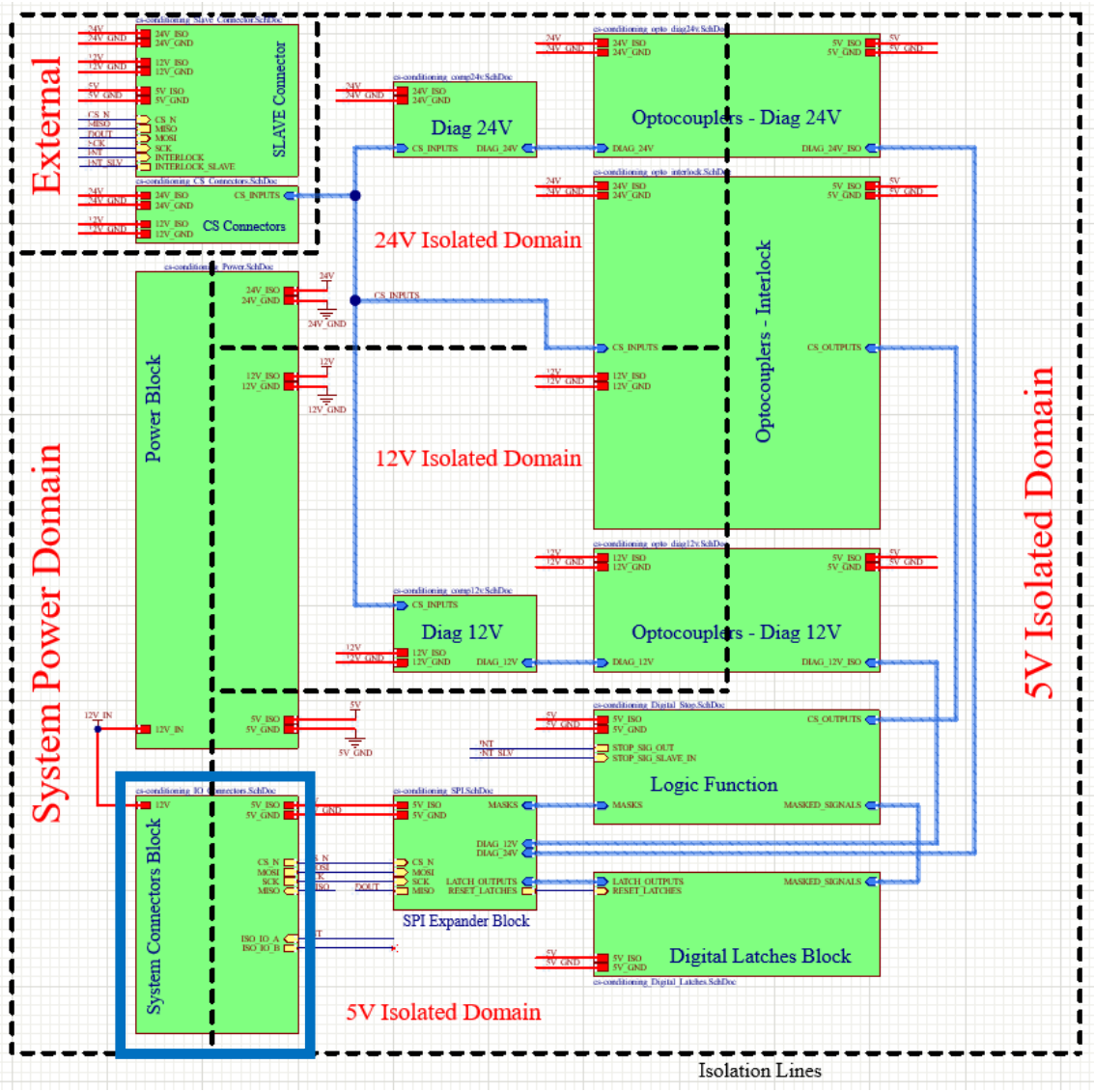
# The sub-module design details

- Power Block



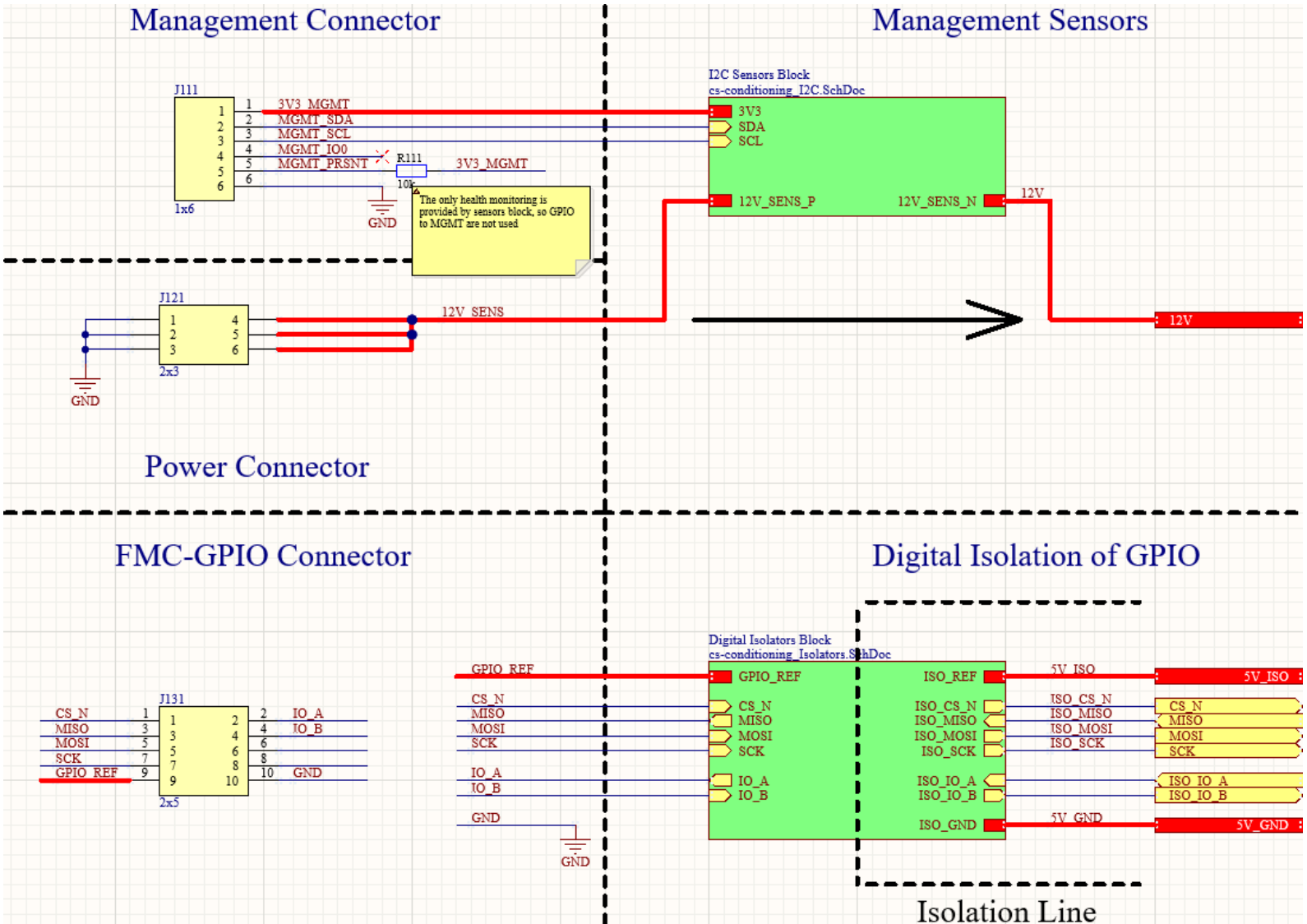
# The sub-module design details

- System Connectors Block



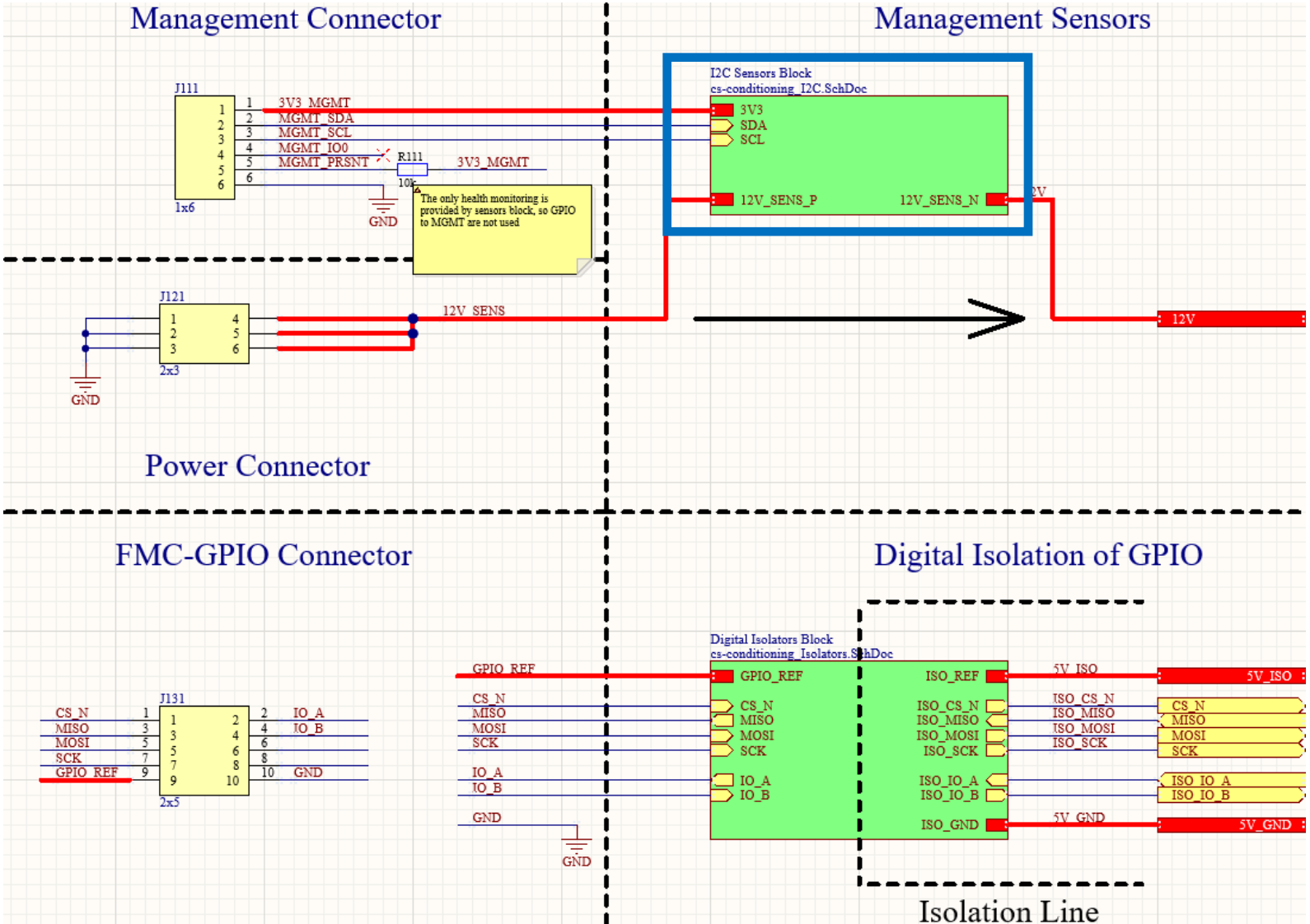
# The sub-module design details

- System Connectors Block



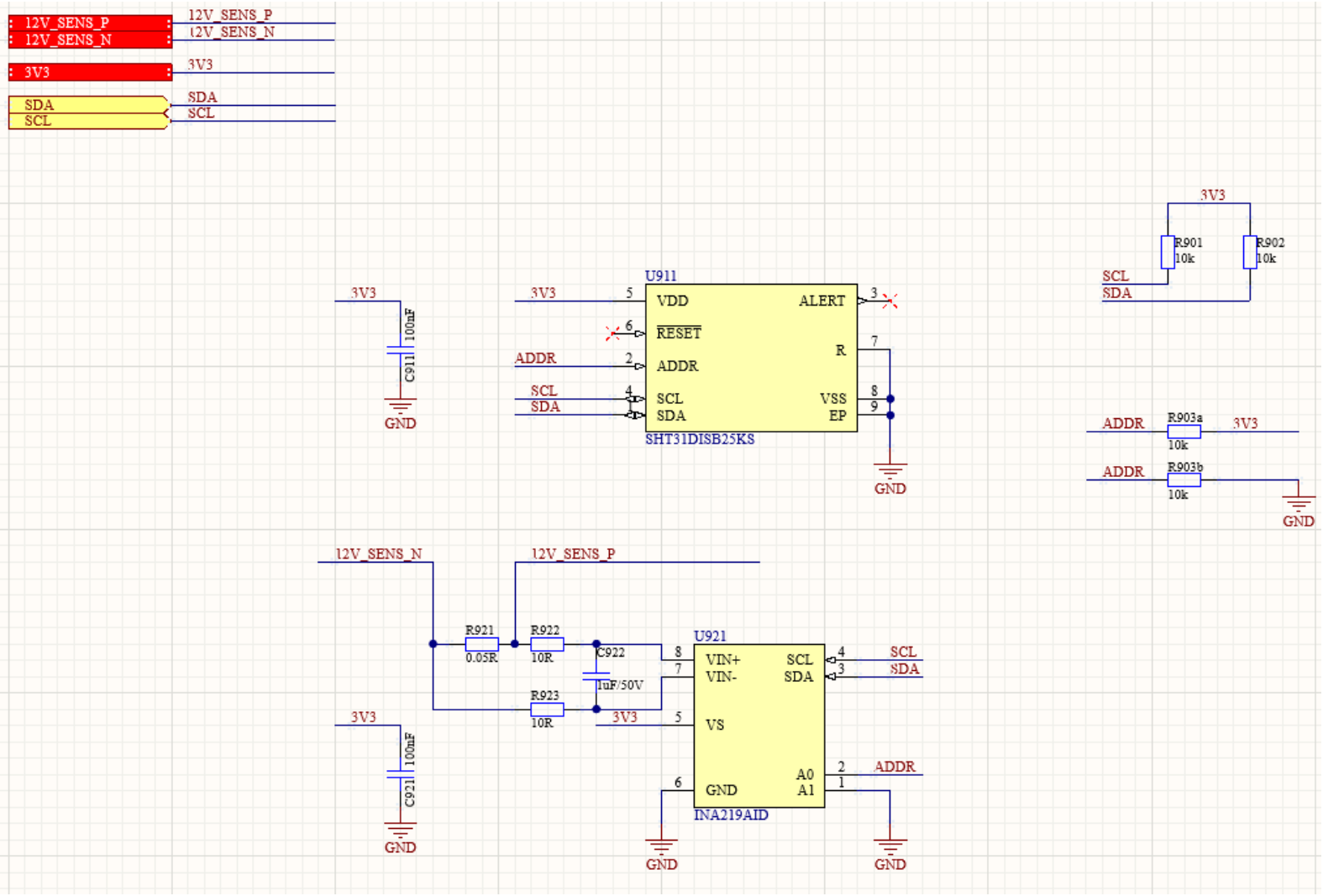
# The sub-module design details

## Management Sensors



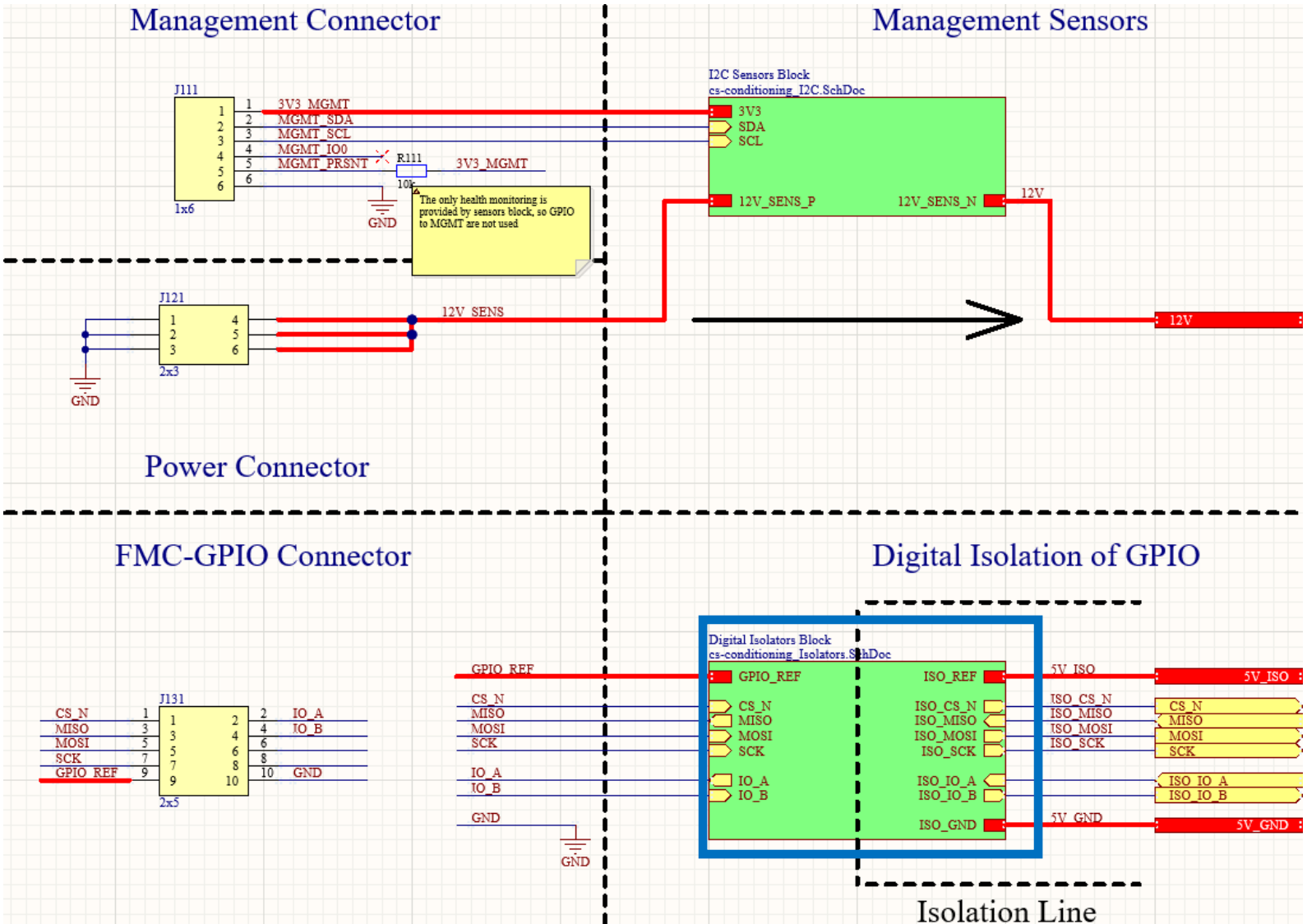
# The sub-module design details

## Management Sensors Schematic Diagram



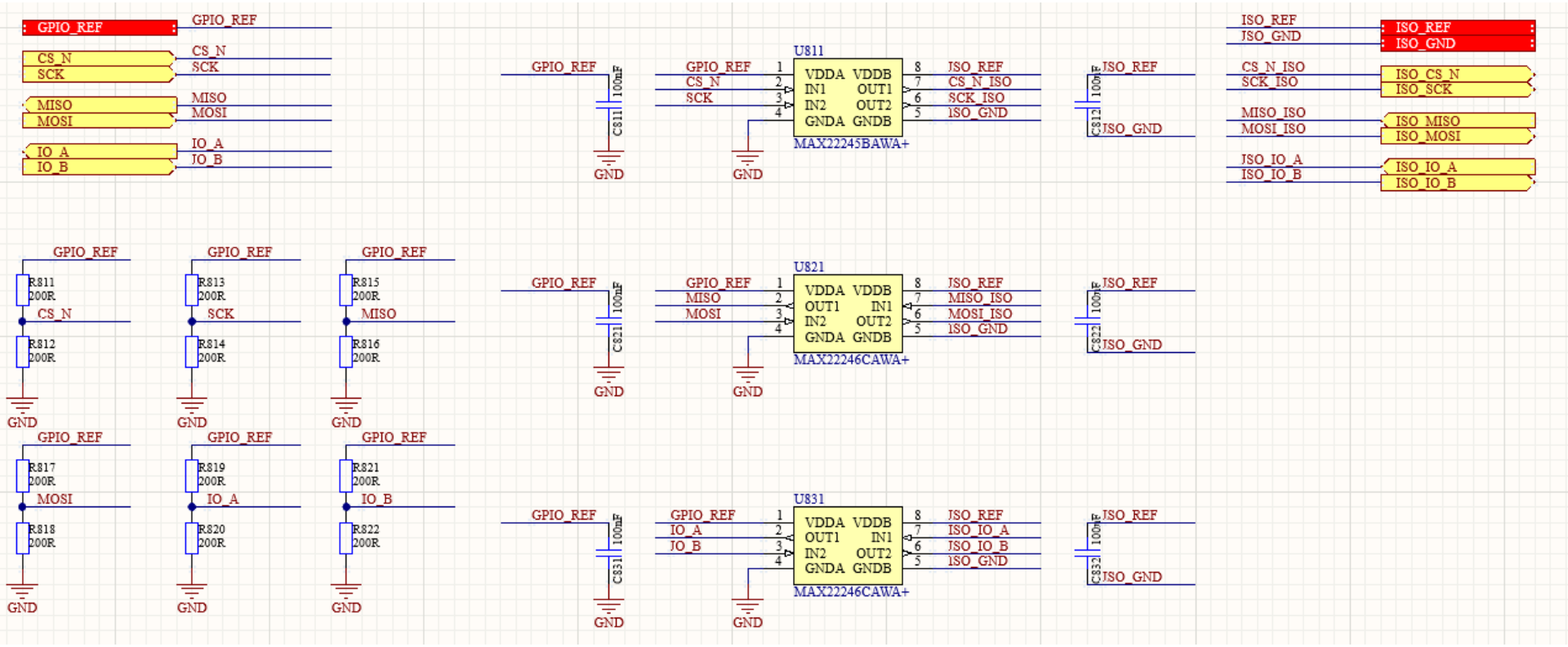
# The sub-module design details

## Digital Isolation of GPIO



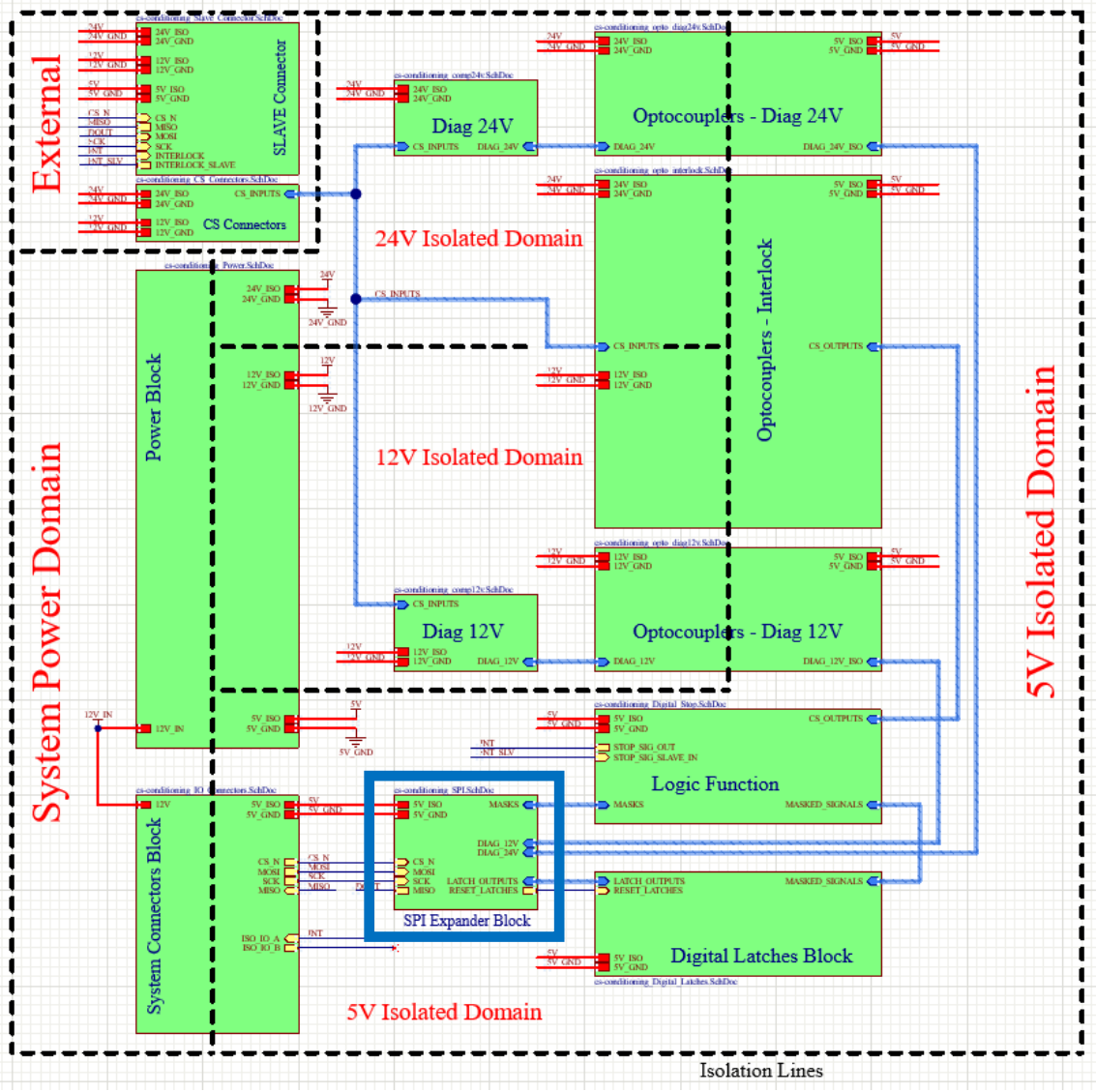
# The sub-module design details

## Digital Isolation of GPIO Schematic Diagram



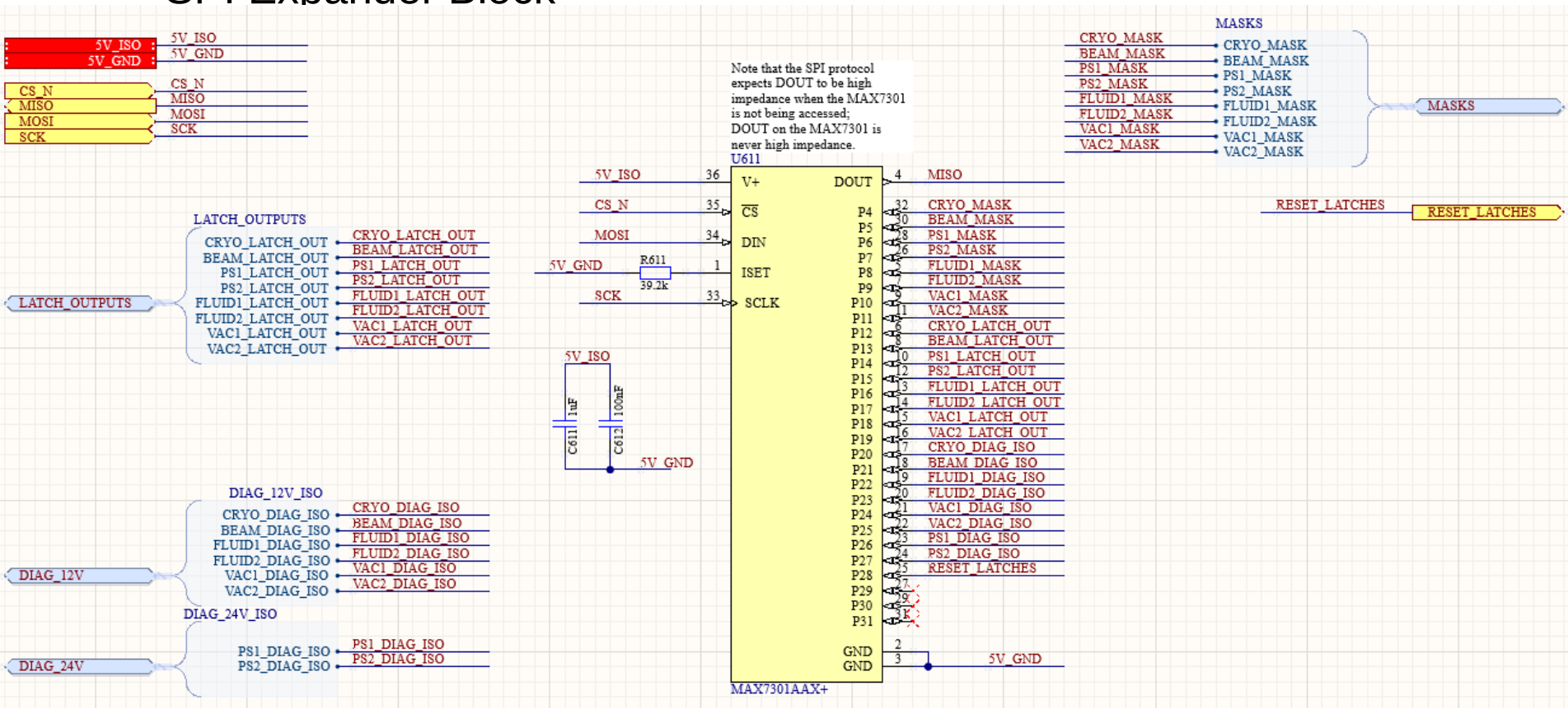
# The sub-module design details

- SPI Expander Block



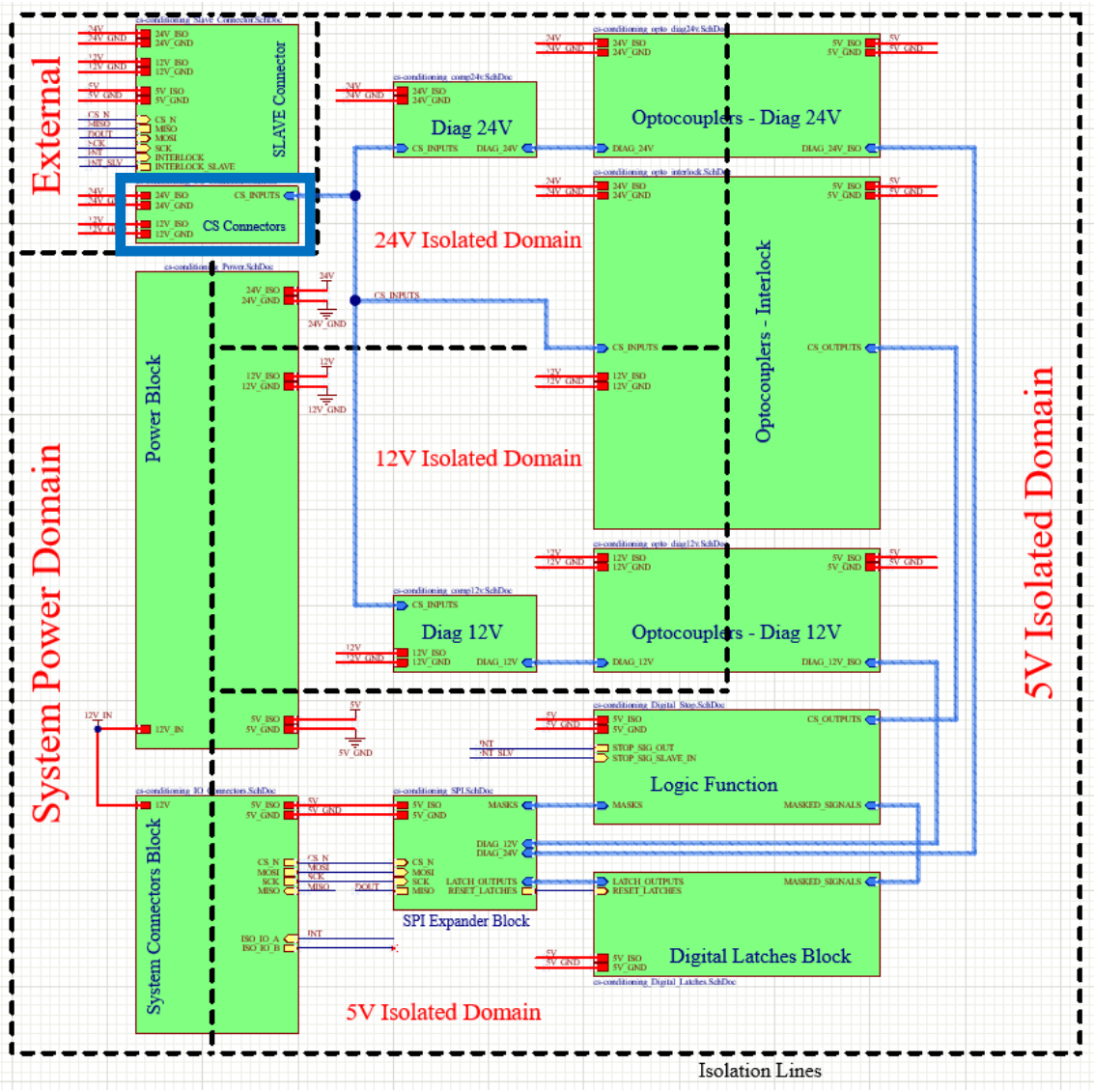
# The sub-module design details

- SPI Expander Block



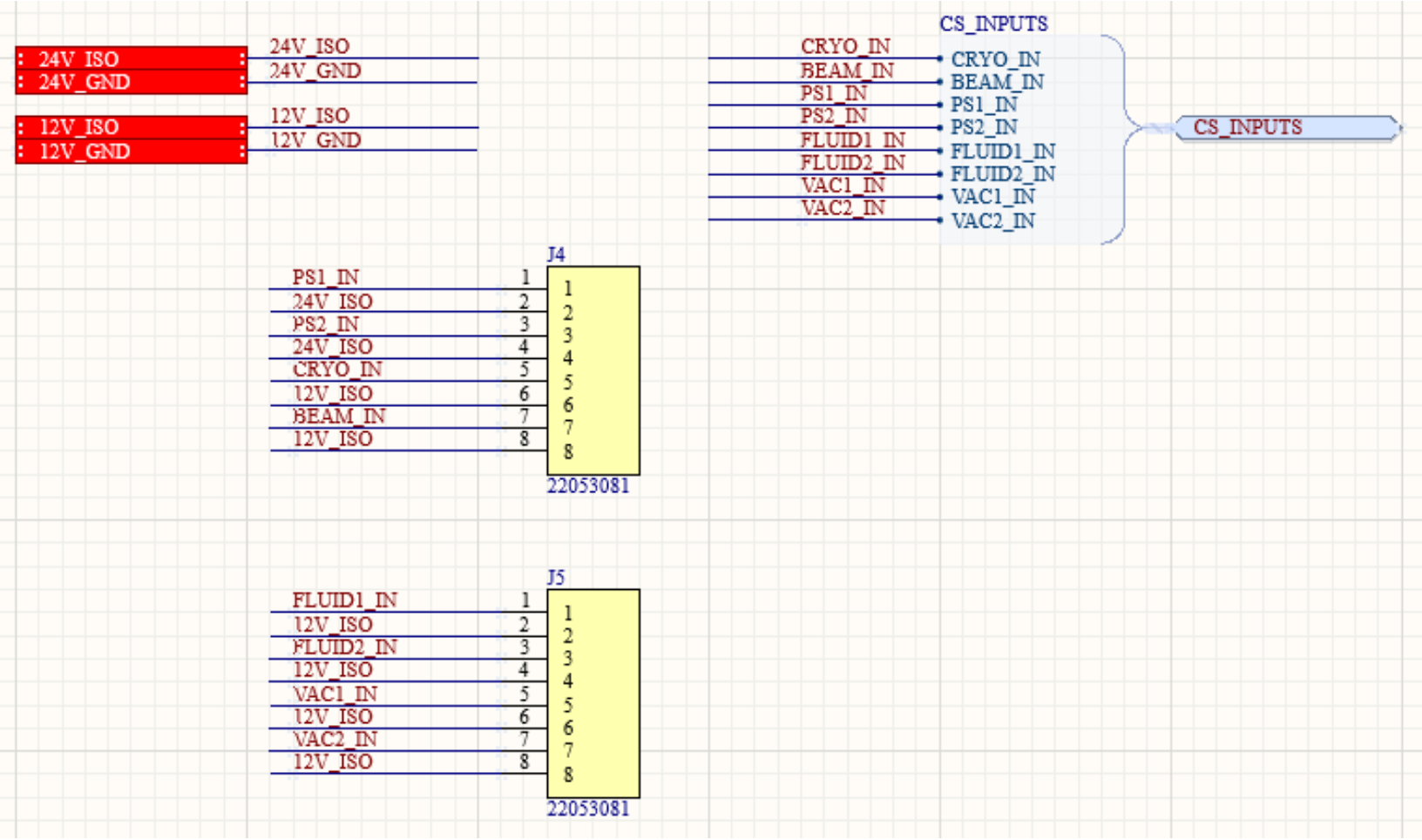
# The sub-module design details

- CS Connectors Block



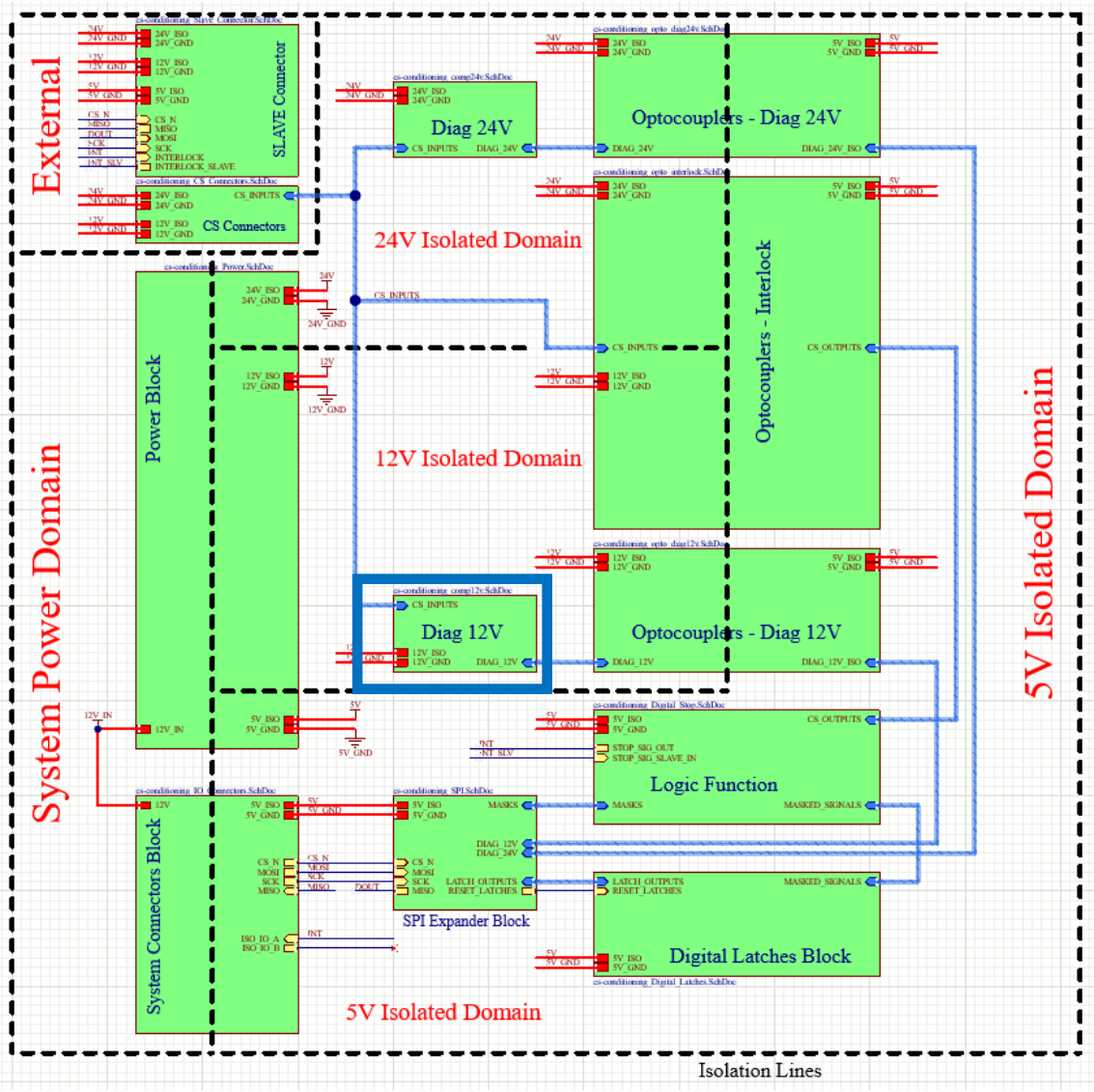
# The sub-module design details

- CS Connectors Block



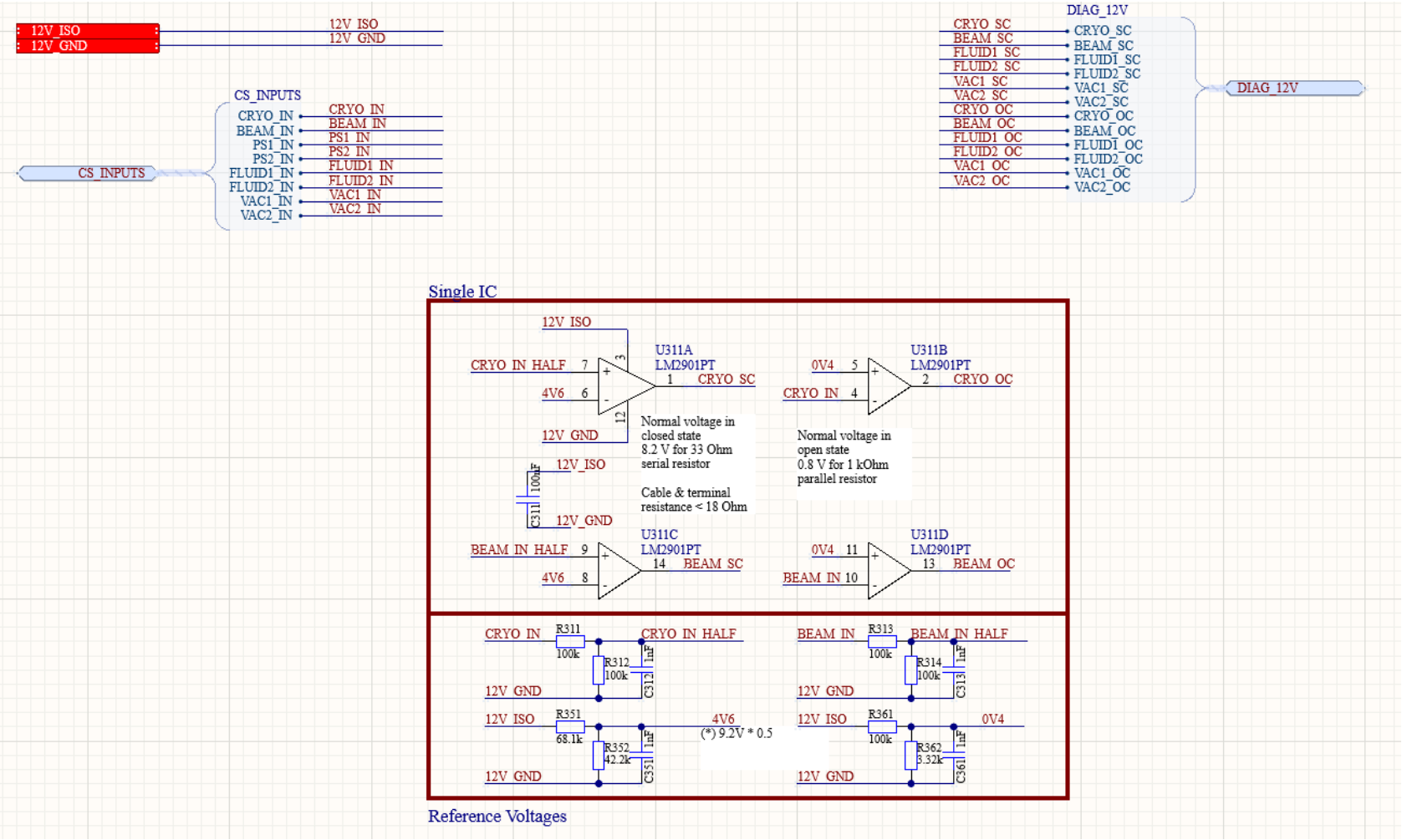
# The sub-module design details

- Diag 12V Block



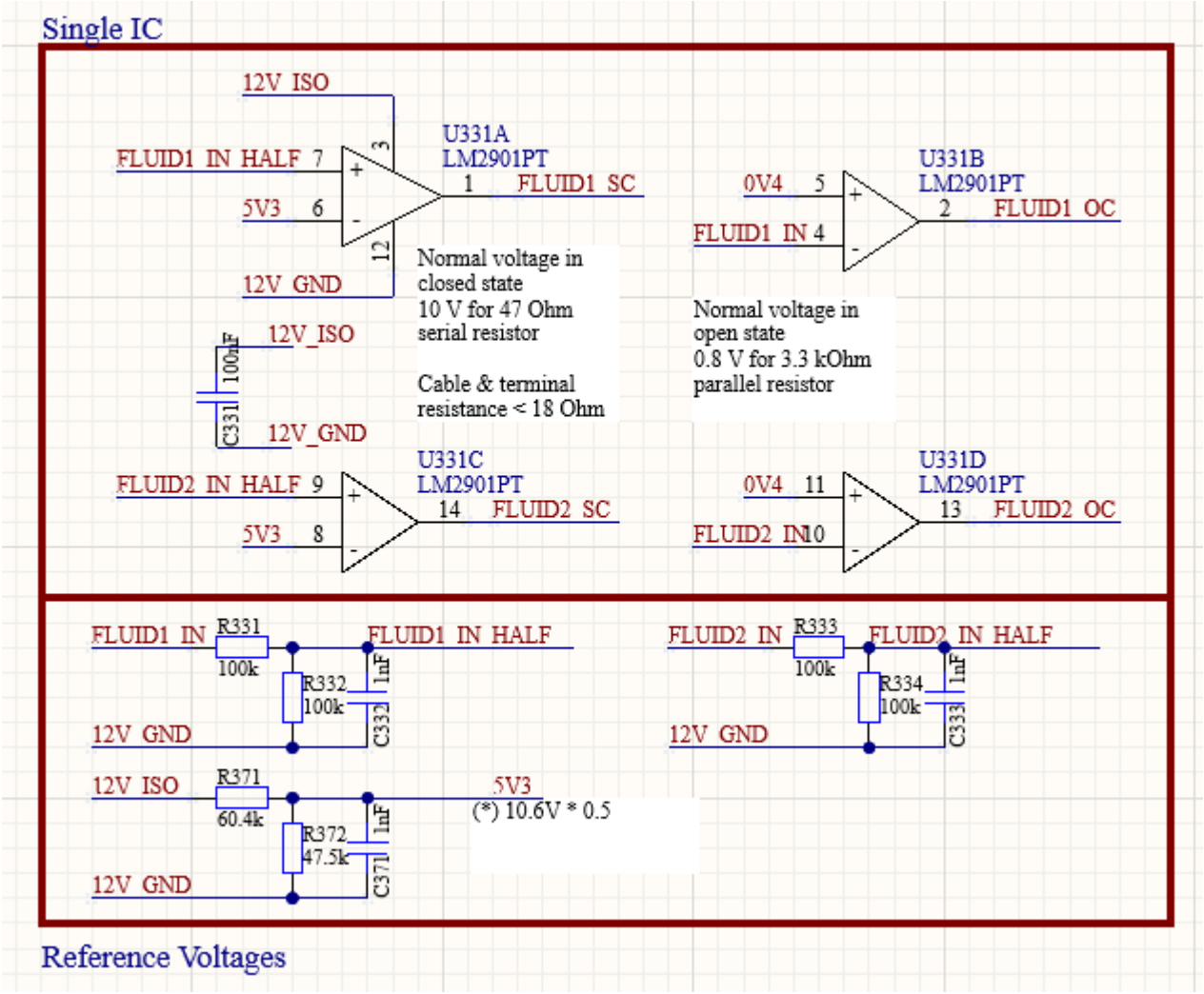
# The sub-module design details

- Diag 12V Block – CRYO and BEAM input signals



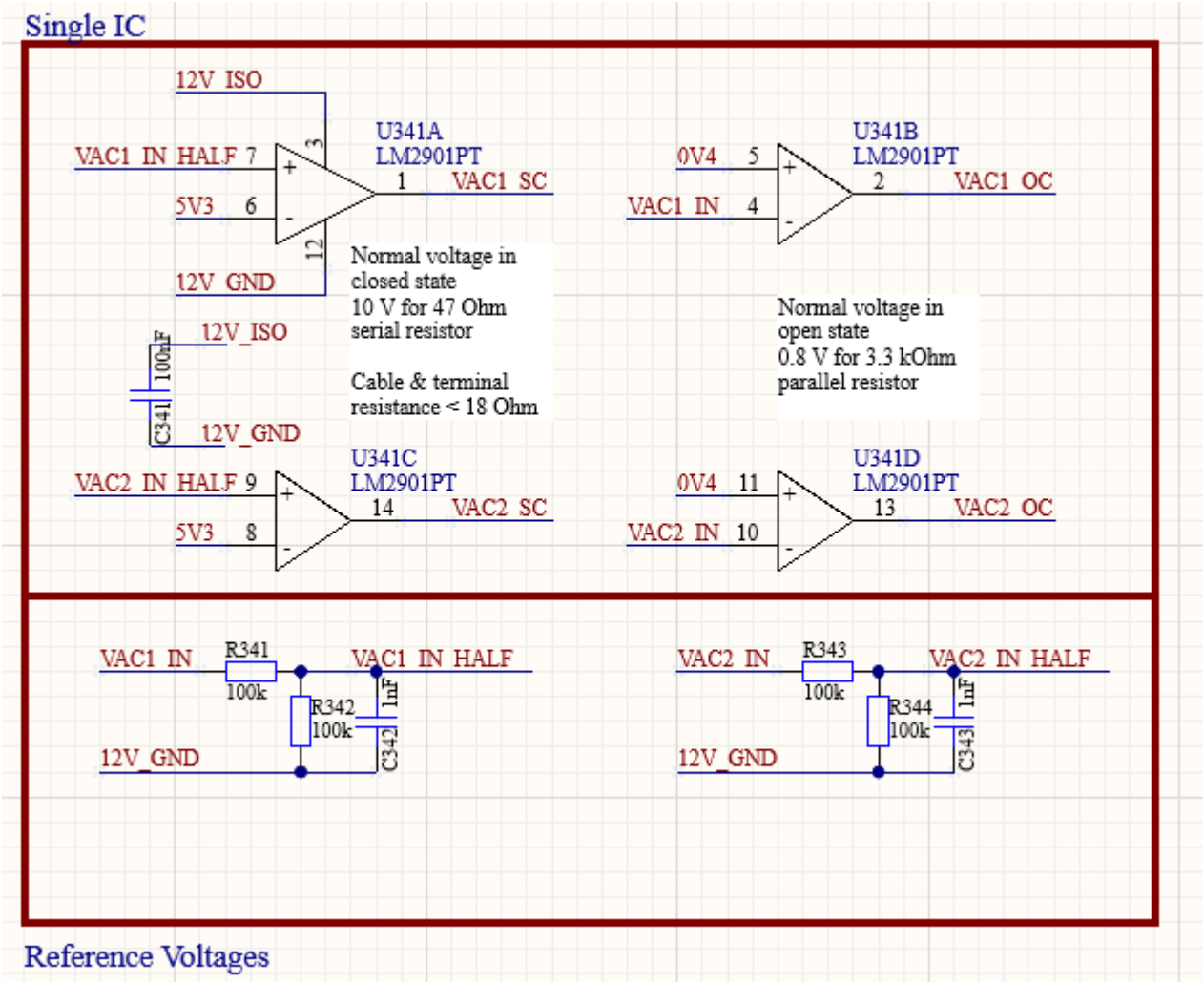
# The sub-module design details

- Diag 12V Block – FLUID input signal



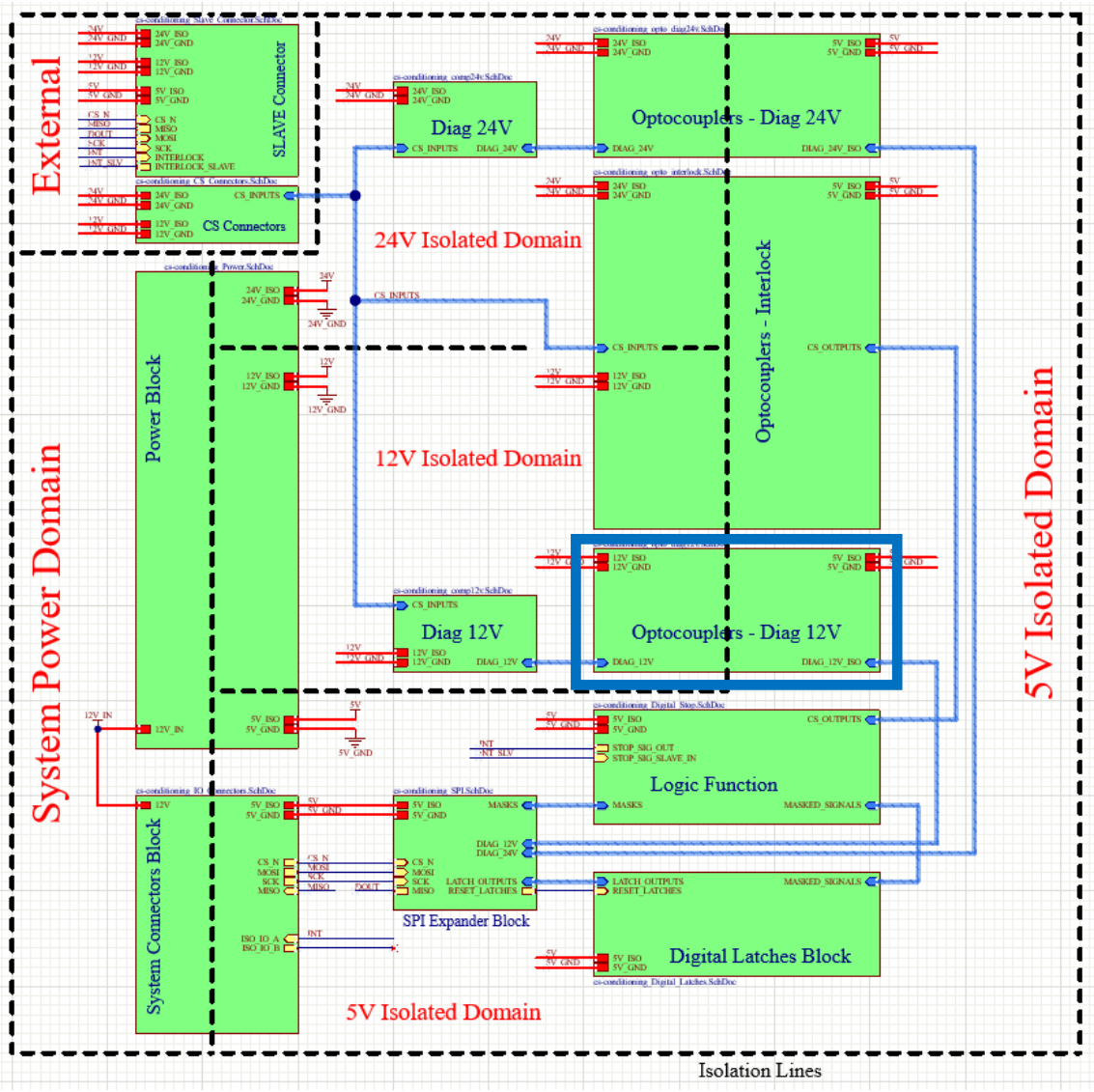
# The sub-module design details

- Diag 12V Block – Vacuum input signal



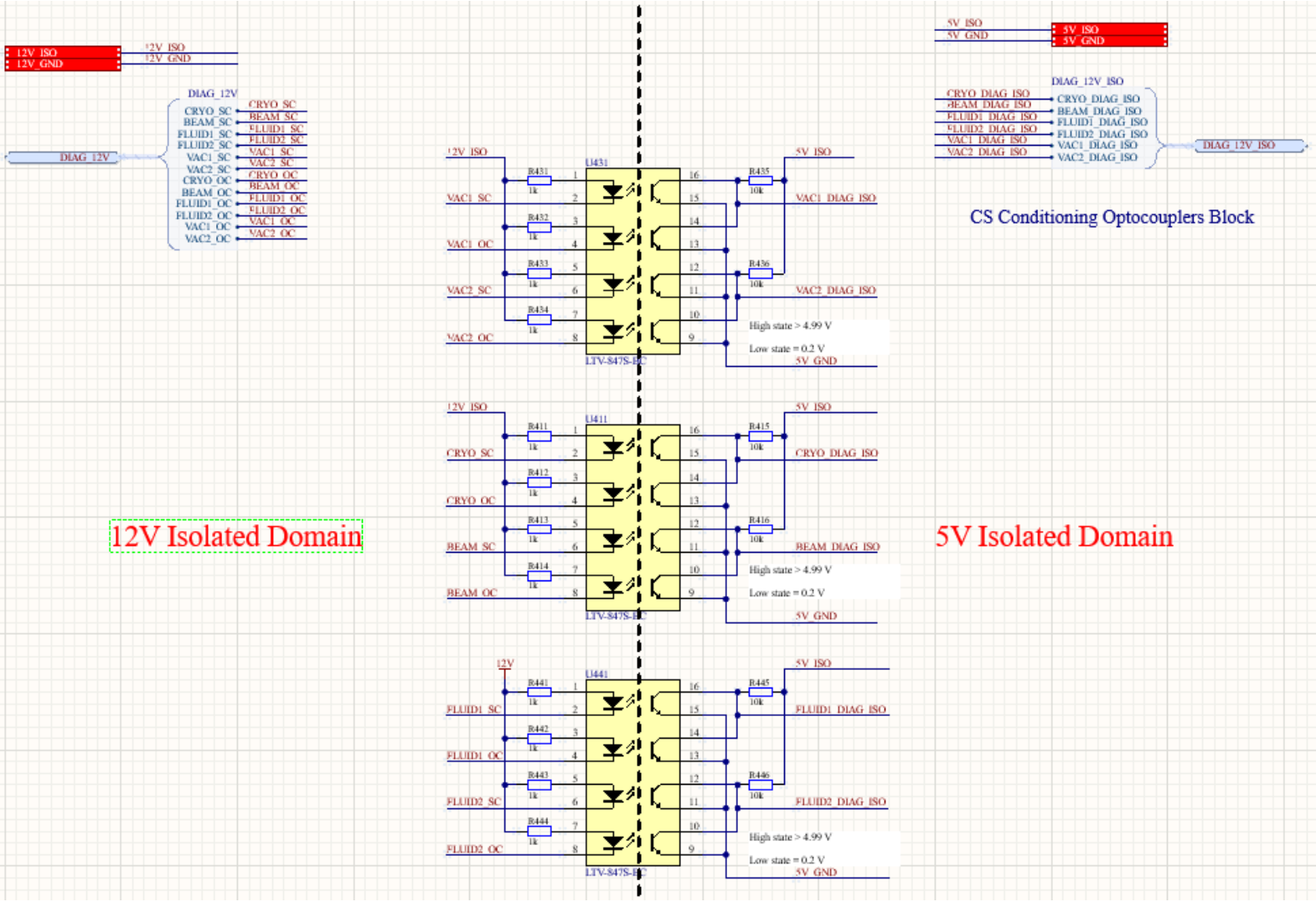
# The sub-module design details

- Optocouplers – Diag 12V Block



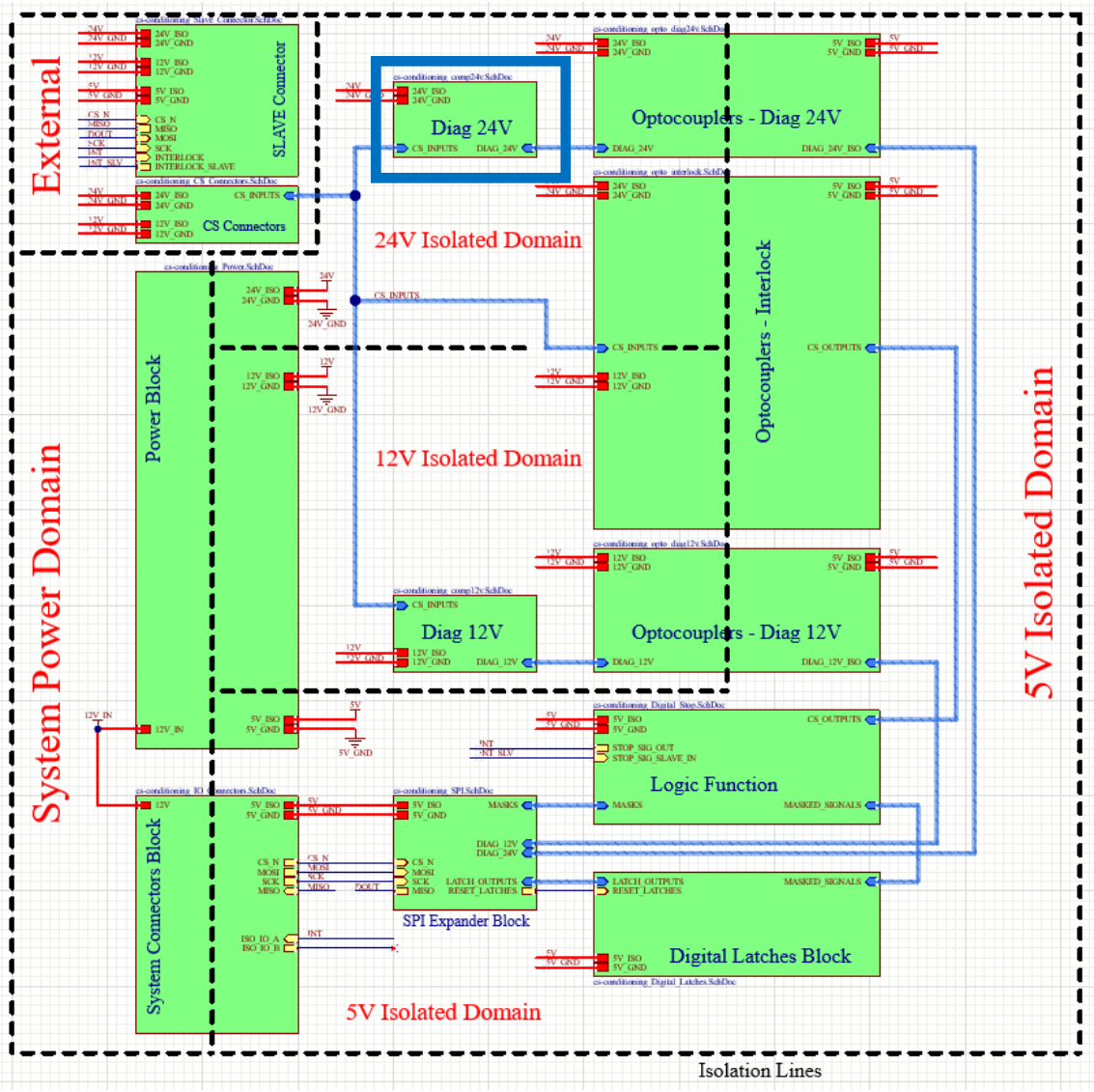
# The sub-module design details

- Optocouplers – Diag 12V Block



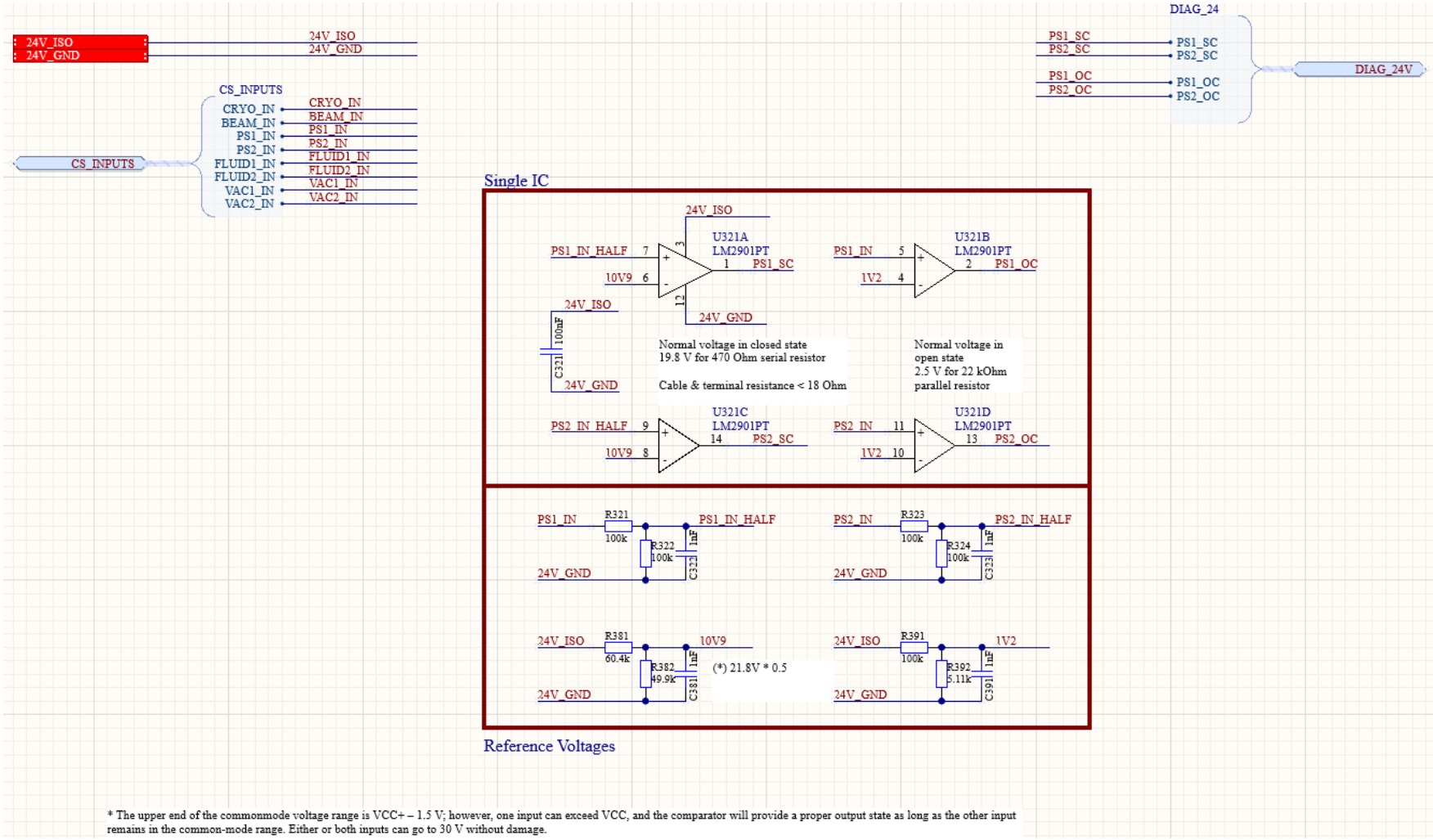
# The sub-module design details

- Diag 24V Block



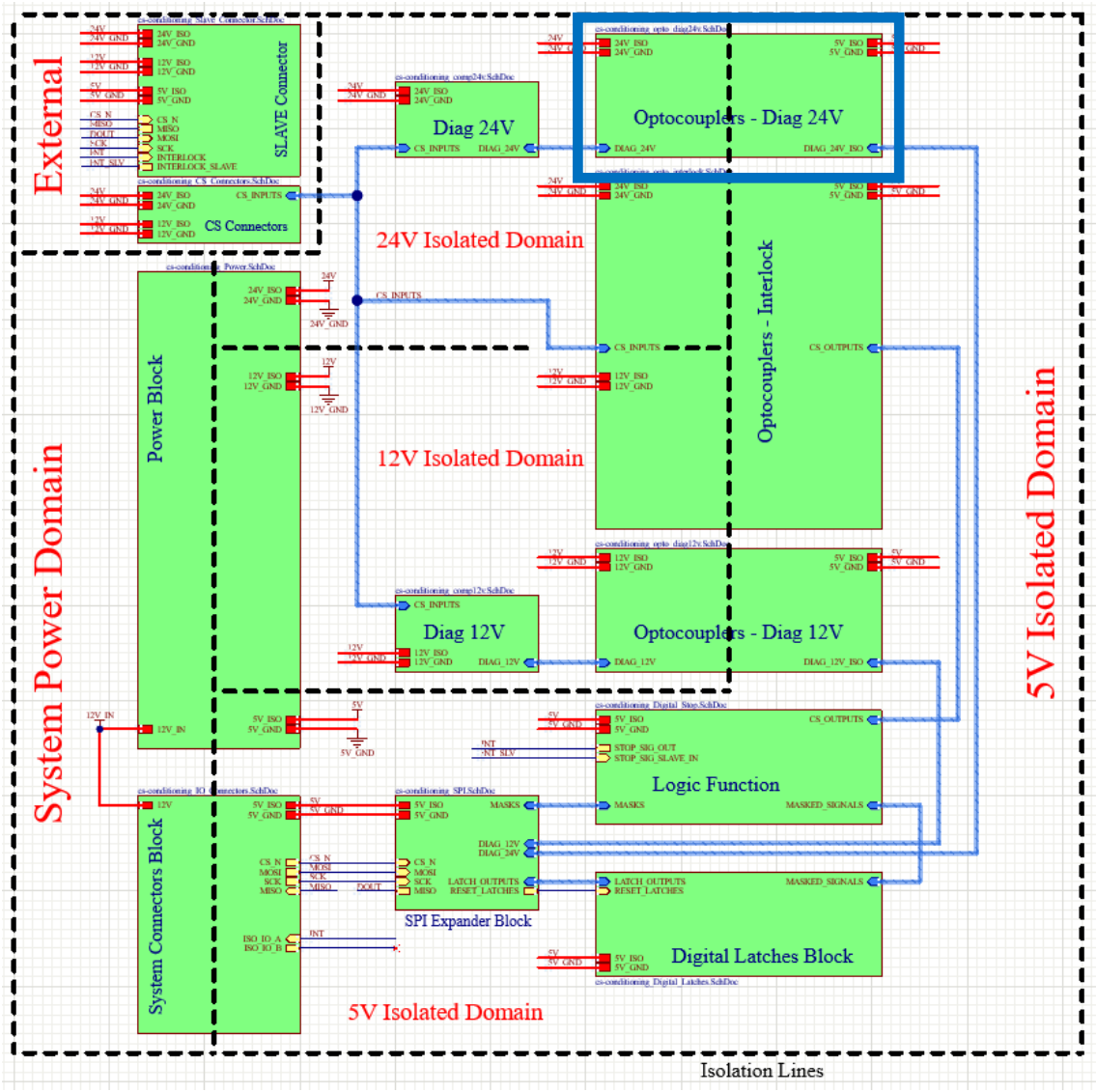
# The sub-module design details

- Diag 24V Block



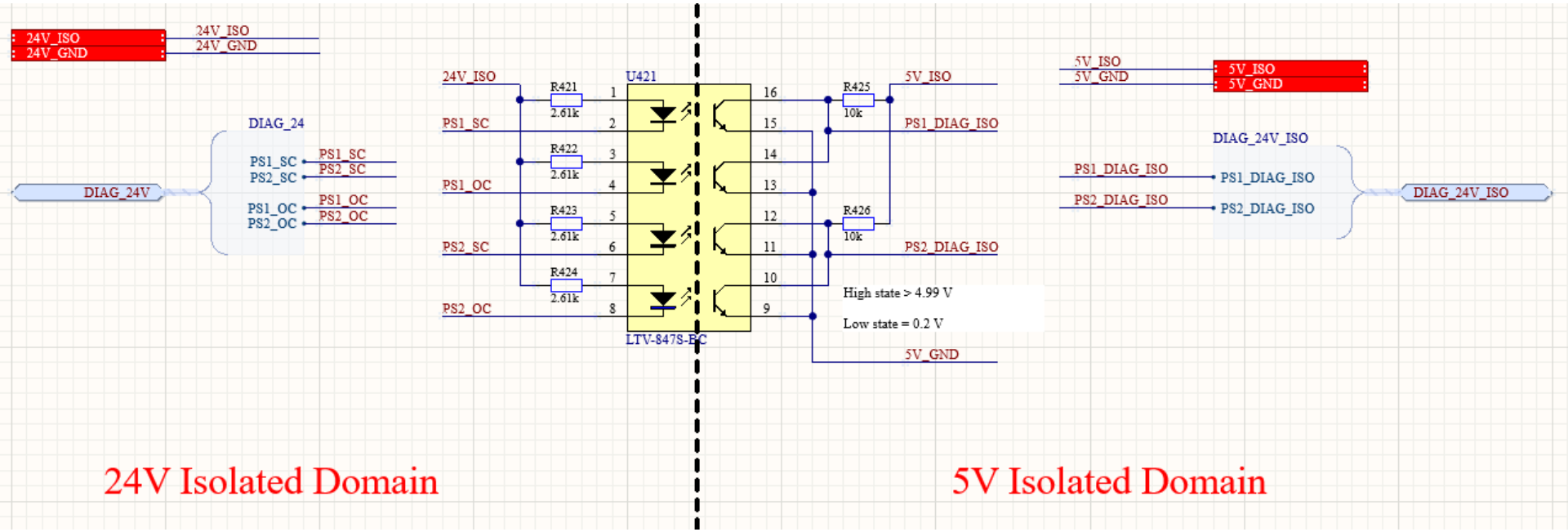
# The sub-module design details

- Optocouplers – Diag 24V Block



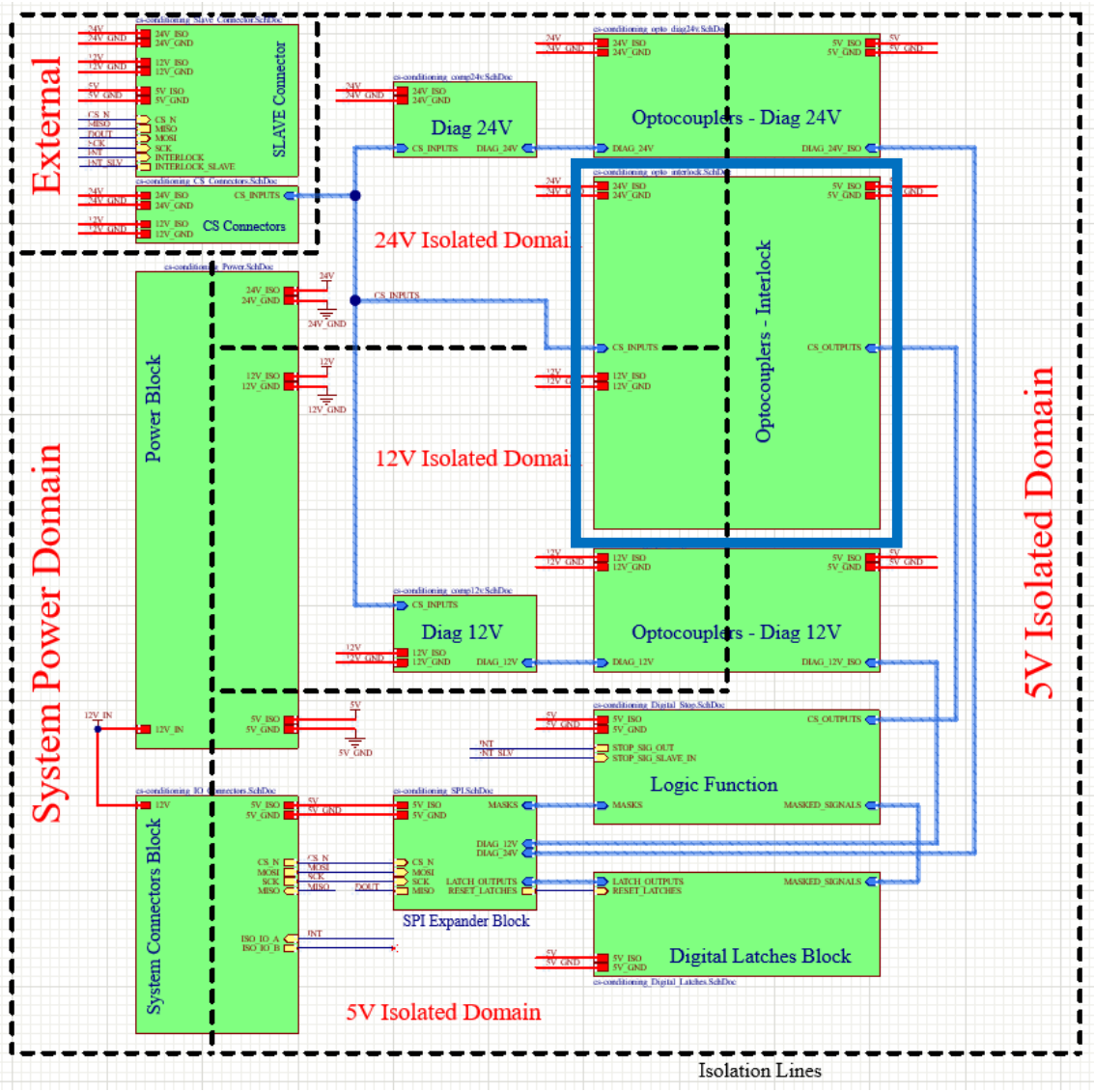
# The sub-module design details

- Optocouplers – Diag 24V Block



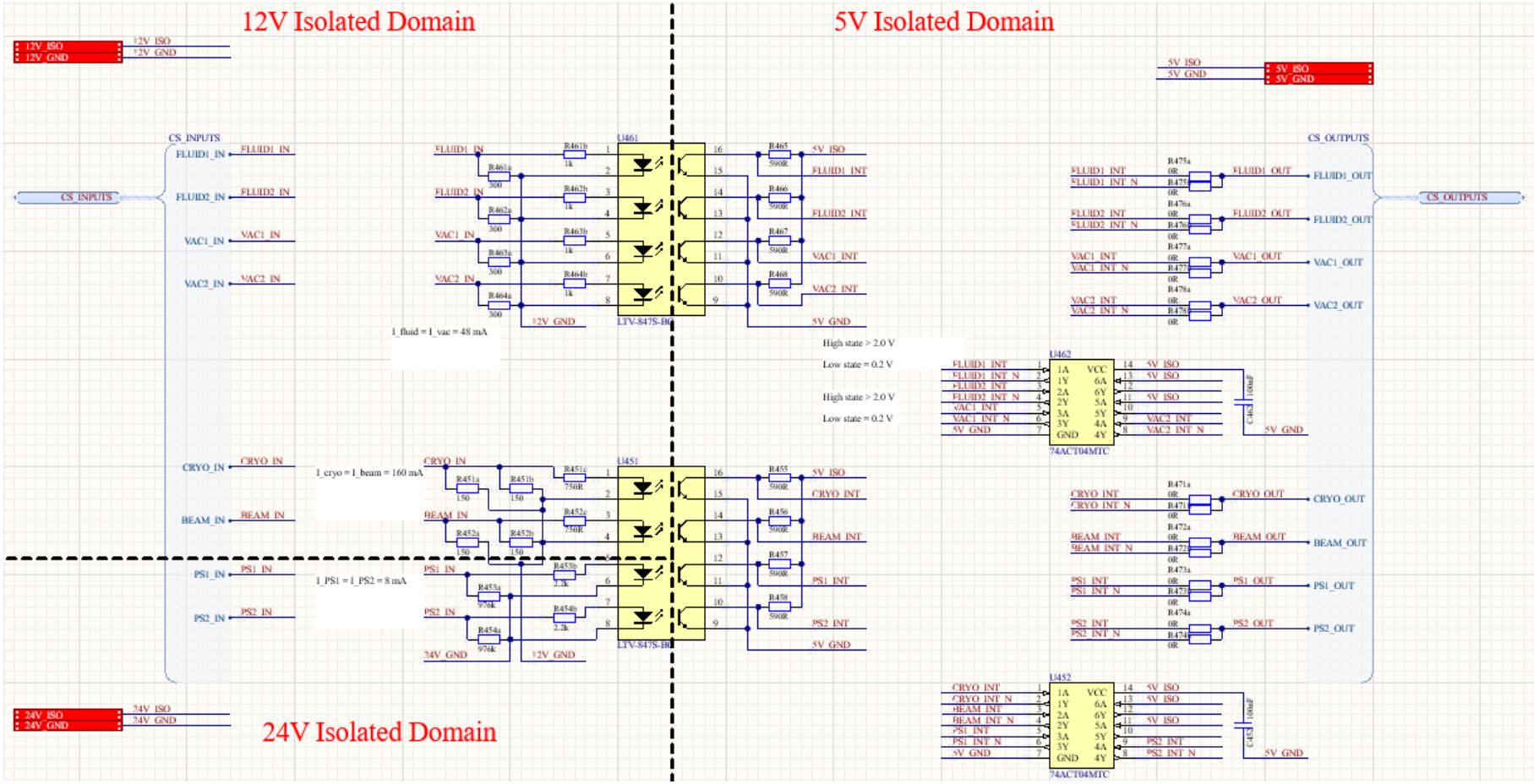
# The sub-module design details

- Optocouplers – Interlock



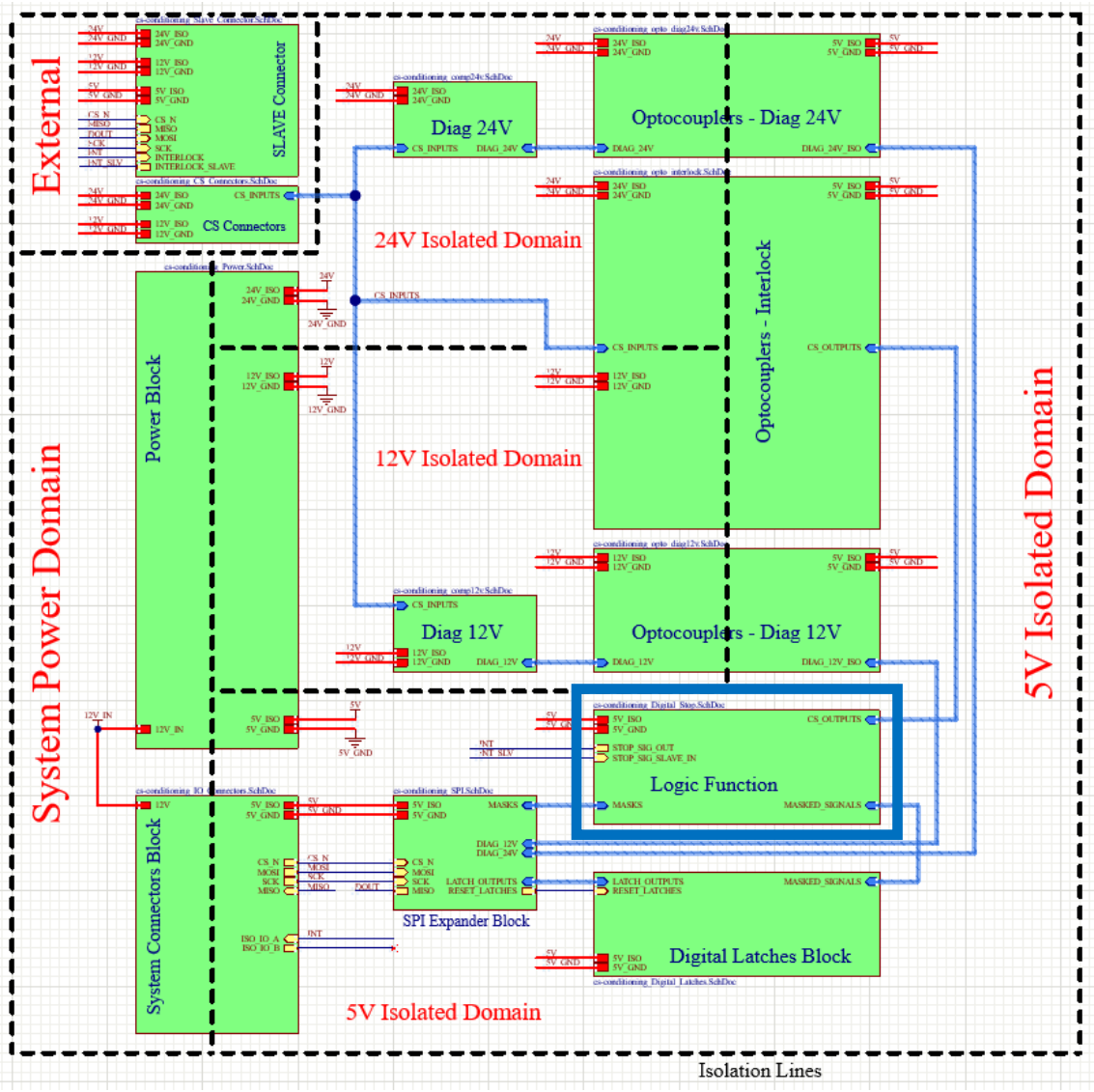
# The sub-module design details

- Optocouplers – Interlock



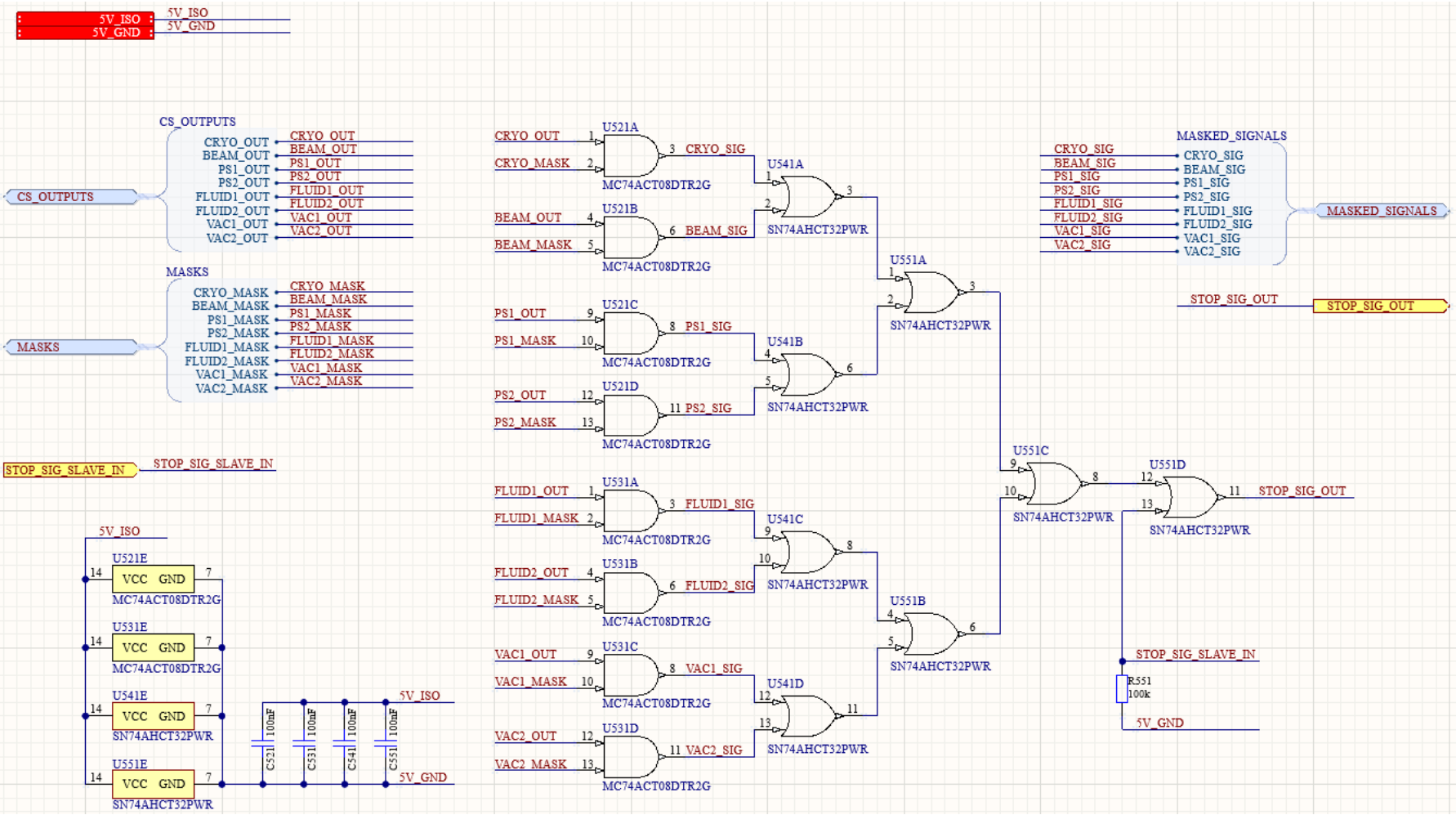
# The sub-module design details

- Logic Function Block



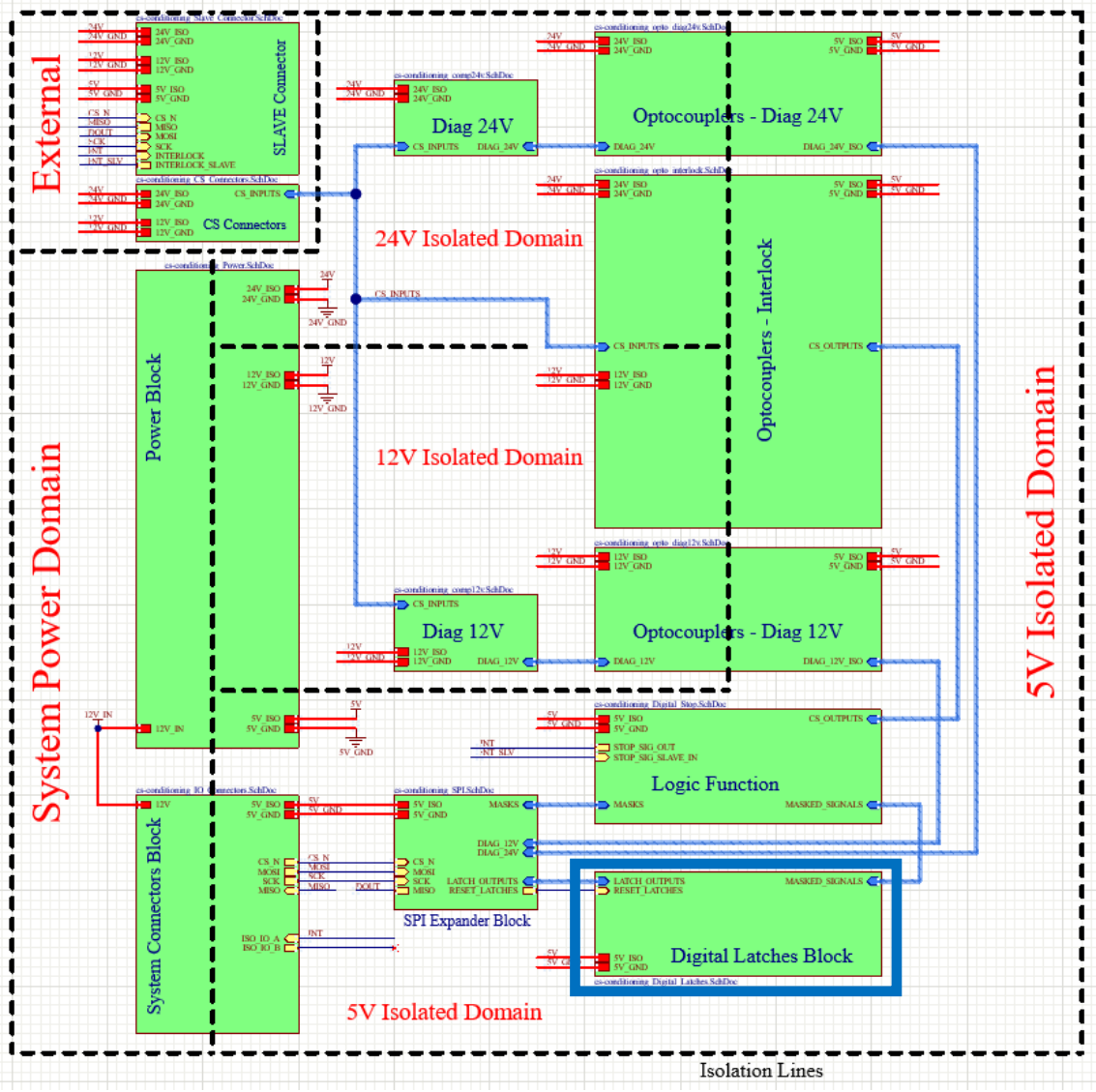
# The sub-module design details

- Logic Function Block



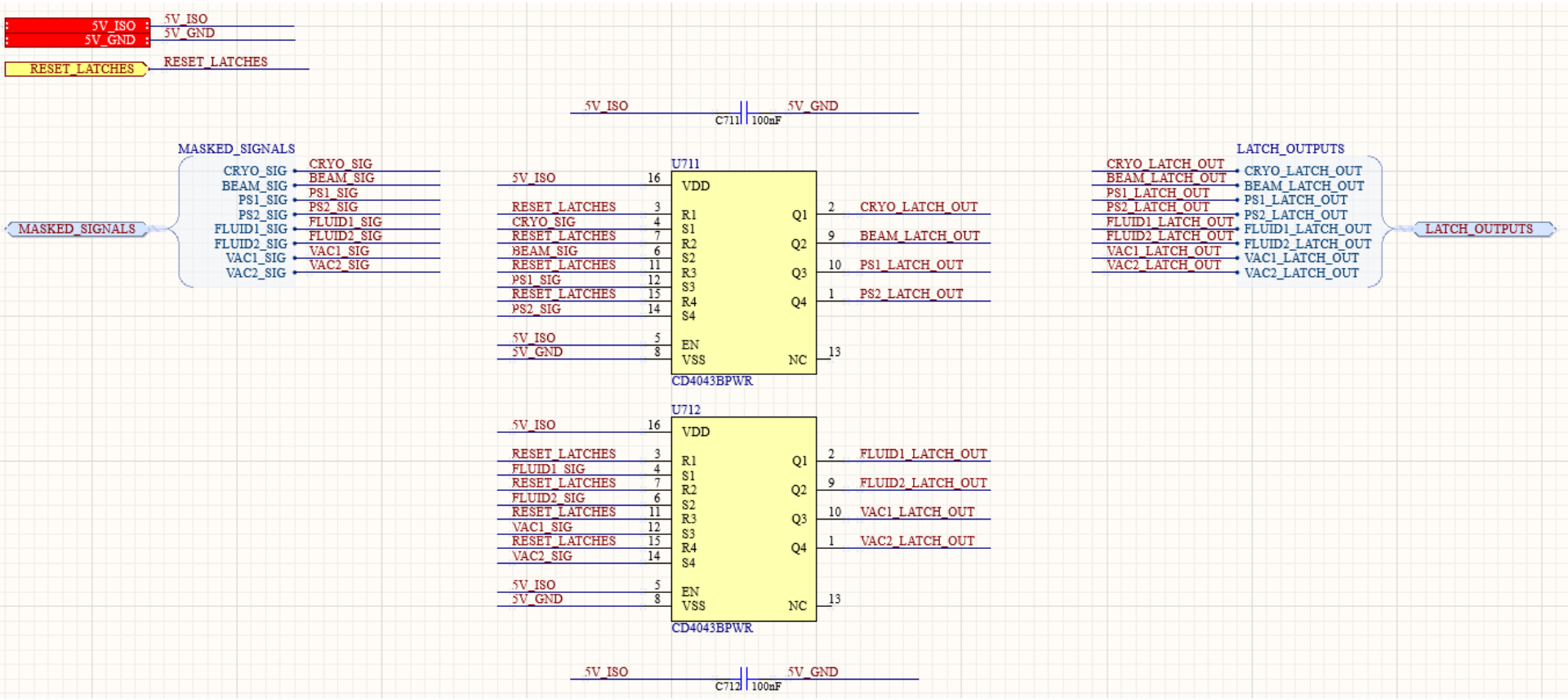
# The sub-module design details

- Digital Latches Block



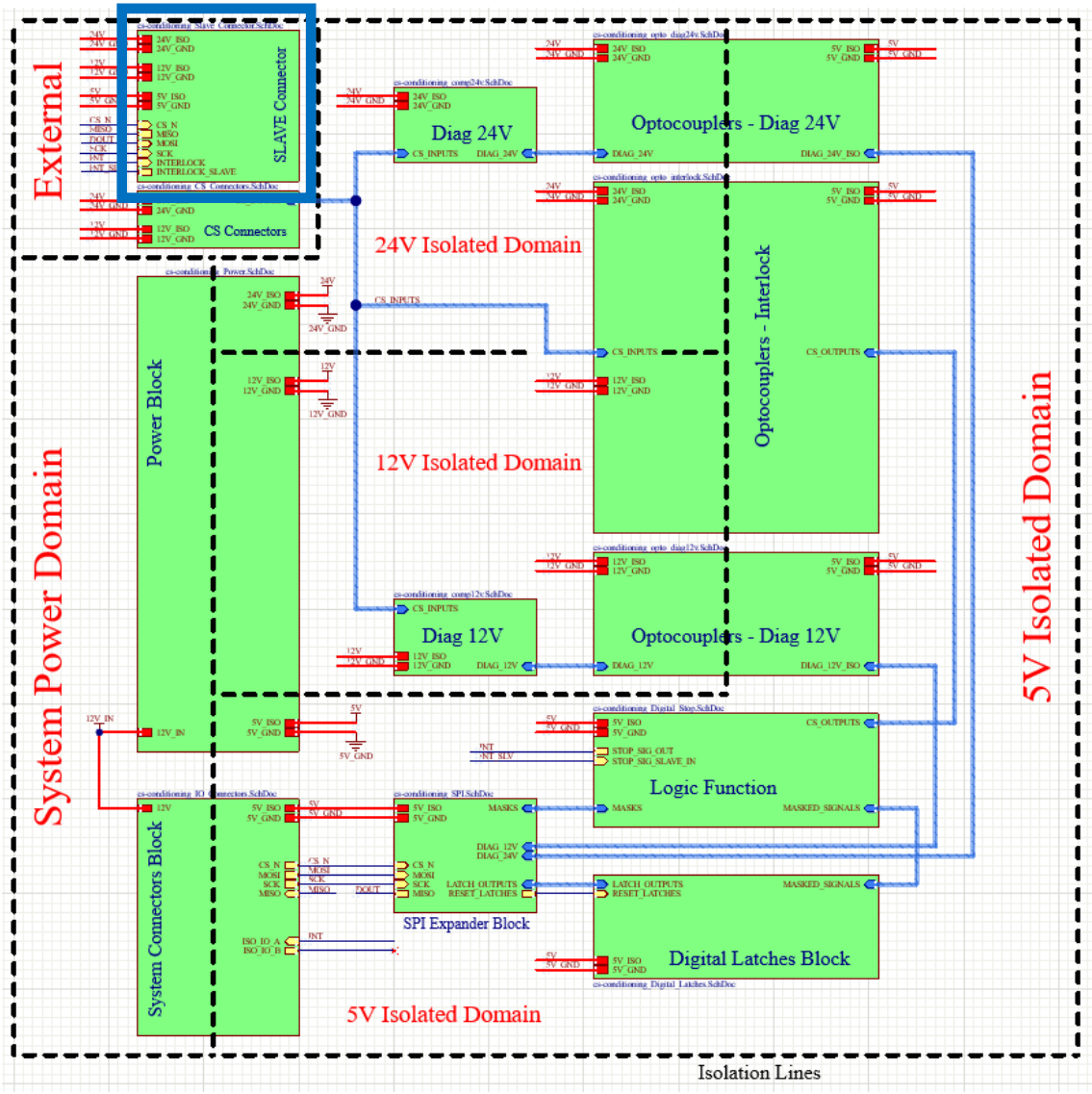
# The sub-module design details

- Digital Latches Block



# The sub-module design details

- SLAVE Connector Block



# The sub-module design details

- ADC GP Connectors Block