



Main logic realization HW

Piotr Amrozik





About me

Piotr Amrozik

Ph.D. in Electrical Engineering

- Role
 - RFPI project contractor
 - PCB designer / FPGA engineer
- Relevant experience
 - FastLogic Sp. z o.o.: FPGA Expert – FPGA prototyping, timing and synchronization, cryptography and hash algorithms (2020-2021)
 - National projects: Contractor – ASIC designer, PCB designer, FPGA engineer (2017-2020)
 - Ericpol Sp. z o.o. FPGA Engineer – ARUZ Large-scale, FPGA-based Analyzer of Real Complex Systems (2015-2017)





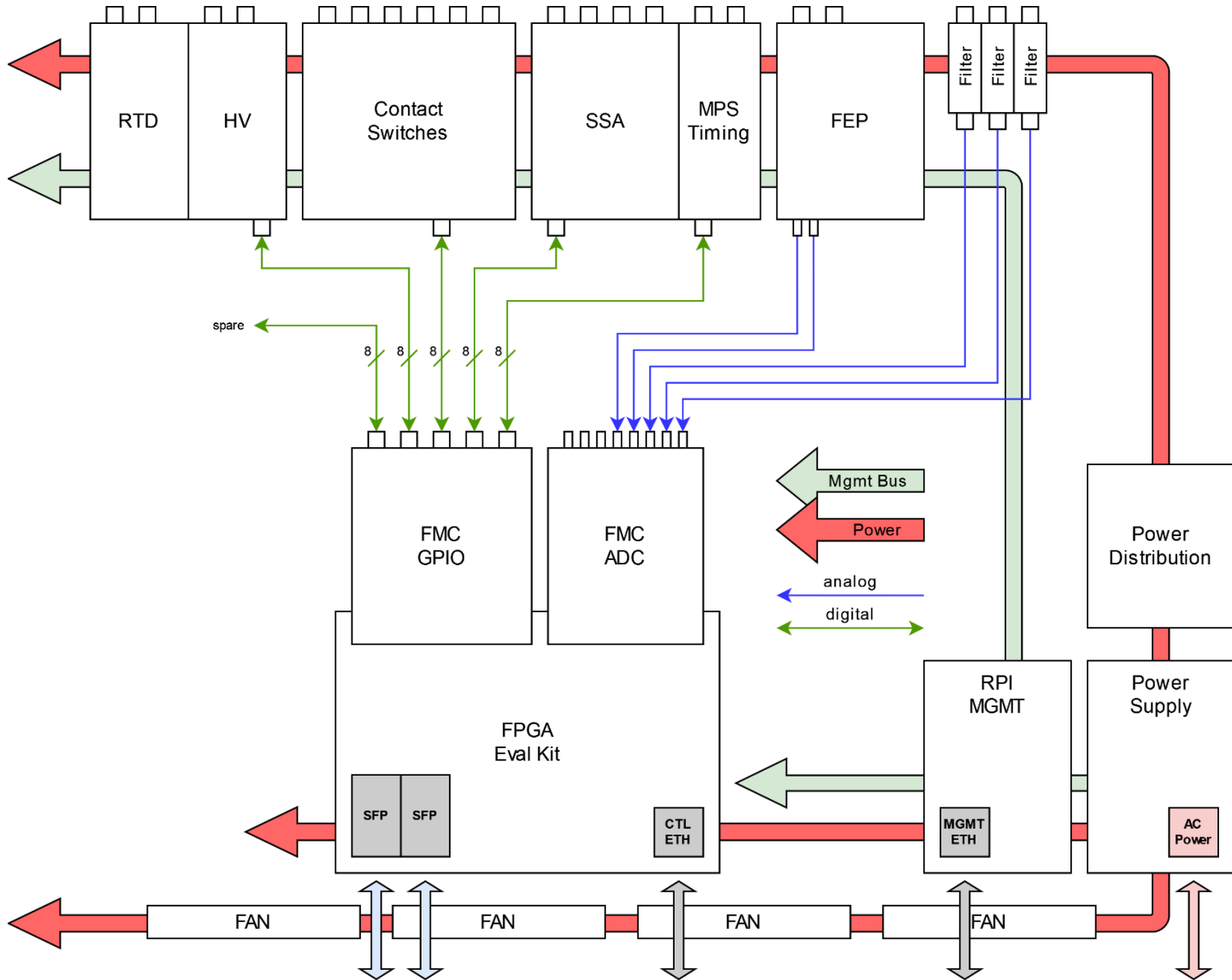
Agenda

- Main components
- Main FPGA module (features)
- FMC GPIO module:
 - specification,
 - design and schematics,
 - module production, assembly and commissioning,
 - tests results
- The FMC ADC module:
 - specification,
 - design and schematics,
 - module production, assembly and commissioning,
 - tests results
- Summary



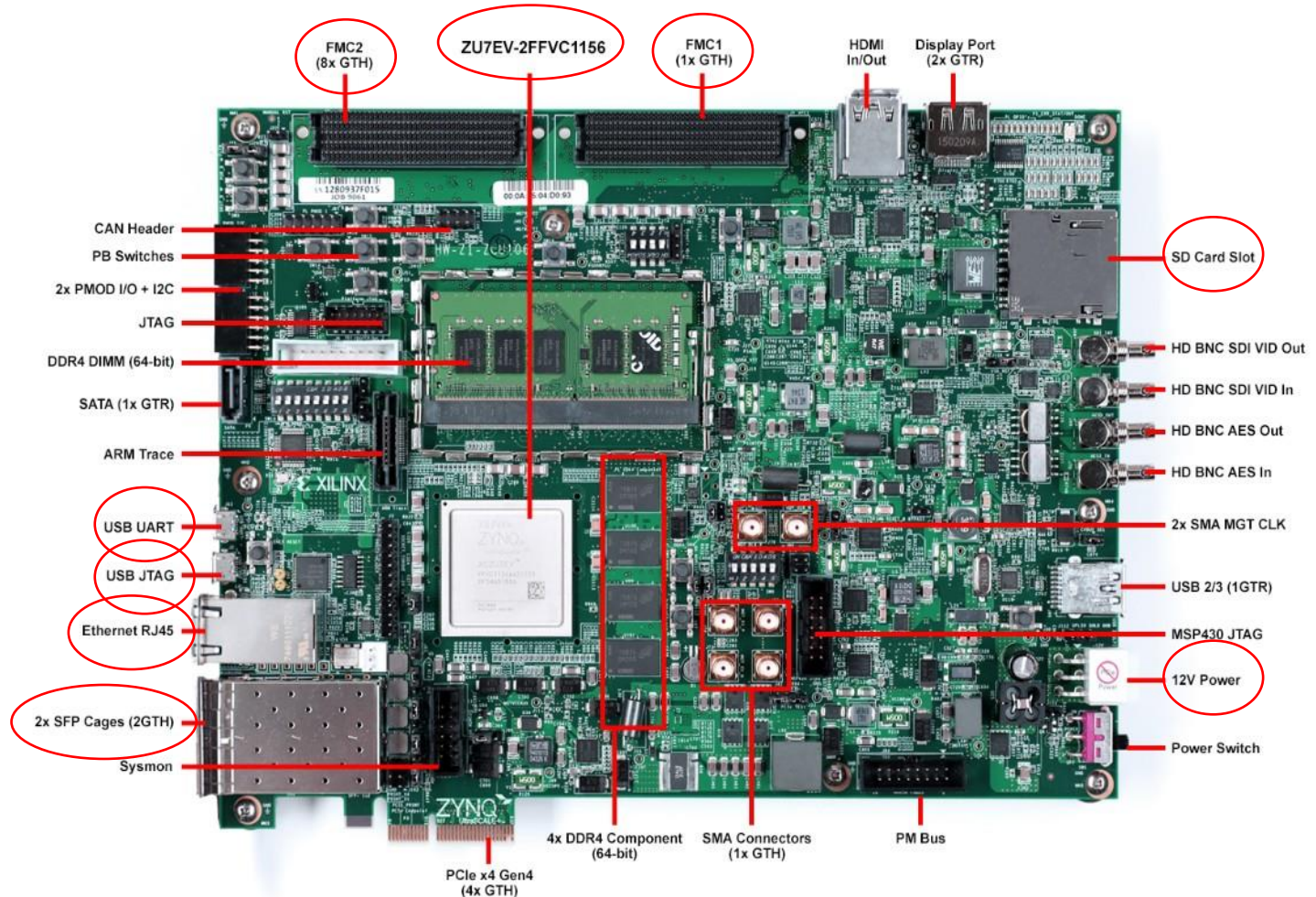


The main logic components



Main FPGA module – Xilinx ZCU106

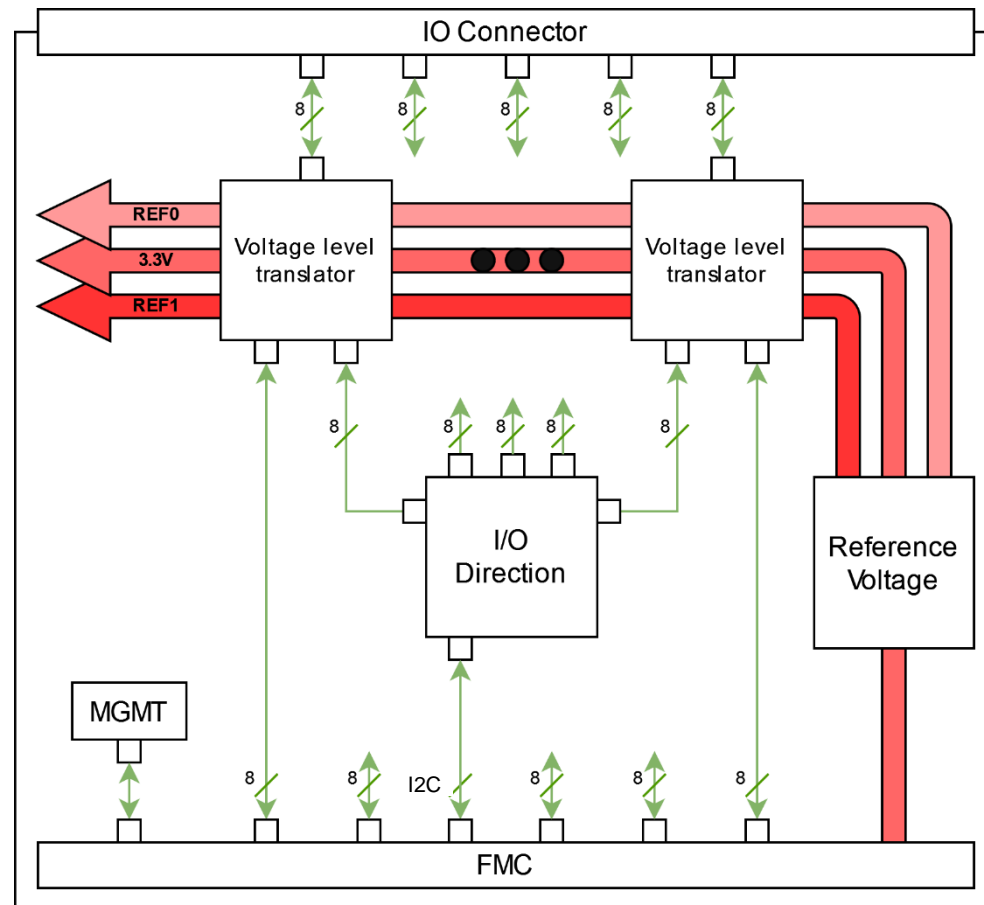
- Zynq UltraScale+™ MPSoC is equipped with a quad-core Arm® Cortex®-A53 applications processor, and 16nm FinFET+ programmable logic
- 2x FPGA mezzanine card (FMC) interfaces for I/O expansion





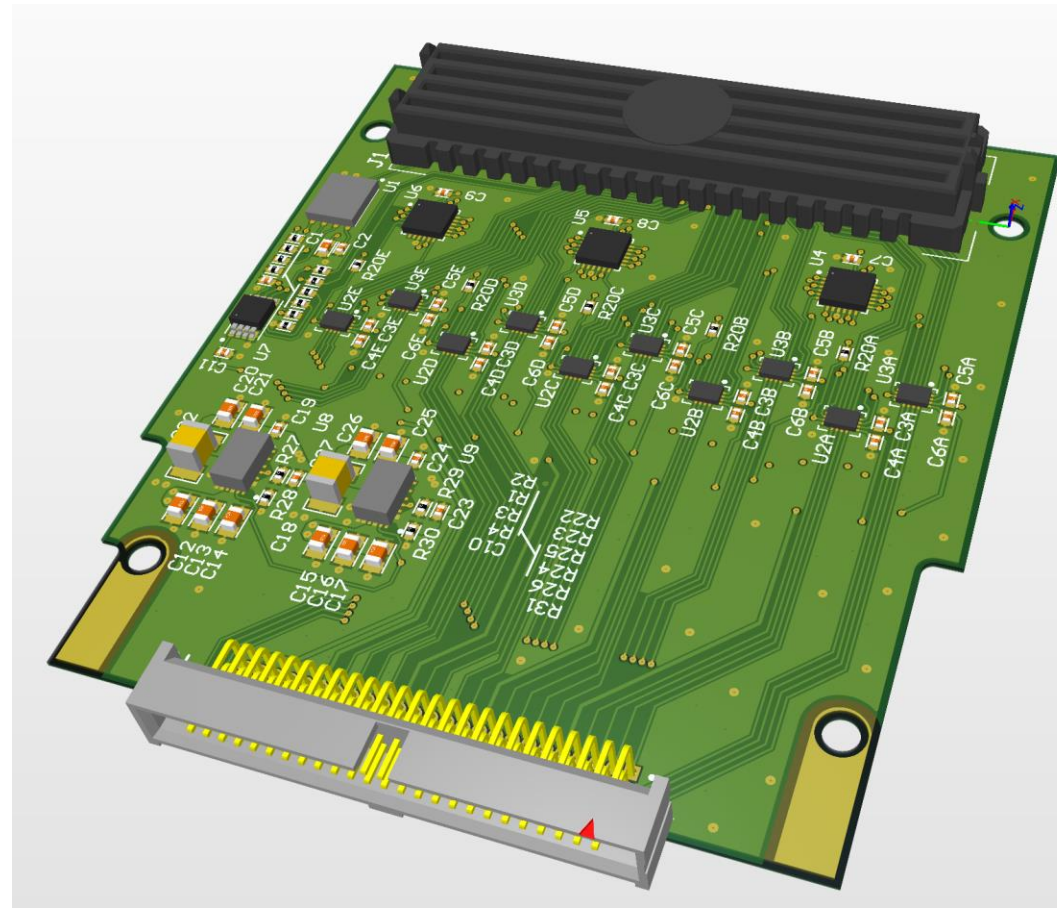
FMC GPIO – specification

- FPGA mezzanine card (FMC) compliant
- 8 GPIO single-ended and 2 power connections for every board (40 GPIOs in total)
- Each GPIO leads signals
 - up to 50MHz
 - terminated on external boards
 - Thevenin termination on receiver
 - Series termination on transmitter
- buffered with voltage translators:
 - with configurable amplitude (3.3V, 1.8V, 1.2V)
 - with configurable direction and Hi-Z state via I2C expanders (controlled by Zynq ARM or programmable logic)
- Board is powered from ZCU106 (12V, 3.3V, 3.3V AUX, VADJ)
- 1.2V and 1.8V produced by on-board DC/DC converters



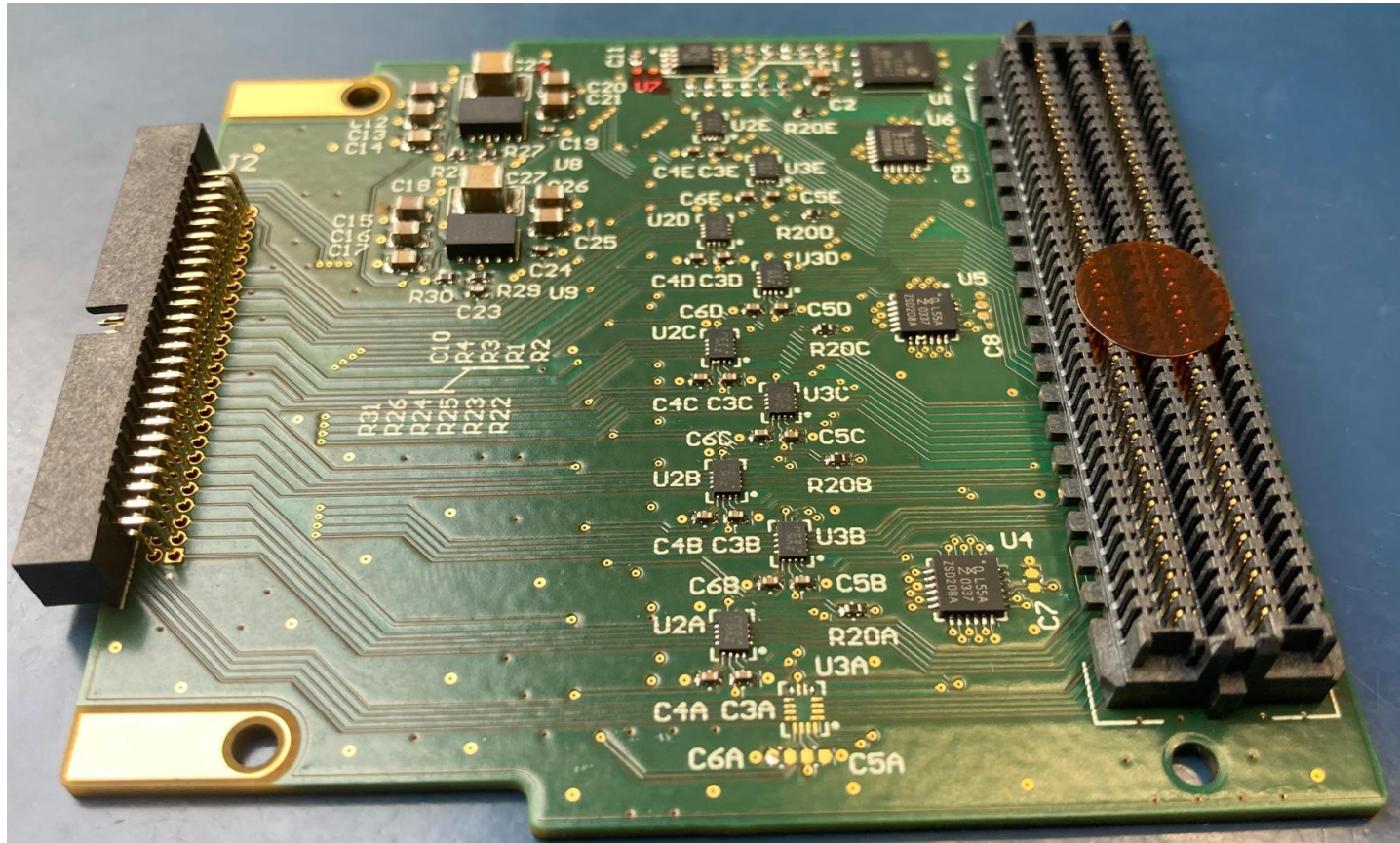
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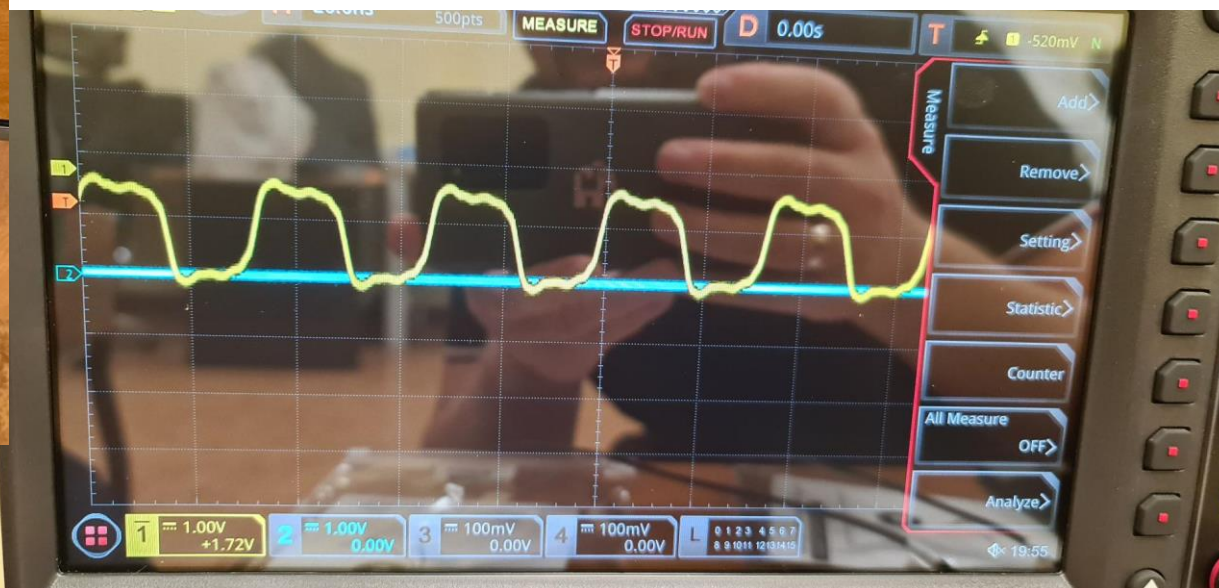


FMC-GPIO – assembly












FMC GPIO – tests (loopback test)





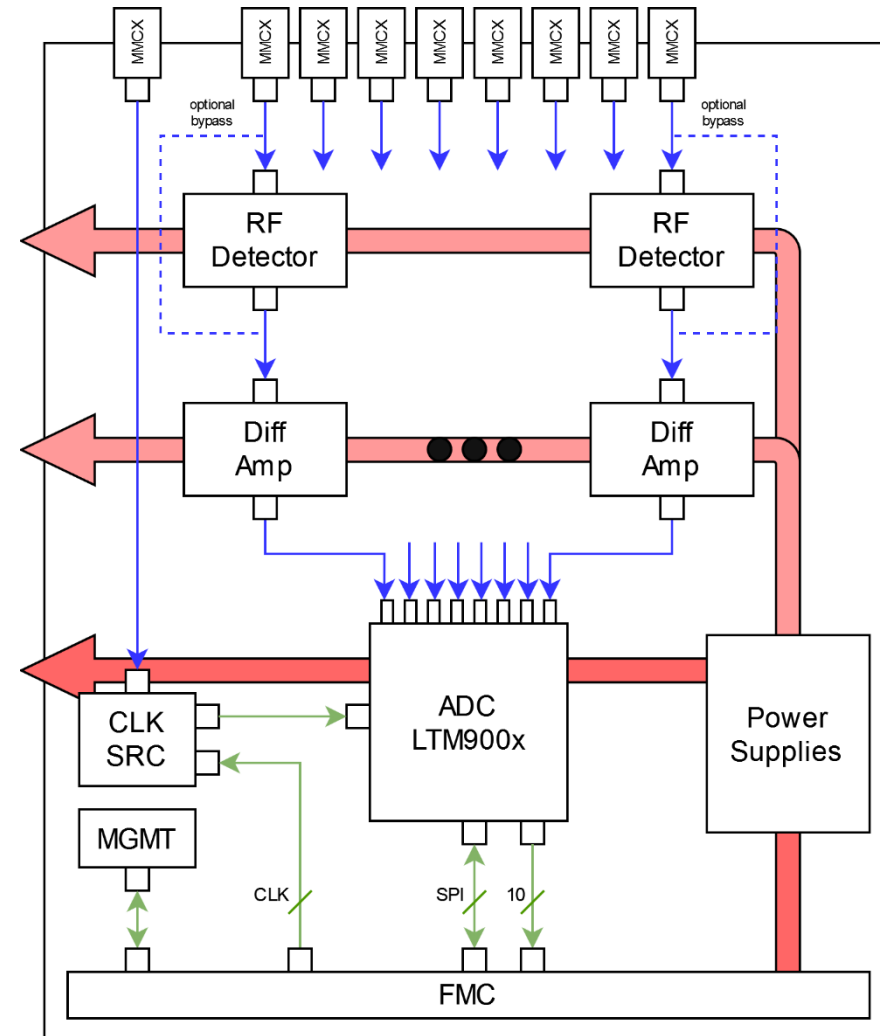
FMC GPIO – tests (summary)

- FPGA mezzanine card (FMC) compliant 
- 8 GPIO single-ended and 2 power connections for every board (40 GPIOs in total) 
- Each GPIO leads signals 
 - up to 50MHz
 - terminated on external boards
 - buffered with voltage translators:
 - with configurable amplitude (3.3V, 1.8V, 1.2V) 
 - with configurable direction and Hi-Z state via I2C expanders (controlled by Zynq ARM or PL) 
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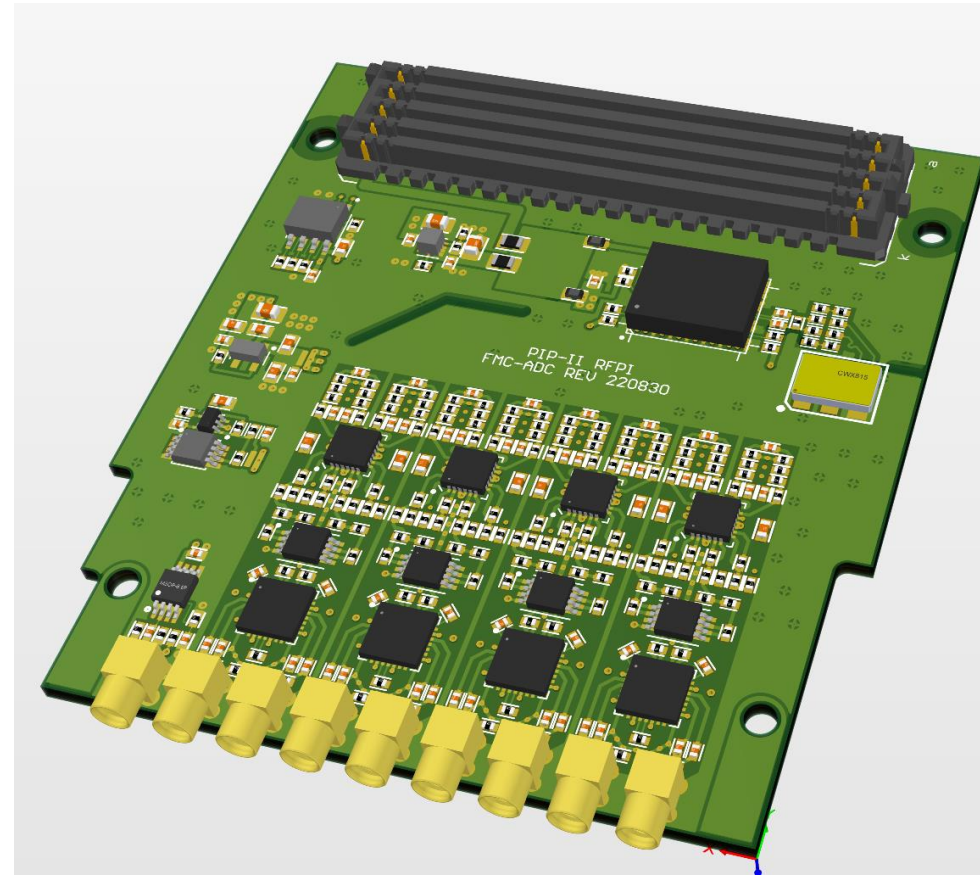
FMC ADC – specification (digital part)

- FPGA mezzanine card (FMC) compliant
- On-board ADC communication LTM9006-14 (8 channels, 14-bit, 25MS/s):
 - control SPI interface via FMC connector
 - 8x data channels
- Clock signal for on-board ADC:
 - produced by FPGA via FMC connector
 - generated by on-board 125MHz oscillator
 - generated externally via MMCX connector
- Board powered from ZCU106 (12V, 3.3V, 3.3V AUX, VADJ)
- 1.8V and 3.0V and V_BIAS produced by on-board DC/DC converters









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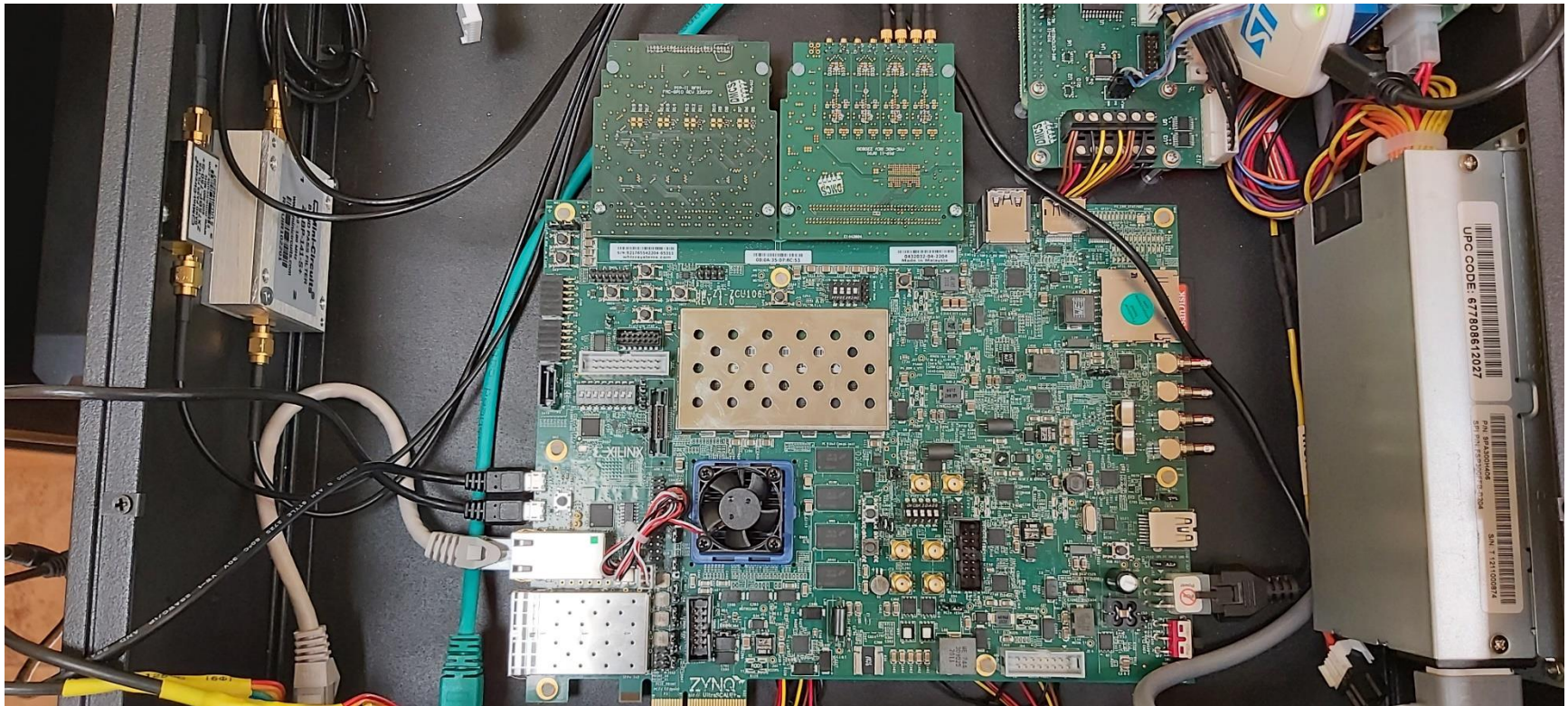


FMC-ADC – tests (digital part)

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- On-board ADC communication LTM9006-14 (8 channels, 14-bit, 25MS/s):
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Main logic components assembly



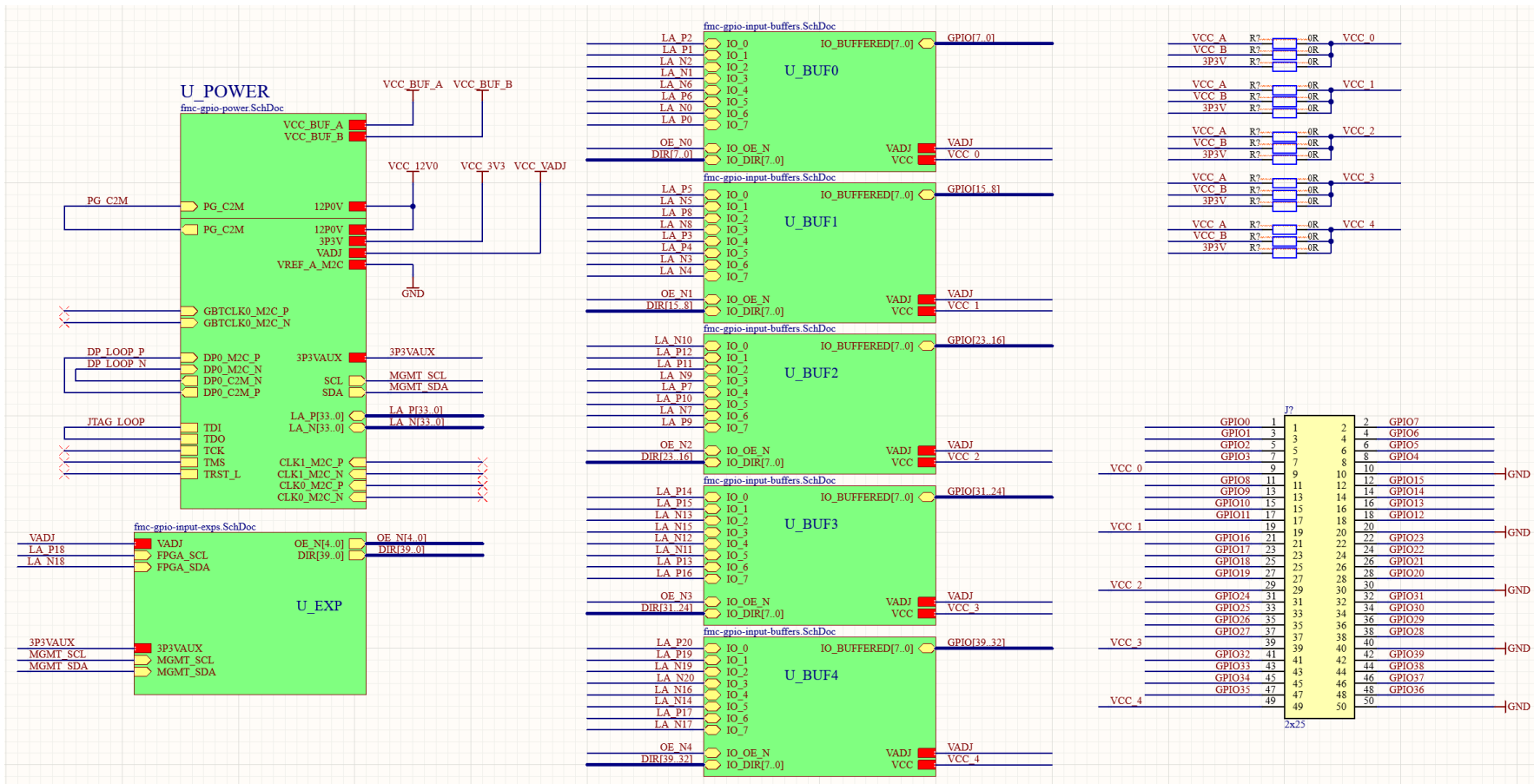


Thank you for your attention!





FMC GPIO – schematic





FMC ADC – schematic

