Signal Conditioning: SSA sub-module

Bartosz Pękosławski & Paweł Marciniak

About us

Bartosz PĘKOSŁAWSKI

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - Projects on machine vibration monitoring – hardware engineer (2006 – 2011)
  - TULCOEMPA – hardware designer (2011 – 2015)
  - SPParTAN – hardware designer (2019 – 2022)
  - FOSREM – hardware designer (2021 – present)

Paweł MARCINIAK

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - INNOREH – software designer (2017 – 2021)
  - SPParTAN – firmware designer (2019 – 2022)
  - ITER – hardware engineer (2021 – 2022)
  - FOSREM – hardware designer (2021 – present)

Agenda

- The SSA module requirements
- The PoC version specification and scope
- The sub-module design details
- Implementation
- Test results discussion
- Full scale design plans
- Summary

The SSA module requirements

- The SSA signals group:
  (SSA Inh, SSA DC Inh, LLRF Inh, MPS Inh)
- Delay between input and output less then 1 μs
- Isolation between inputs and outputs

Signal Name	Peripheral Need	IO Pins per Peripheral	IO Pins Per RFPI	Signal Type	Quantity	I/O	RFPI Response Time	Impedance	Cable Type	Connector
SSA Inh	IO	1	4	TTL/digital output	1 per cavity/coupler	Output	<1 μs	50Ω	coaxial RG-58	SMA
SSA DC Inh	IO	1	4	TTL/digital output	1 per cavity/coupler	Output	<1 μs	50Ω	coaxial RG-58	SMA
LLRF Inh	IO	1	4	TTL/digital output	1 per cavity/coupler	Output	<1 μs	50Ω	coaxial RG-58	SMA
MPS Inh	IO	1	4	TTL/digital output	1 per cavity/coupler	Output	<1 μs	50Ω	coaxial RG-58	SMA

The PoC version specification and scope

- One PCB board which supports 8 signals:
  - SSA Inh (x1)
  - SSA DC Inh (x1)
  - 1x LLRF Inh (x1)
  - ~~MPS Inh~~
  - SPARE signals (x5)
- Management Block
- Power Supply Voltage: 12 V
- Management Block Supply Voltage: 3.3 V
- Isolation of GPIO and MGMT_STATUS signals
- Connector type: BNC

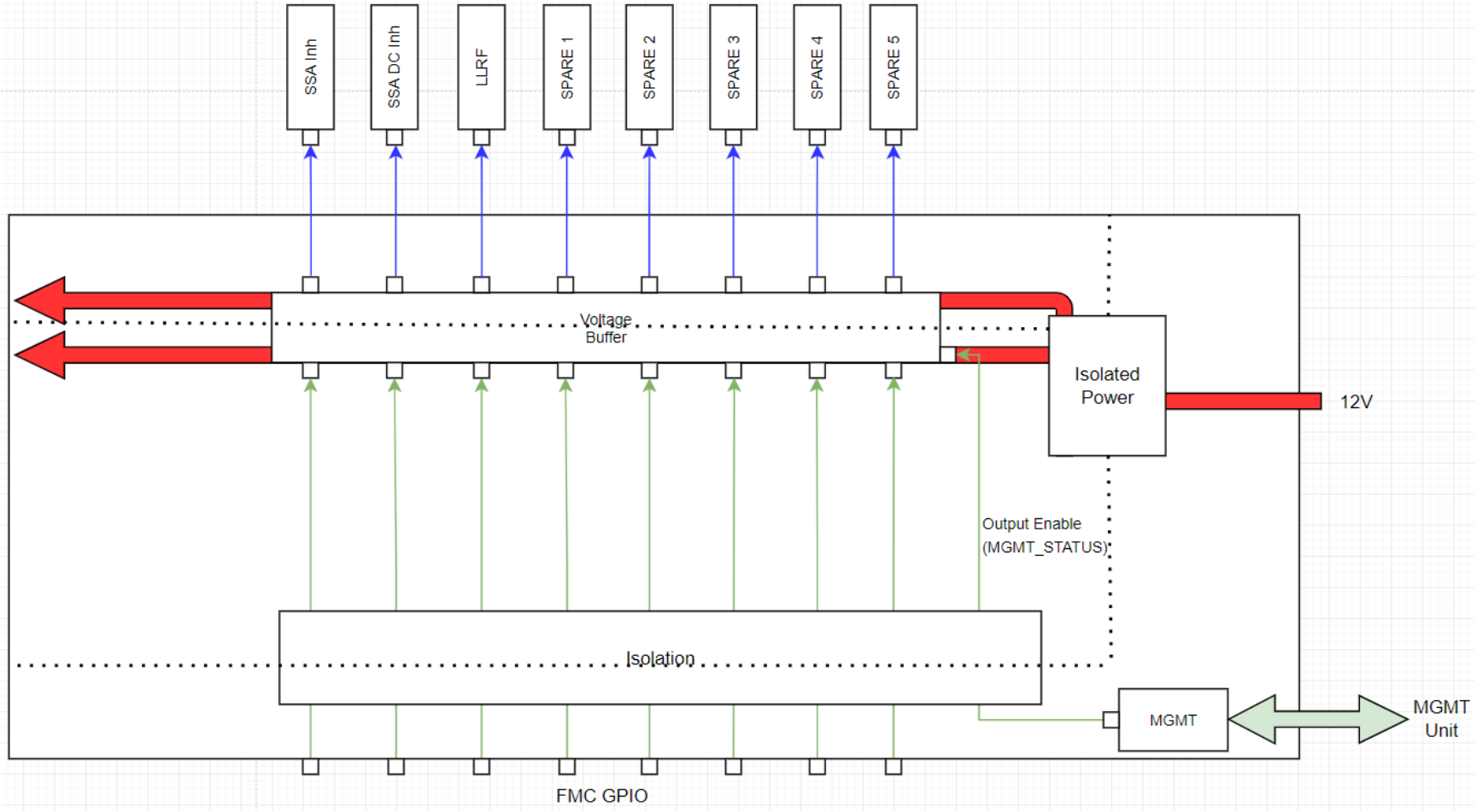
The PoC version specification and scope

Management Block:

- I2C communication with Raspberry PI
- Current measurement
- Temperature and humidity measurements
- Permission signal (MGMT_STATUS)

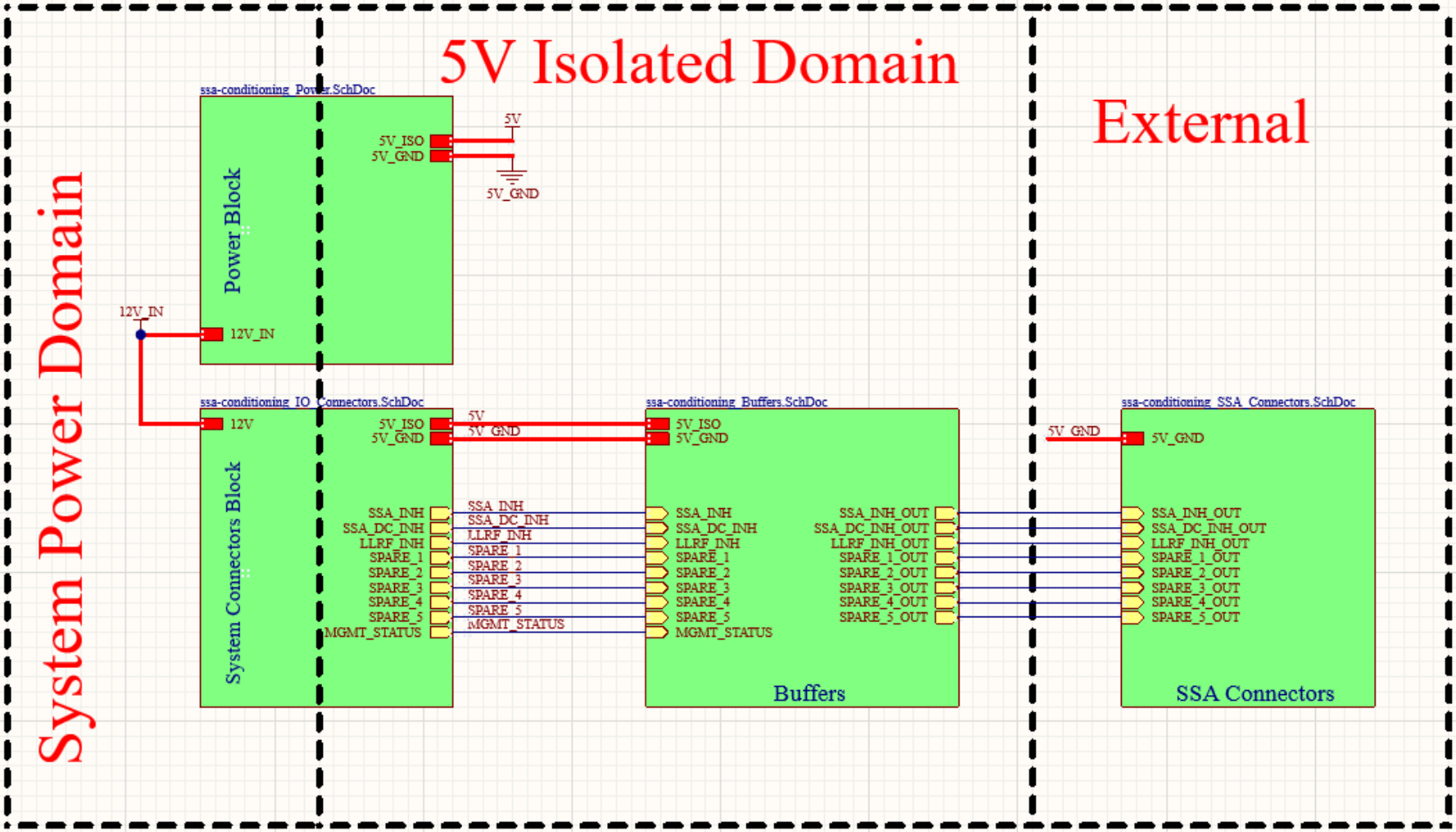
The sub-module design details

Conceptual diagram



The sub-module design details

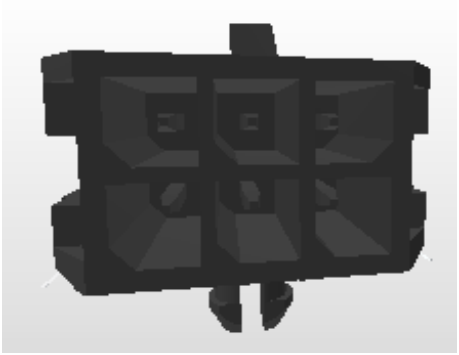
Block diagram



The sub-module design details

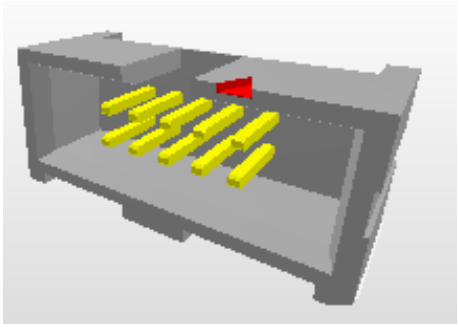
System Connectors Block

- Power Connector (12 V)



- MGMT Connector (I^2C, MGMT_STATUS, MGMT_PRESENT) and sensors

- FMC GPIO Connector



- Isolation of GPIO and MGMT_STATUS signals based on MAX22245BAWA+ digital isolators (2 channels, 7 ns delay, up to 25 Mbps, 868 V_{RMS} continous / 5 kV_{RMS} 60s / 12.8 kV_{RMS} surge galvanic isolation)

The sub-module design details

Buffers Block

- Two 74AHCT125 quad buffers (TTL logic levels, 3-14 ns propagation delay)
- Output enable inputs controlled by MGMT_STATUS signal (inverted)

SSA Connectors Block

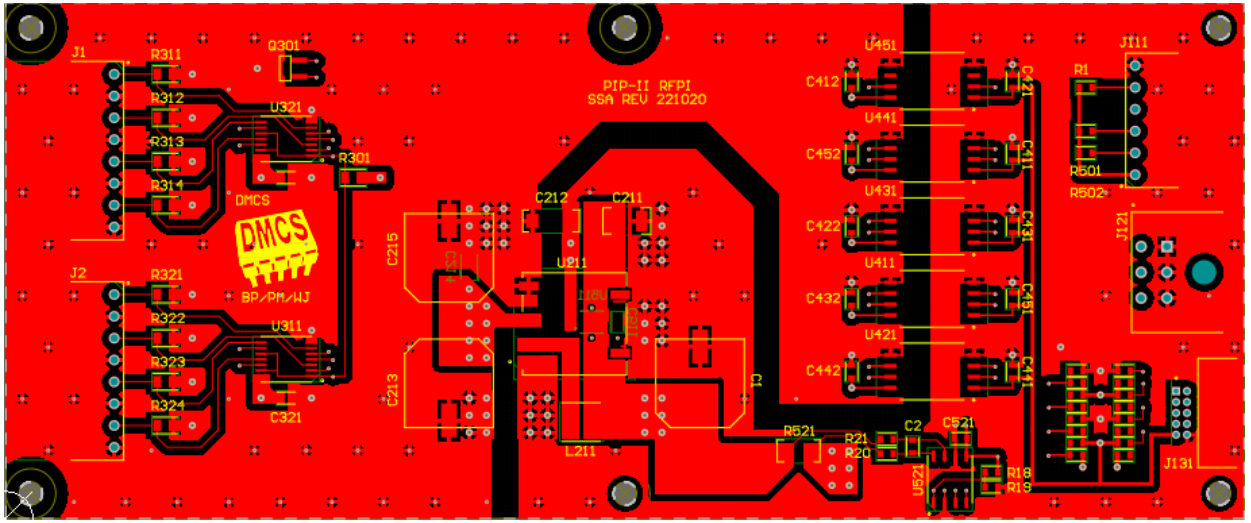
- Two 8-pin connectors (universal) for interconnecting with front panel connectors

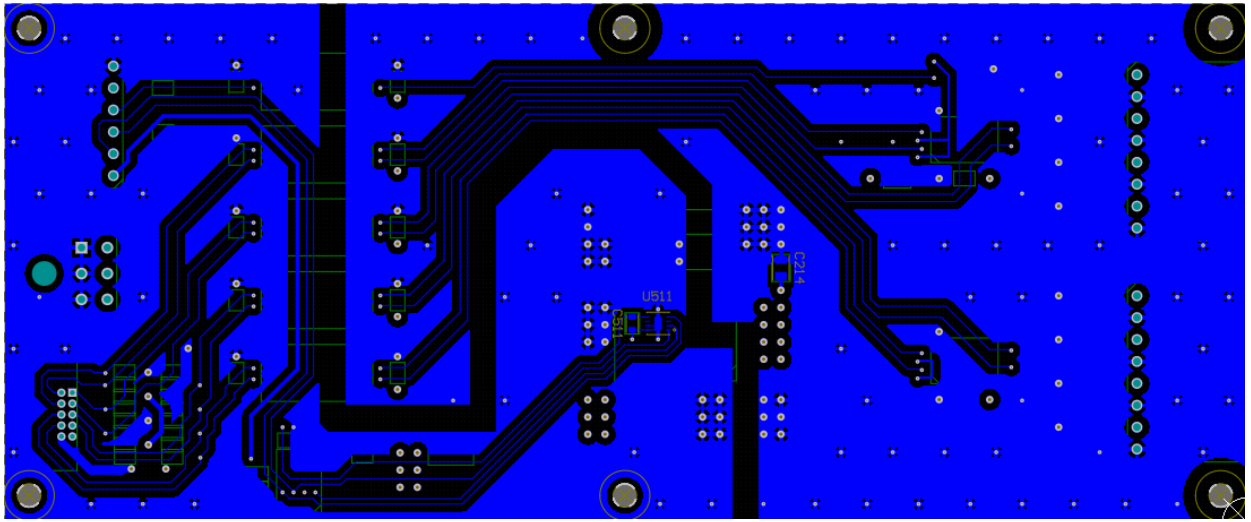
Power Block

- 12V → 5V SMPC module Traco Power TRS 2-1211 (isolated, 9-18 V input, max. 2 W output power, 80% efficiency, 1.6 kV isolation)
- EN 55032 class A external filter at the input for radiated and conducted emission

Implementation

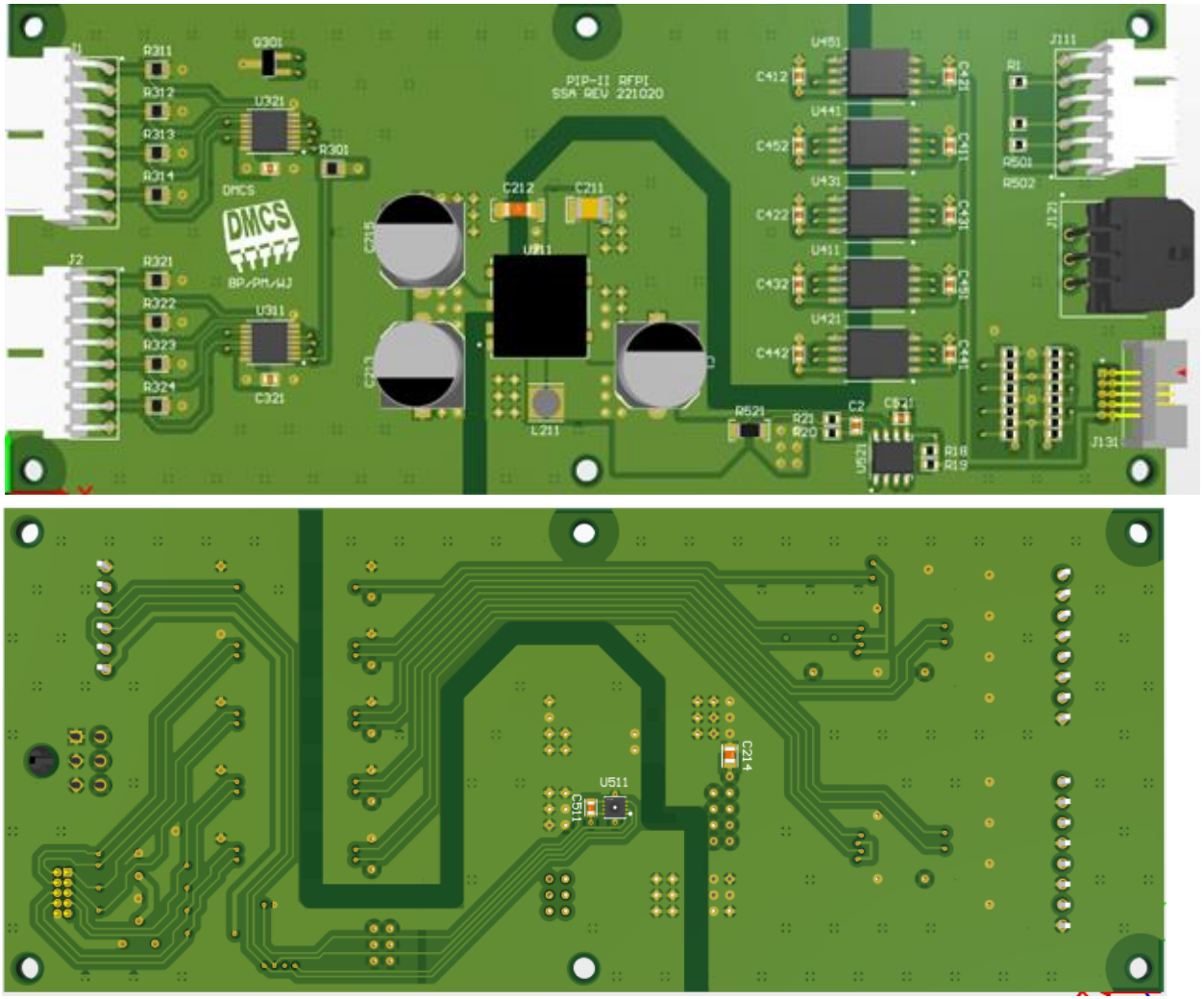
4-layer PCB, dimensions: 144 mm x 60 mm





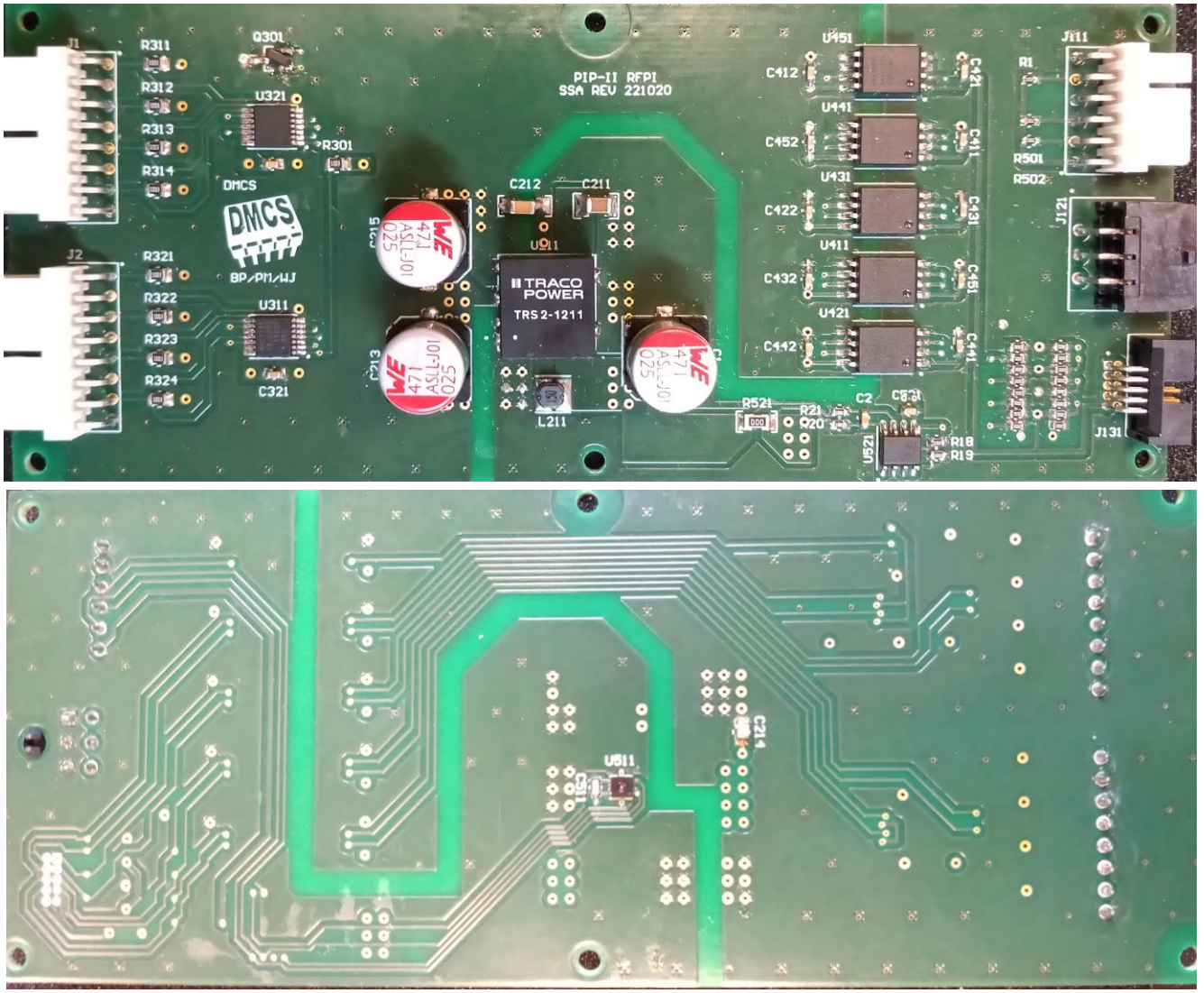
Implementation

3D model



Implementation

Real view

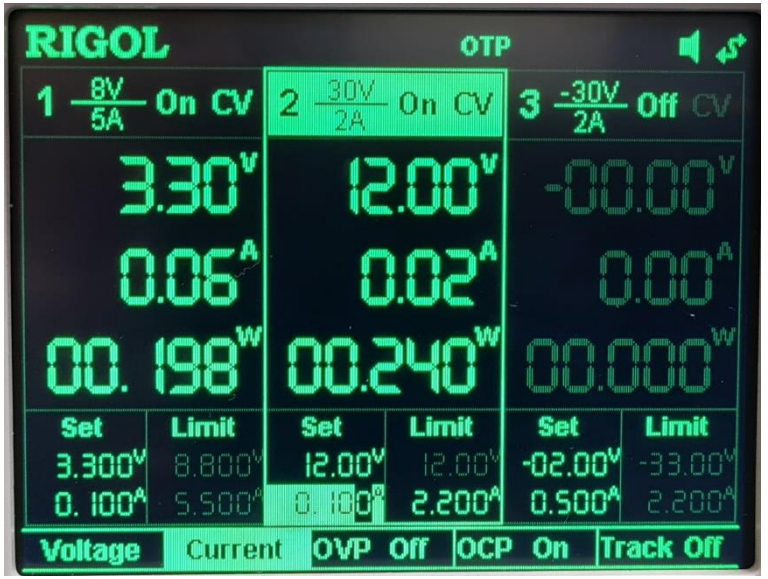


Test results discussion

- Detection of soldering faults (manual soldering)
  - Short circuits
  - Damaged tracks
  - Missing or broken connections
- Operation of the power block (correctness of voltage levels)
- Output signal control
- Delay between input and output signals
- I^2C communication with temperature and supply current sensors
- Operation of MGMT_STATUS input

Test results discussion

- **Detection of soldering faults, e.g. short circuits, damaged tracks, missing or broken connections**
  - No errors were detected on the basis of the visual inspection.
- **Operation of the power block (correct voltage levels)**
  - The power block works properly
  - Current consumptions are as expected (aprox. 60 mA for 3.3 V voltage domain, and 20 mA for 12 V voltage domain)
  - Output voltage is correct (5.0 V)



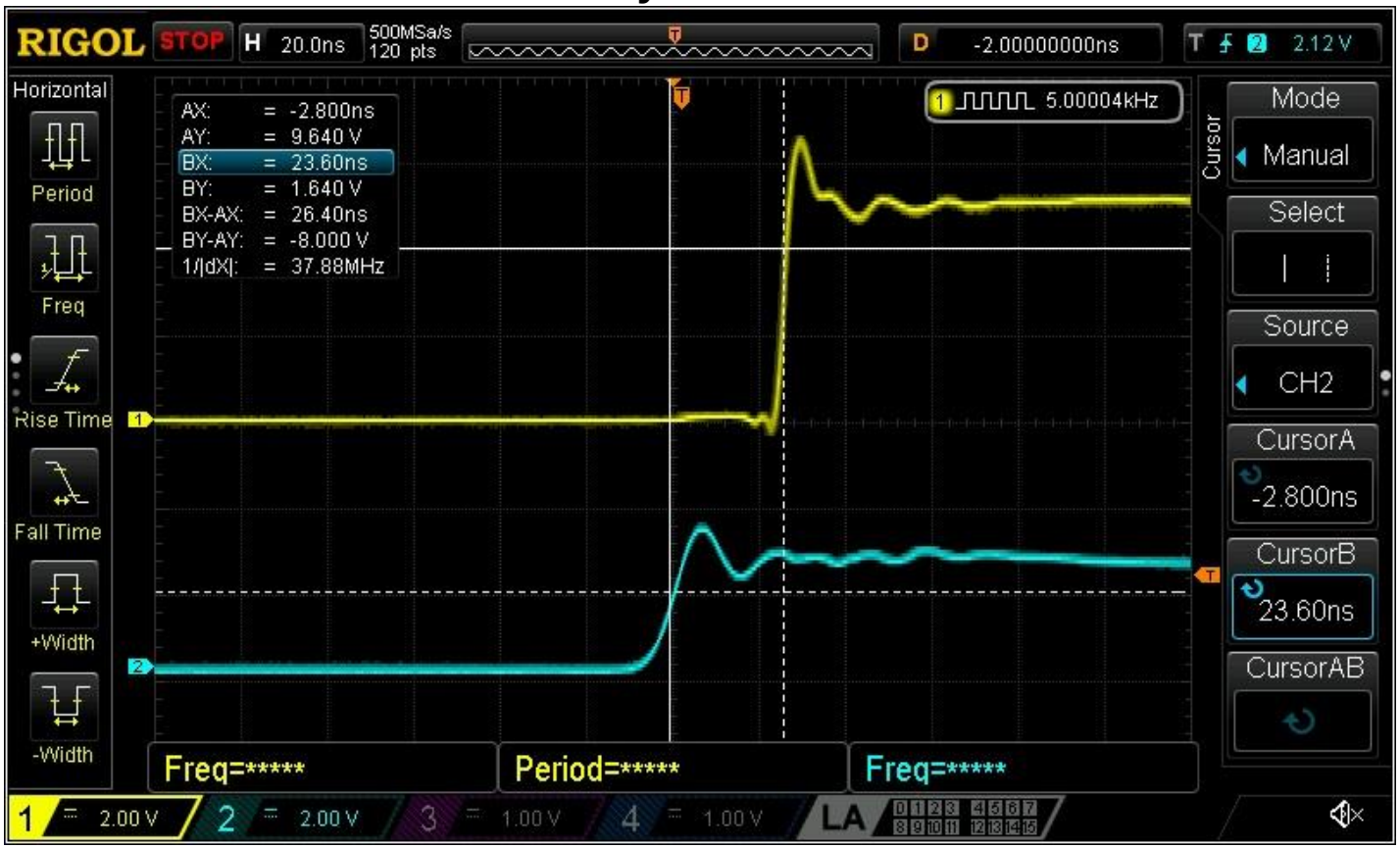
Test results discussion

- **Correctness of output signal control**
  - The correctness of the output signal for 4 frequencies was checked: (5 kHz, 50 kHz, 500 kHz, 5 MHz)

Test results discussion

- **Delay between input and output signals**
  - The delay between input and output signals for 4 frequencies (5 kHz, 50 kHz, 500 kHz, 5 MHz) was measured:

Delay = ~25 ns



Test results discussion

- **I²C communication with temperature and supply current sensors**
  - As part of the tests, the correctness of I²C communication with two sensors was checked:
    - STH31 - Connection with the temperature sensor was established and correct temperature was read.
    - INA219 – Connection with the sensor was established.
- **Operation of MGMT_STATUS input**
  - MGMT_STATUS input operation is correct. When the MGMT_STATUS input is in the low state, all SSA output control signals are in the low state.

Full scale design plans

- The presented solution can be adopted in the final design
- 12 channels are needed in the final design

- Changes in schematic diagrams (duplication of selected blocks)
- PCB project redesign

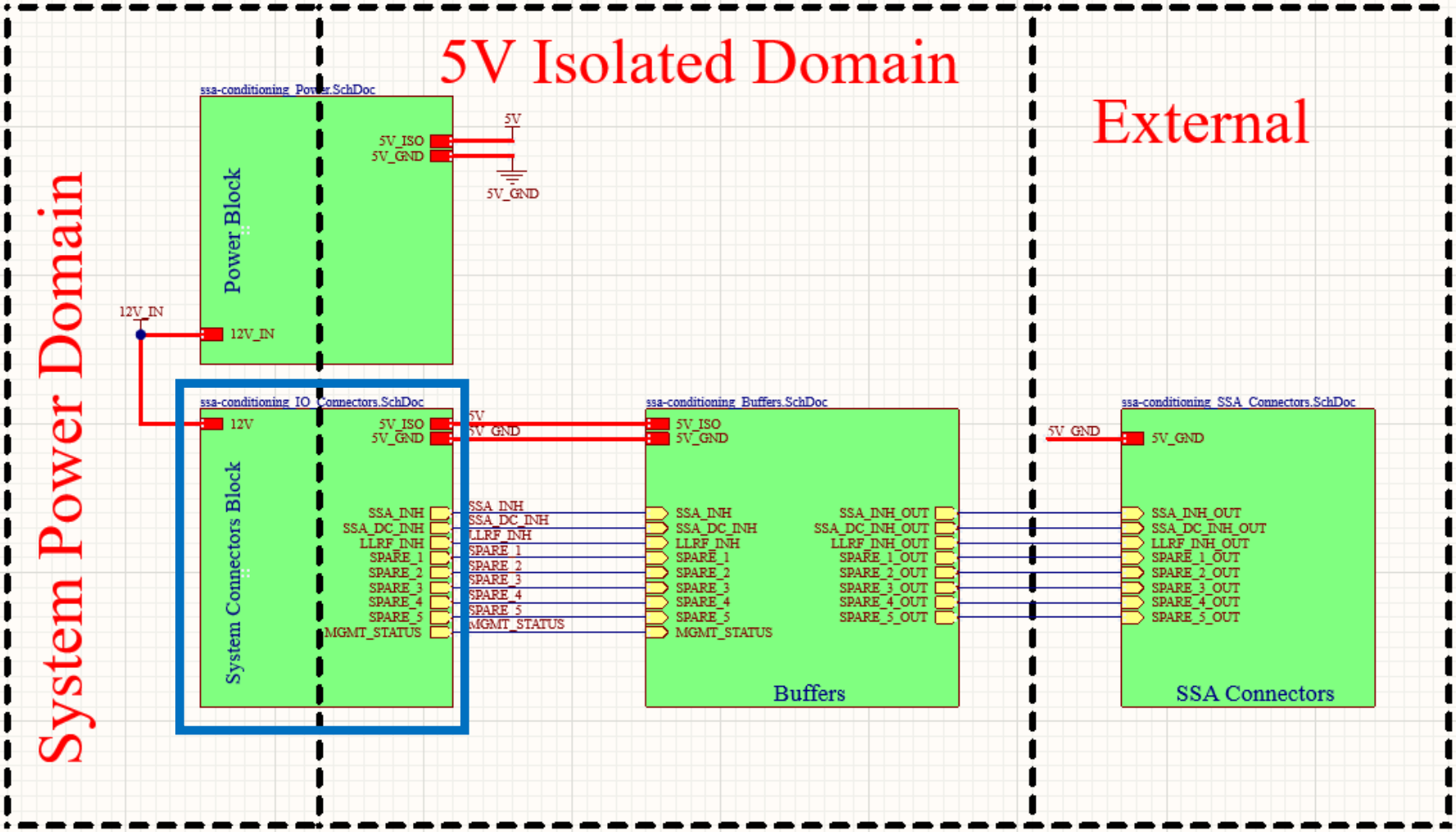
Summary

- Requirements
  - 4 output signals per cavity => 16 output signals per module
  - Response time less then 1 µs
- PoC, implementation and verification
  - PCB supporting 8 output signals
  - 4-layer PCB
  - Correct operation of the power block and output signal control
  - Circuit response time (delay between input and output) is about 25 ns
- Full scale design plans
  - Extending the solution to 12 channels (additional buffers and isolators)

Thank You

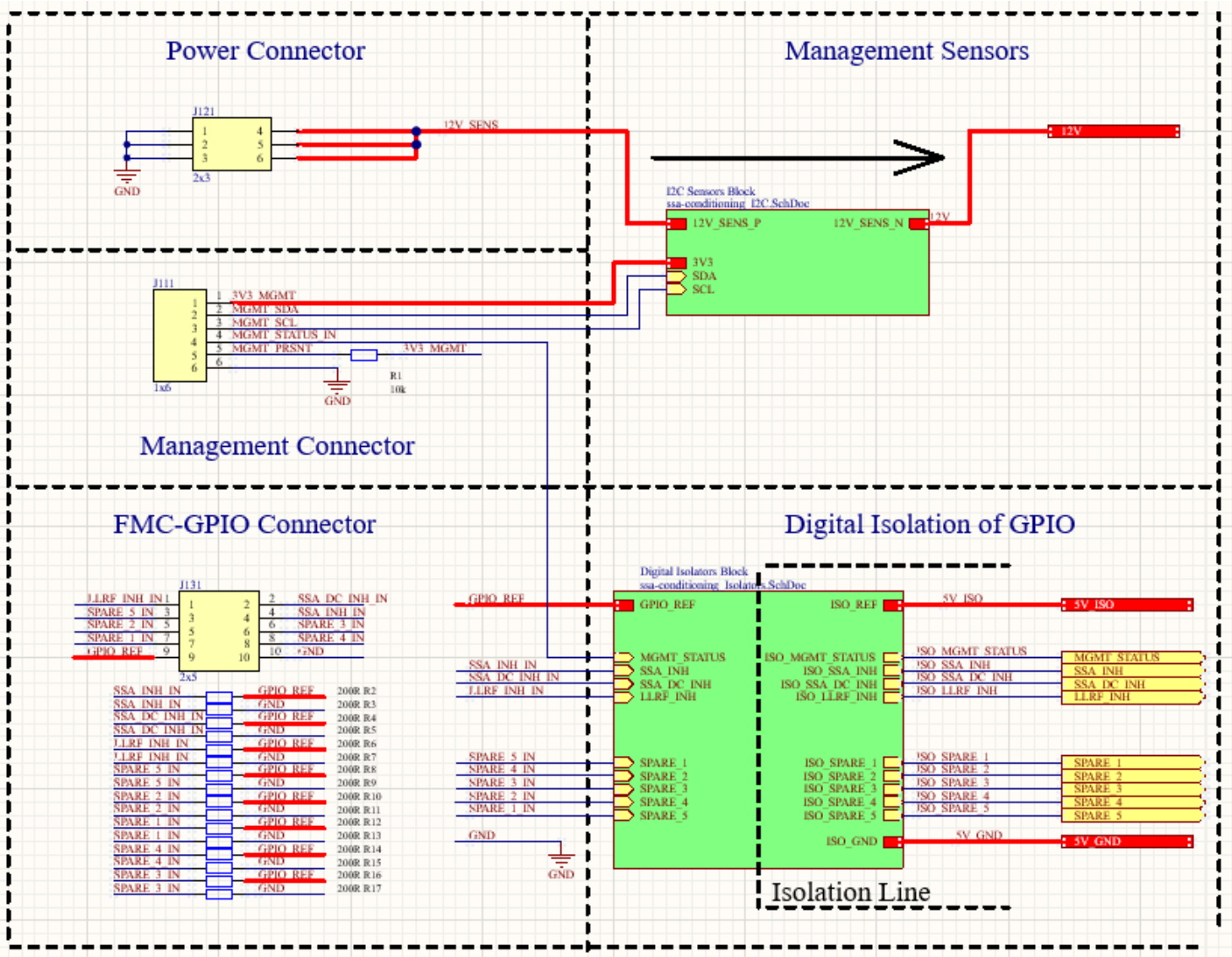
The sub-module design details

- System Connectors Block



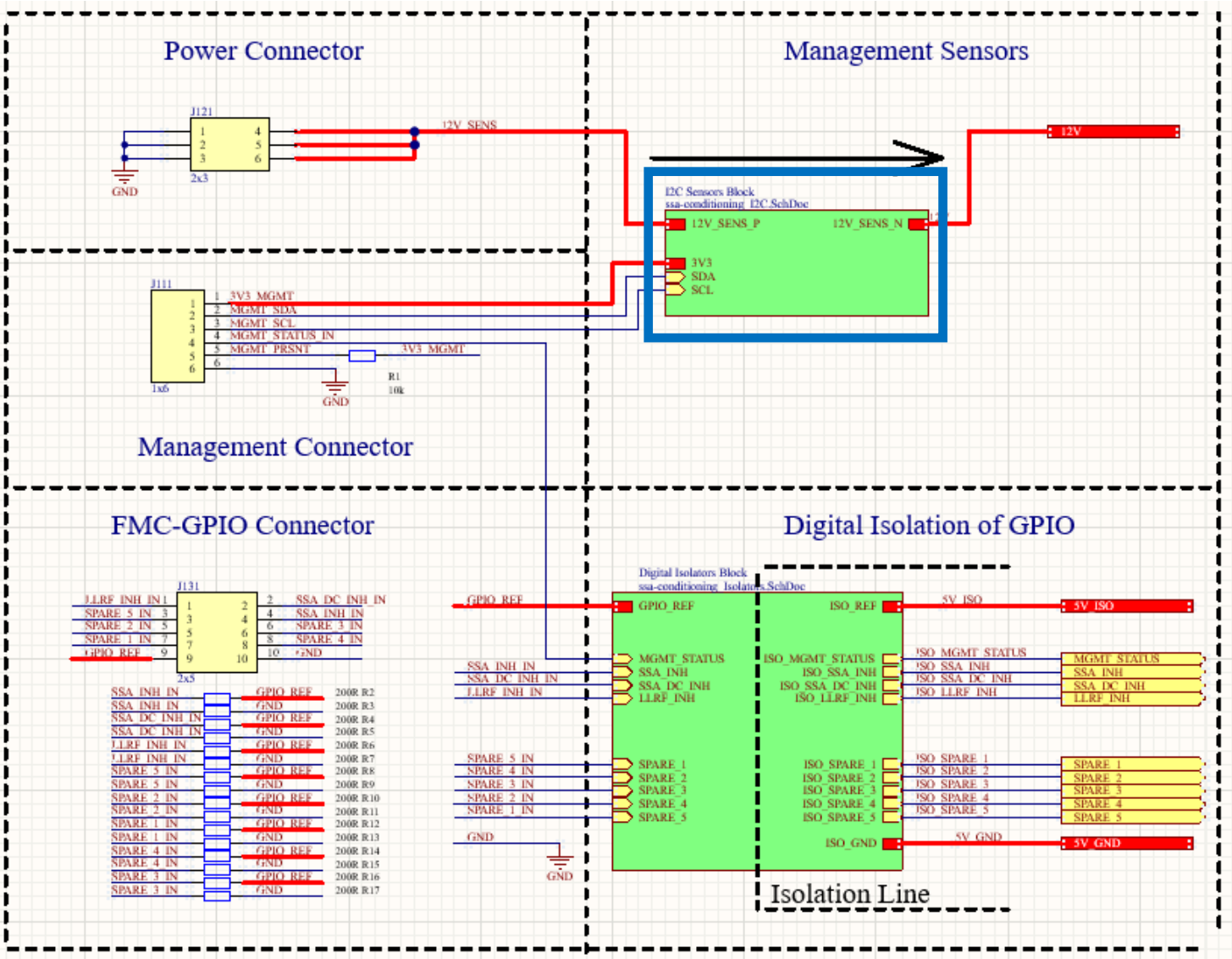
The sub-module design details

System Connectors Block



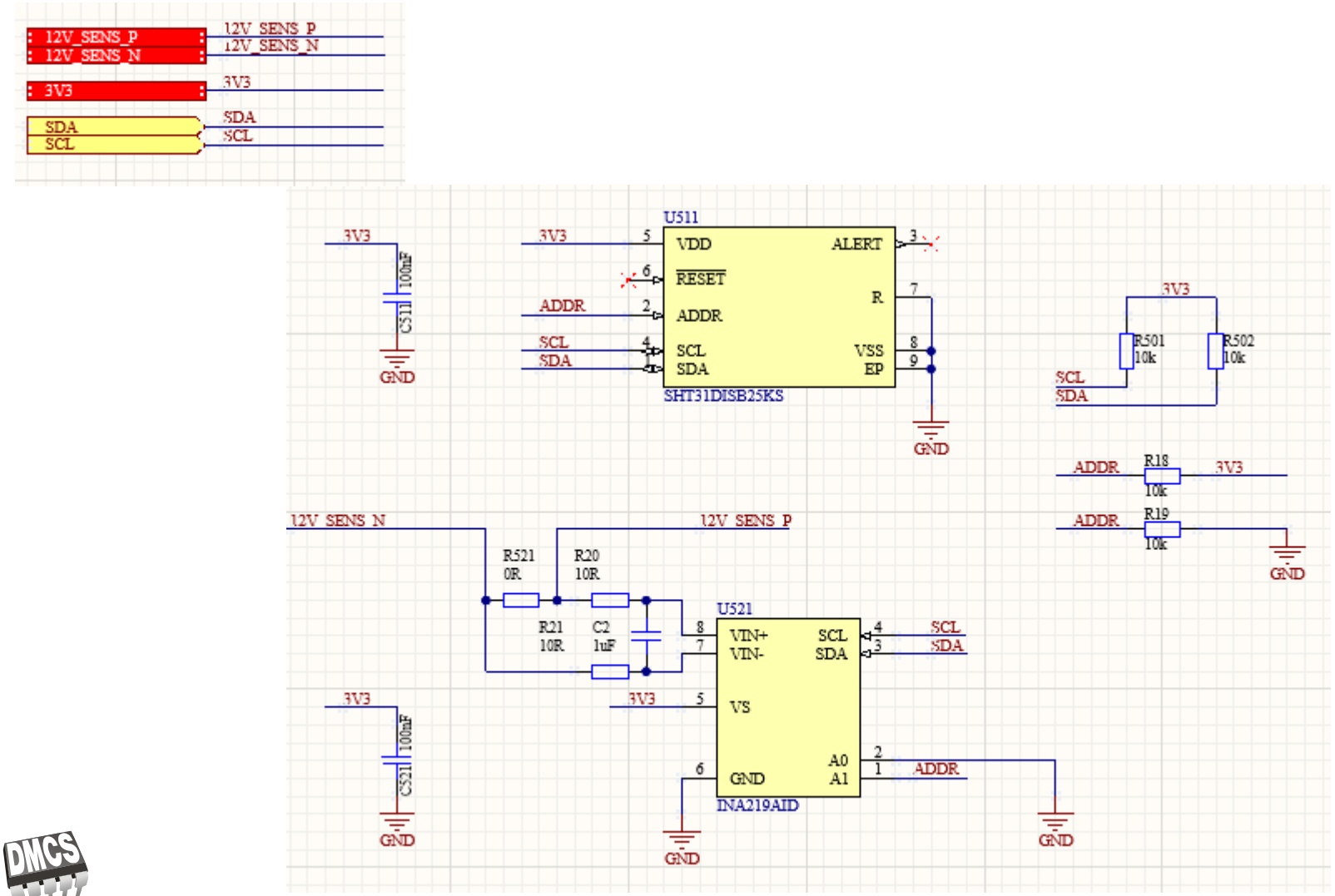
The sub-module design details

Management Sensors



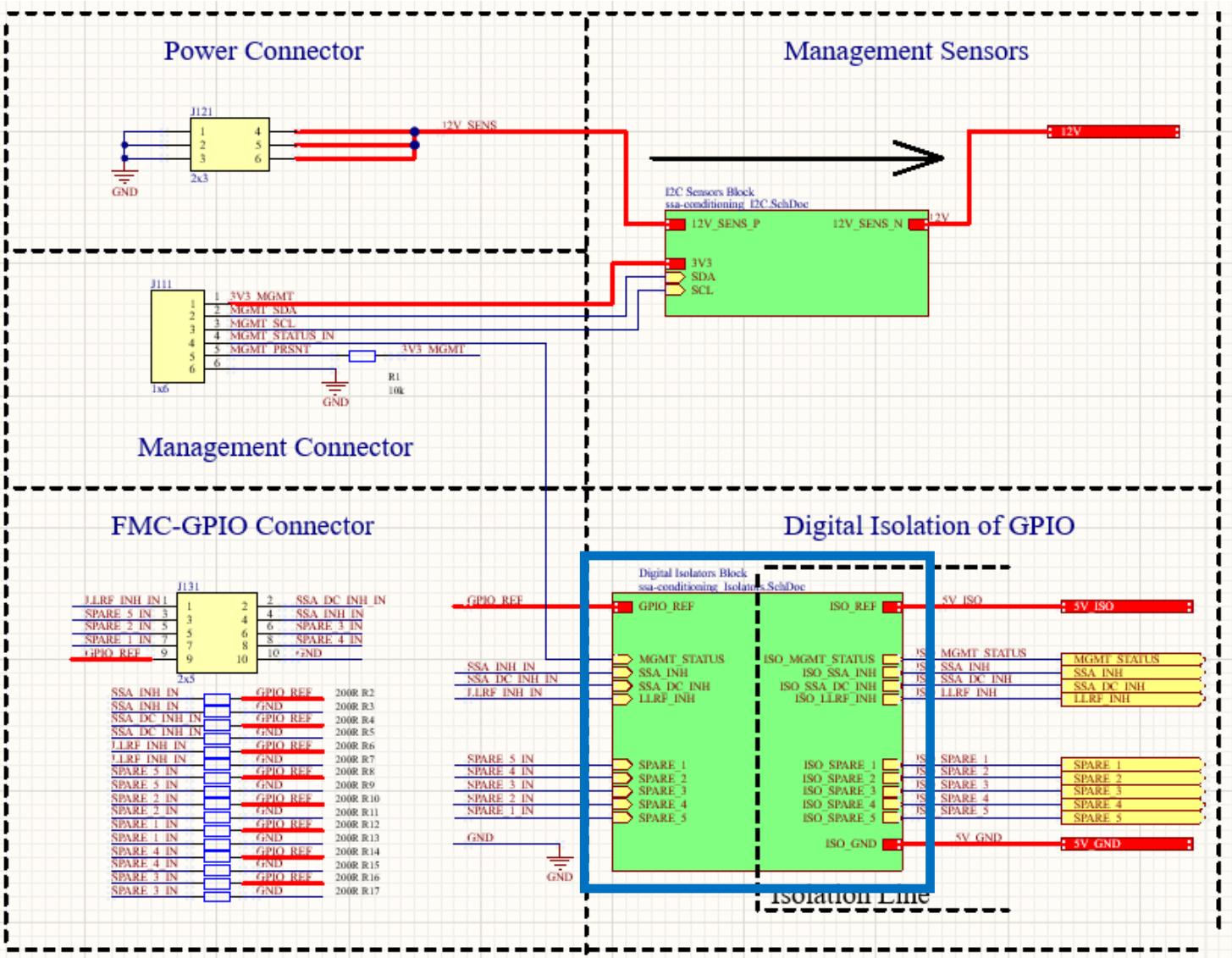
The sub-module design details

Management Sensors Schematic Diagram



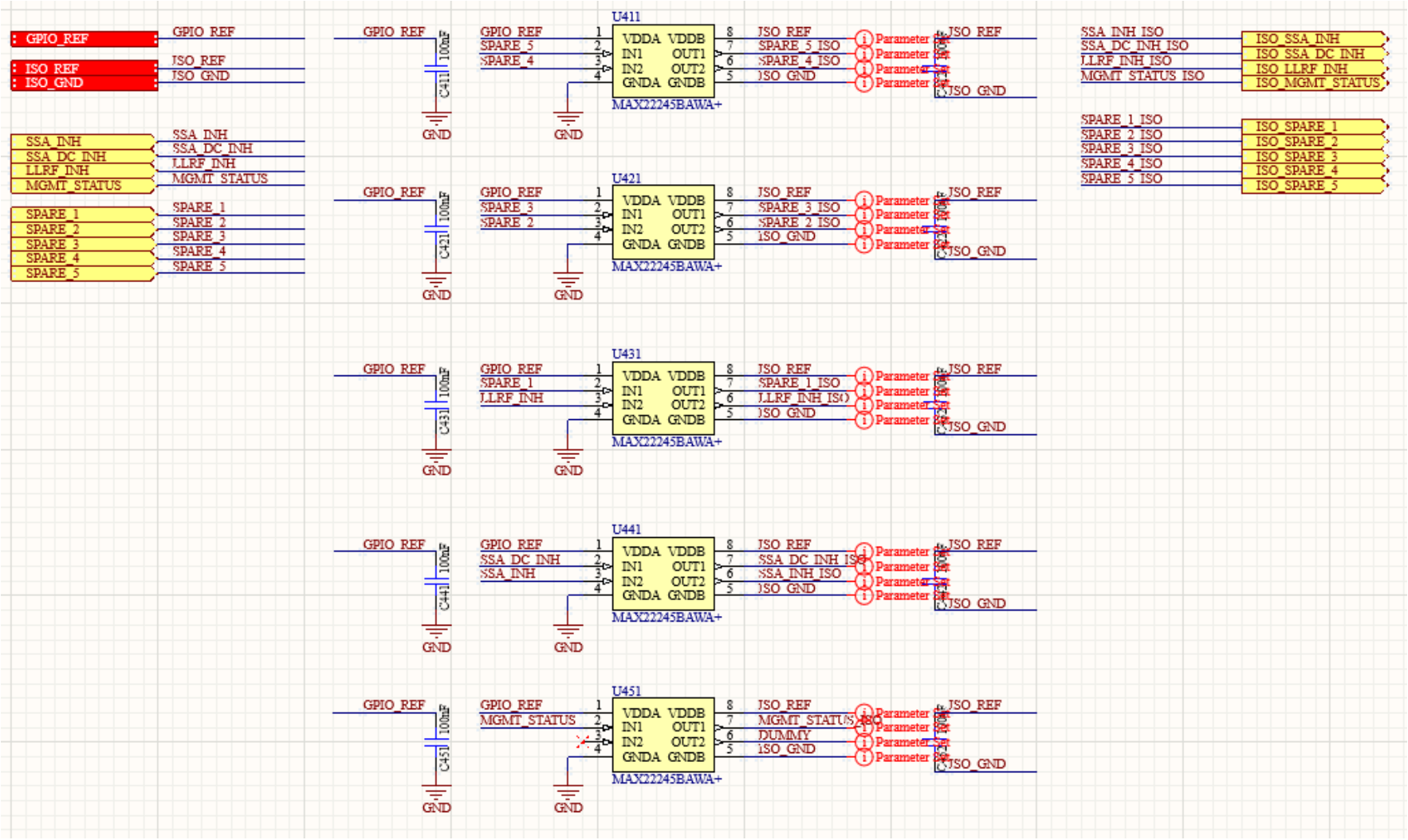
The sub-module design details

Digital Isolation of GPIO



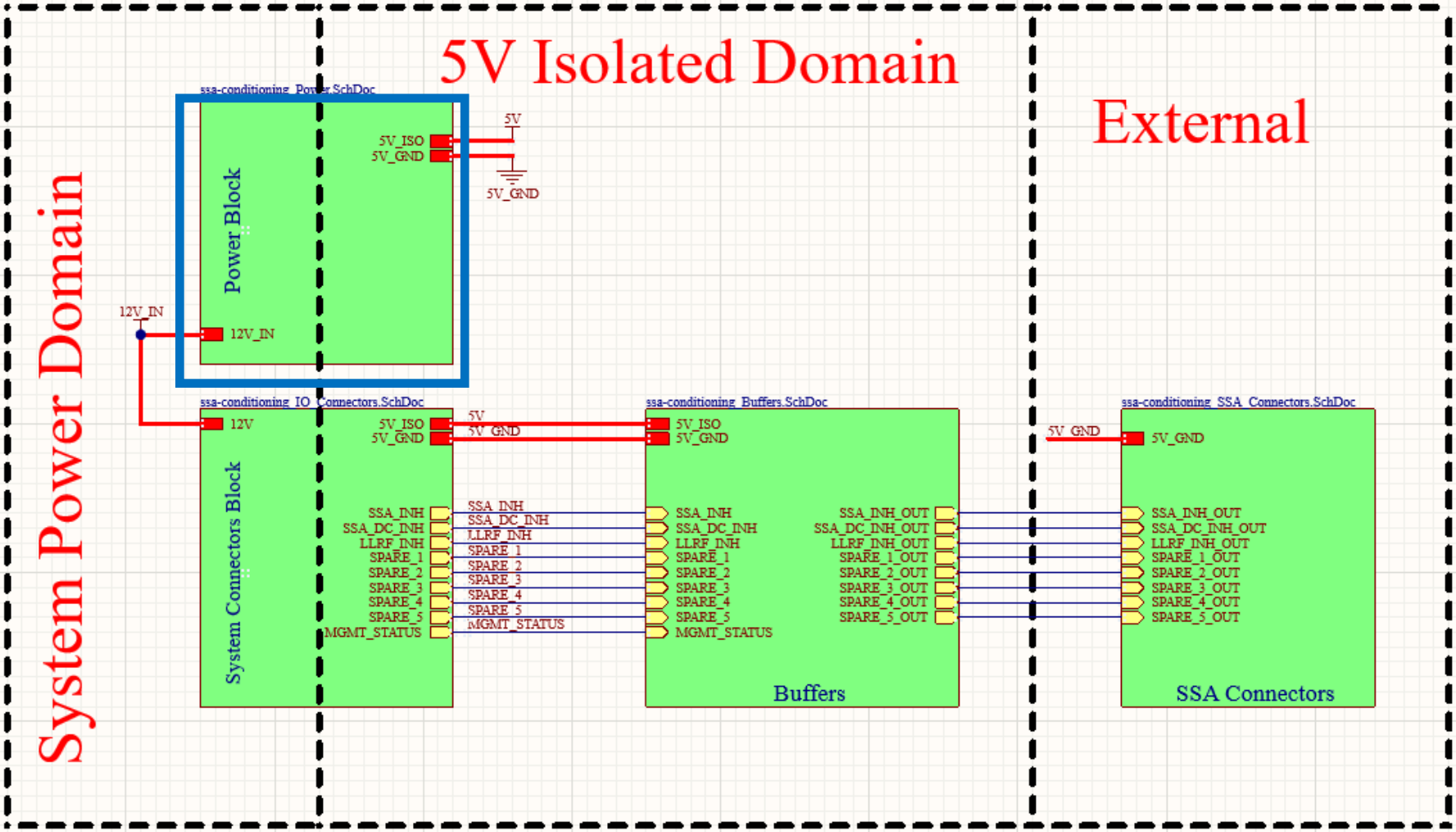
The sub-module design details

Digital Isolation of GPIO Schematic Diagram



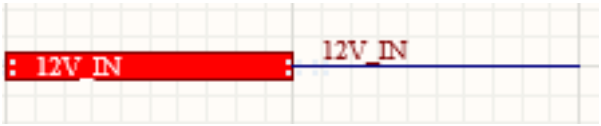
The sub-module design details

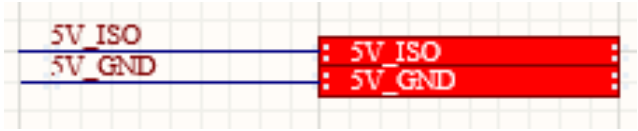
- Power Block

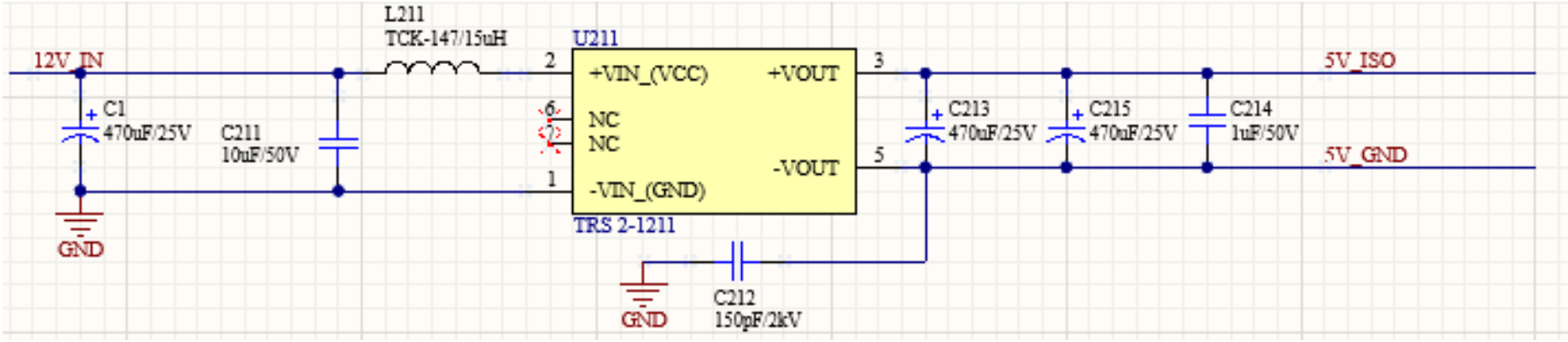


The sub-module design details

Power Block Schematic Diagram

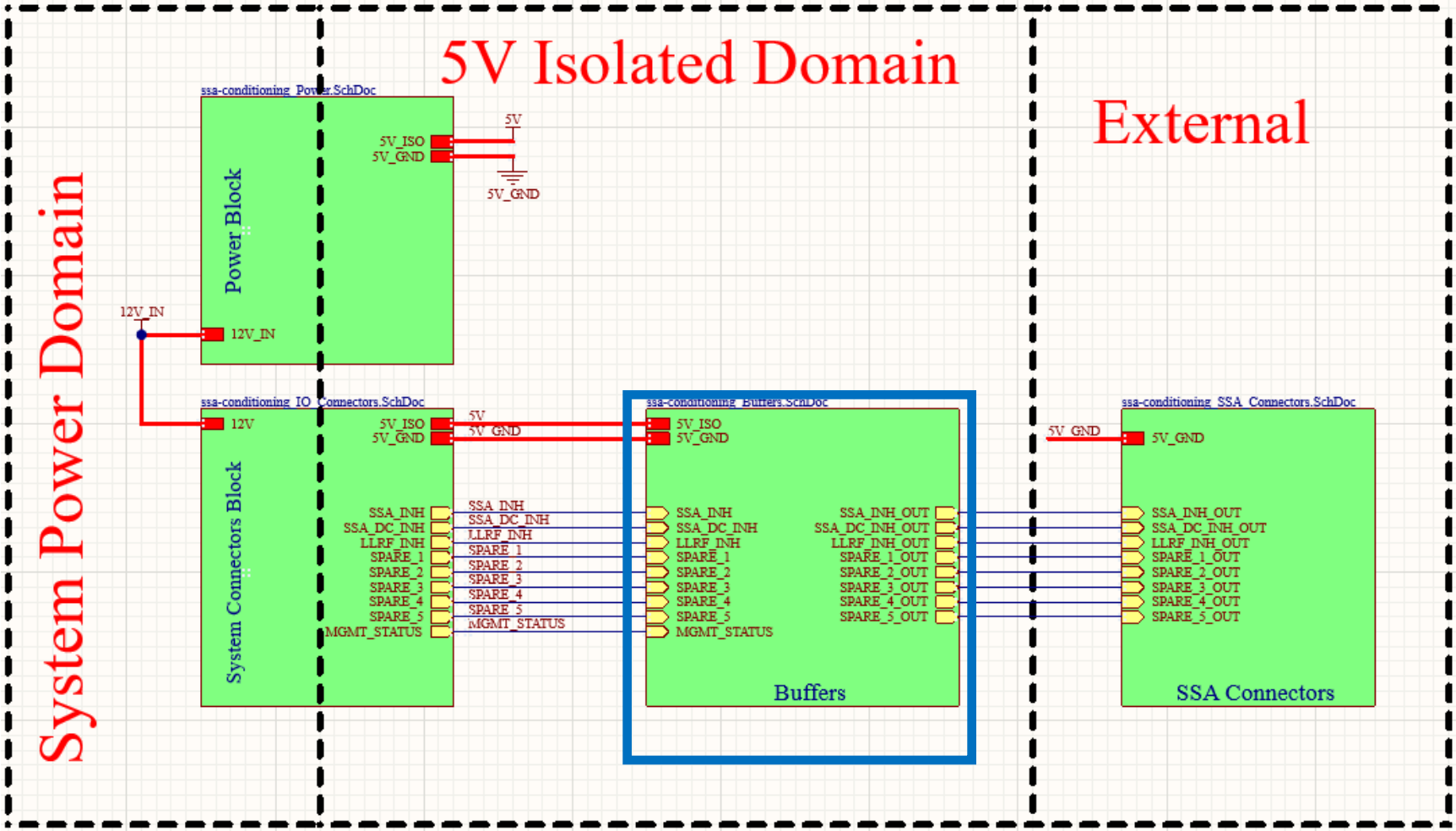






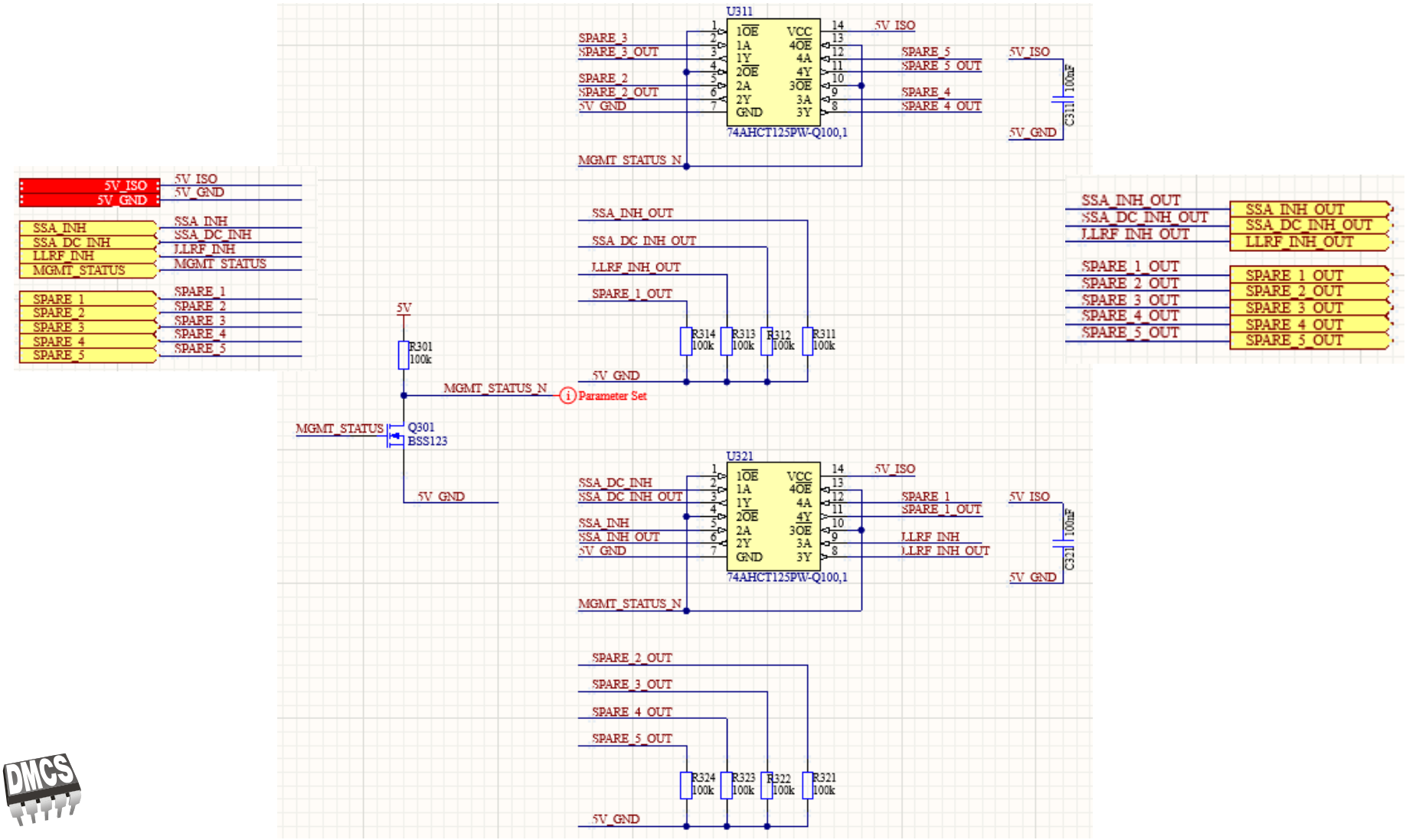
The sub-module design details

Buffers Block



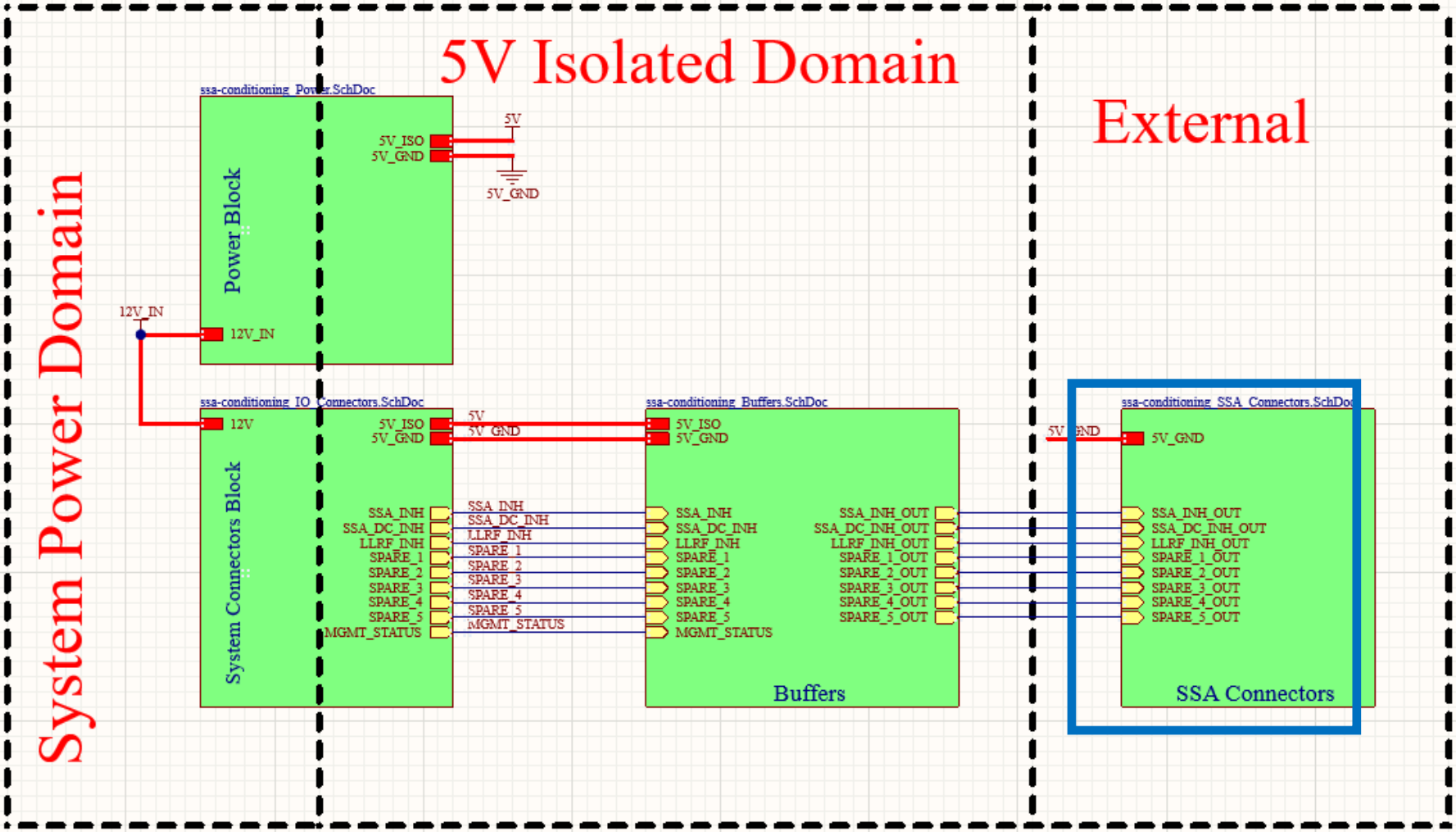
The sub-module design details

Buffers Block Schematic Diagram



The sub-module design details

SSA Connectors Block



The sub-module design details

SSA Connectors Schematic Diagram