Signal Conditioning: Field Emission Probe sub-module

Bartosz Pękosławski & Paweł Marciniak

About us

Bartosz PĘKOSŁAWSKI

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - Projects on machine vibration monitoring – hardware engineer (2006 – 2011)
  - TULCOEMPA – hardware designer (2011 – 2015)
  - SPParTAN – hardware designer (2019 – 2022)
  - FOSREM – hardware designer (2021 – present)

Paweł MARCINIAK

Ph.D. Electrical Engineering

- Role:
  - HW (signal conditioning) designer
- Relevant Experience:
  - INNOREH – software designer (2017 – 2021)
  - SPParTAN – firmware designer (2019 – 2022)
  - ITER – hardware engineer (2021 – 2022)
  - FOSREM – hardware designer (2021 – present)

Agenda

- The FEP module requirements
- The PoC version specification and scope
- The sub-module simulations and design details
- Implementation
- Test results discussion
- Full scale design plans
- Summary

The FEP module requirements

- 1 FEP per cavity/coupler
- transimpedance amplifier used
- bias up to 45 V
- read back up to 10 mA
- trip levels set under software control
- 2 MSPS waveform capture
- < 10 μA resolution
- < 1 μs RFPI response time

The PoC version specification and scope

Two FEP channels

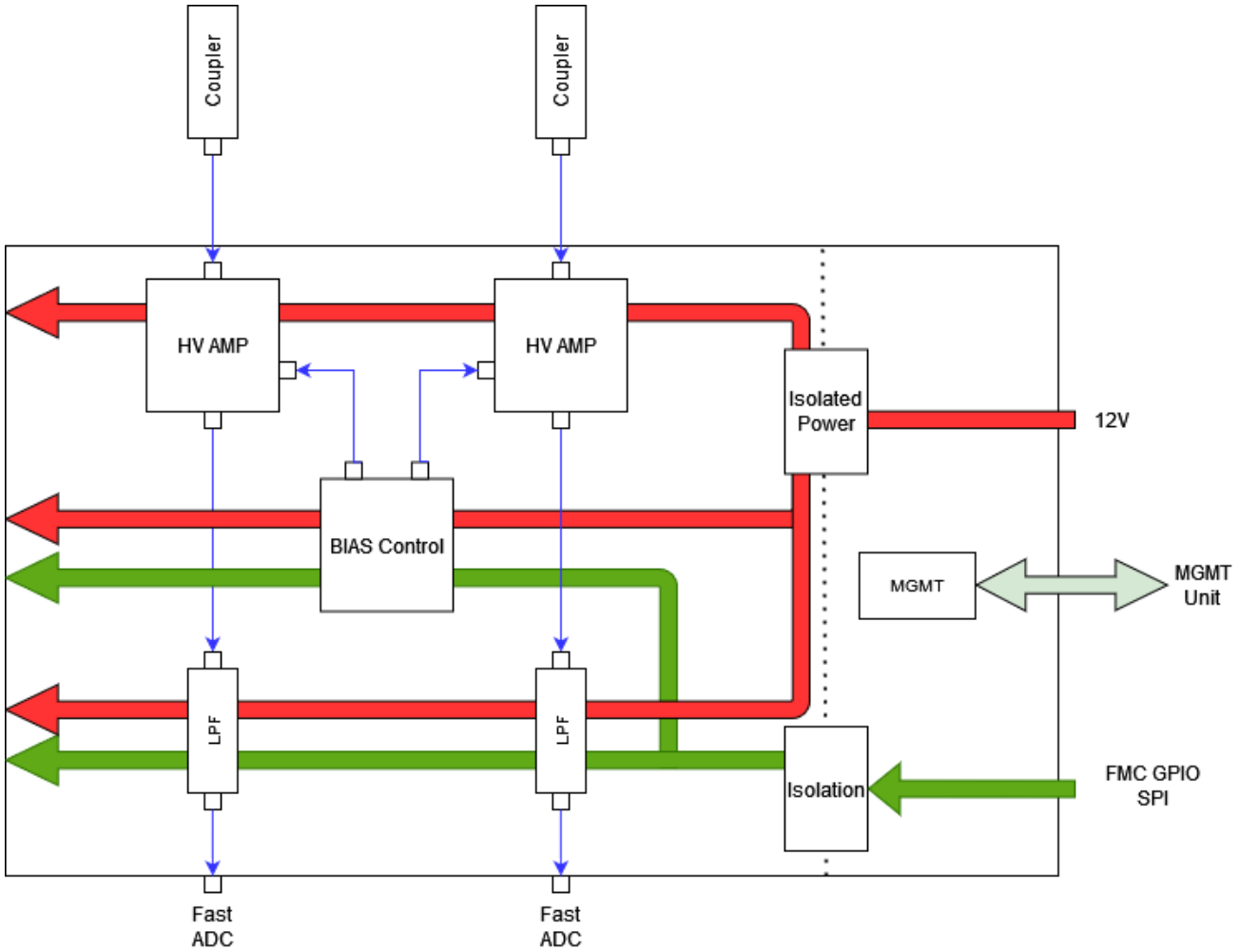
Bias voltage adjustable via SPI up to 45 V

Management Block:

- I²C communication with Raspberry PI
- Current measurement
- Temperature and humidity measurements

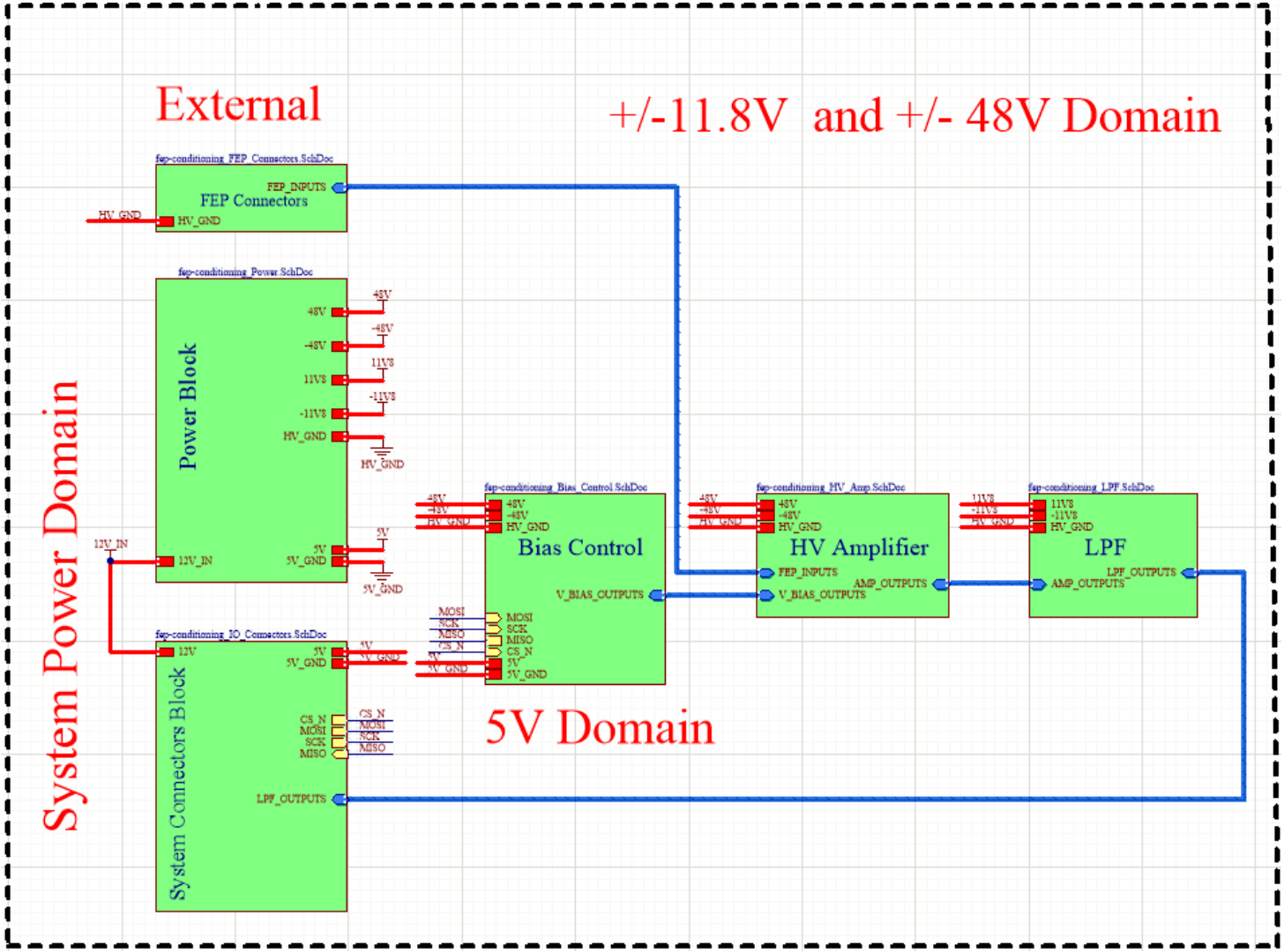
The sub-module design details

Conceptual diagram



The sub-module design details

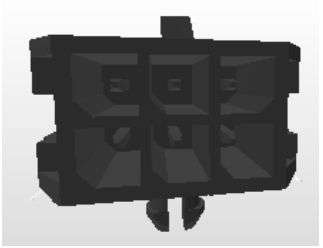
Block diagram



The sub-module design details

System Connectors Block

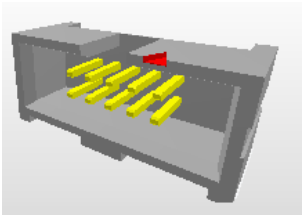
- Power Connector (12 V)



- MGMT Connector (I^2C) and sensors

- Output Signal Connectors (MMCX)

- FMC GPIO Connector (SPI)



- Isolation of SPI signals based on MAX22245BAWA+ and MAX22246CAWA+ digital isolators (2 channels, 7 ns delay, up to 25 / 200 Mbps, 868 V_{RMS} continous / 5 kV_{RMS} 60s / 12.8 kV_{RMS} surge galvanic isolation)

The sub-module design details

Power Block

- 12V → 5V SMPC module Traco Power TRS 2-1211 (isolated, 9-18 V input, max. 2 W output power, 80% efficiency, 1.6 kV isolation)
- 12V → ±12 V SMPC module Traco Power TEN-3-1222N (isolated, 9-18 V input, max. 3 W output power, 84% efficiency, 1.6 kV isolation)
- EN 55032 class A external filters at the inputs for radiated and conducted emission
- LT3032 dual, low noise, positive and negative low dropout (300 mV) voltage linear regulator with 150 mA maximum output current (±12 V → ± 11.8 V)
- Noninverting 12V → 48V SMPC based on LT8580 (0.2 – 1.5 MHz, UVLO, soft-start, 1 A/65 V switch, input voltage range 2.55 – 40 V)
- Inverting, dual inductor 12V → –48 V SMPC based on LT8580

The sub-module design details

FEP Connectors Block

- SMA Connectors

Two SMAJ48A TVS diodes (56.1 V, 5.2 A) + 10 kΩ serial resistors at each input line

Bias Control

- MCP48FEB24-20E quad, 12-bit resolution buffered voltage output Digital-to-Analog Converters (DAC), with volatile user memory
- MAX6138 bandgap voltage reference (4.096V),
  Operating Current Range: 60 µA to 15 mA, 28 μV_{RMS} Output Noise (0.01 to 10 kHz)
- Noninverting voltage amplifier with 10 V/V gain based on LTC6090 OPAMP
  (max. 50 pA input bias current, ±4.75 to ±70 V supply voltage range, 12 MHz GBW,
  21 V/µs slew rate, 3.5 μV_{P-P} Output Noise (0.1 to 10 Hz))

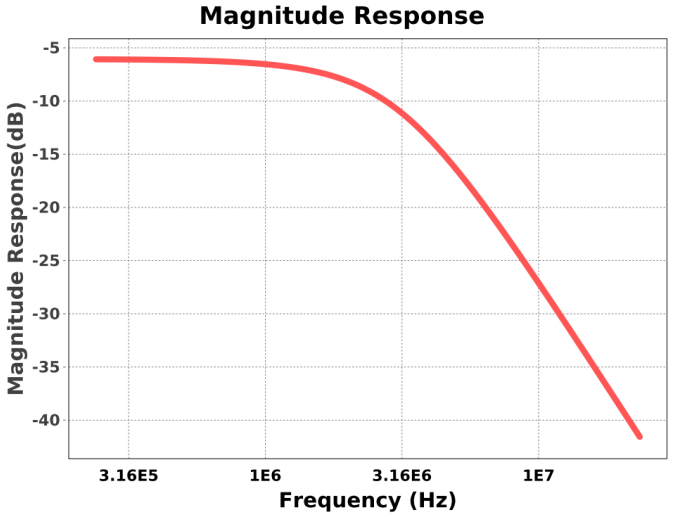
The sub-module design details

HV Amplifier

- Transimpedance amplifier with 470 V/A gain based on LTC6090 OPAMP (max. 50 pA input bias current, ±4.75 to ±70 V supply voltage range, 12 MHz GBW, 21 V/µs slew rate, 3.5 μV_{P-P} Output Noise (0.1 to 10 Hz))
- Inverting voltage amplifier with –1 V/V gain based on LTC6090 OPAMP with ±48 V supply voltage

LPF Block

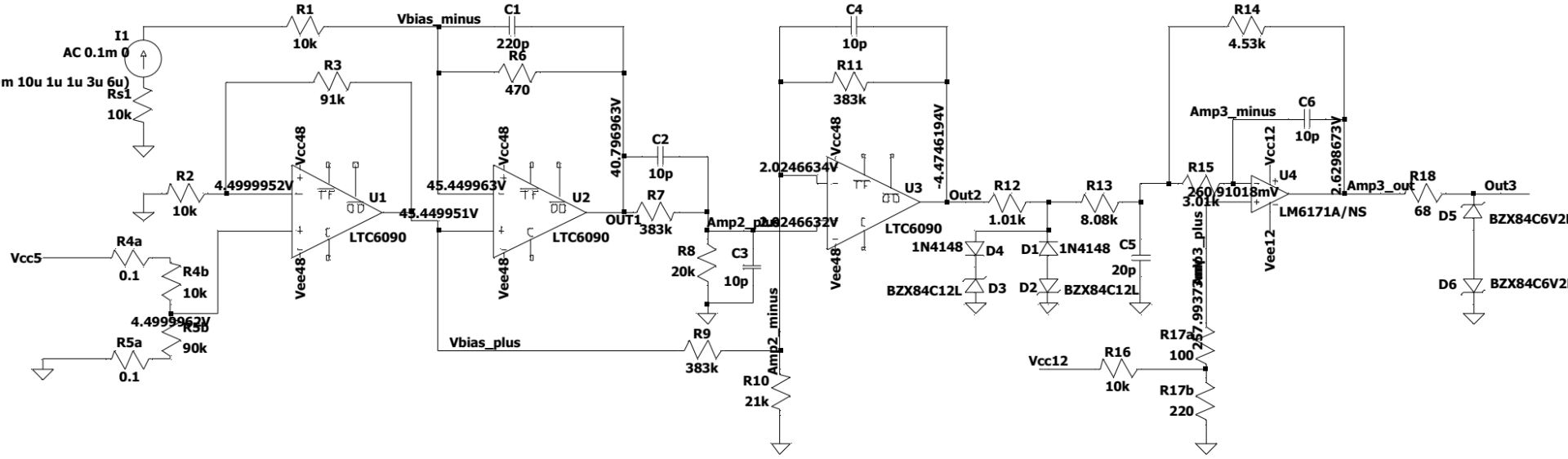
- Bessel LPF (Sallen-Key topology)
  - G = 0.5 V/V
  - f_{-3dB} = 2.4 MHz
  - G(21.4 MHz) = – 40 dB
  - Group delay = 90 ns
  - GBW required = 88.2 MHz



- LM6171BIM OPAMP (100 MHz Unity Gain Bandwidth , Input Voltage-Noise Density 12 nV/√Hz, Slew Rate of 3.6 kV/µs) with ± 12 V supply voltage and I/O clamp circuits

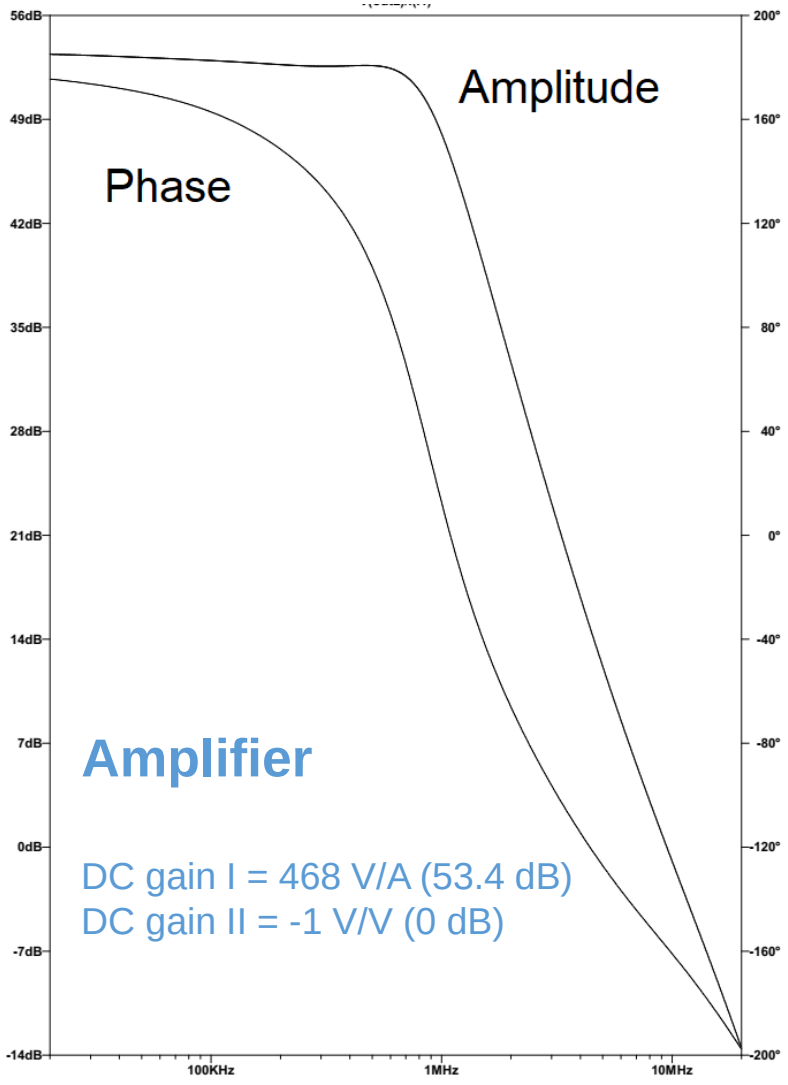
The sub-module simulations and design details

- Signal conditioning path simulated in LTSpice – simulated circuit



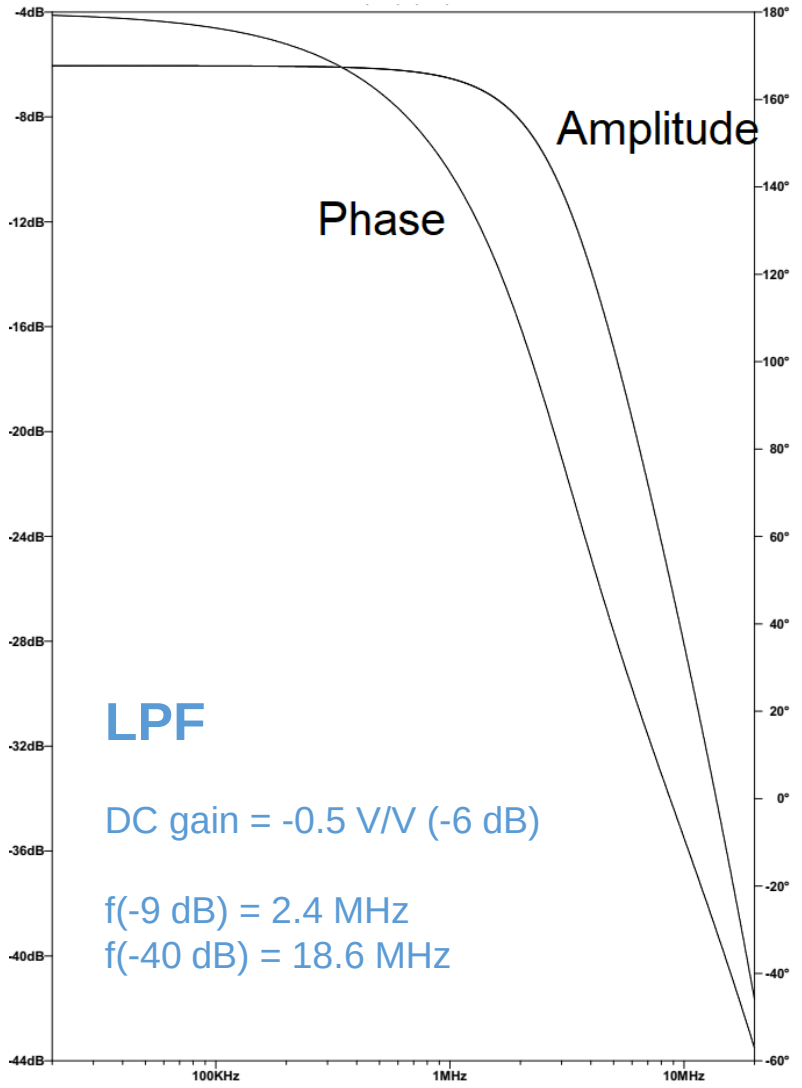
The sub-module simulations and design details

- Signal conditioning path simulated in LTSpice – AC analysis



Amplifier

DC gain I = 468 V/A (53.4 dB)
DC gain II = -1 V/V (0 dB)



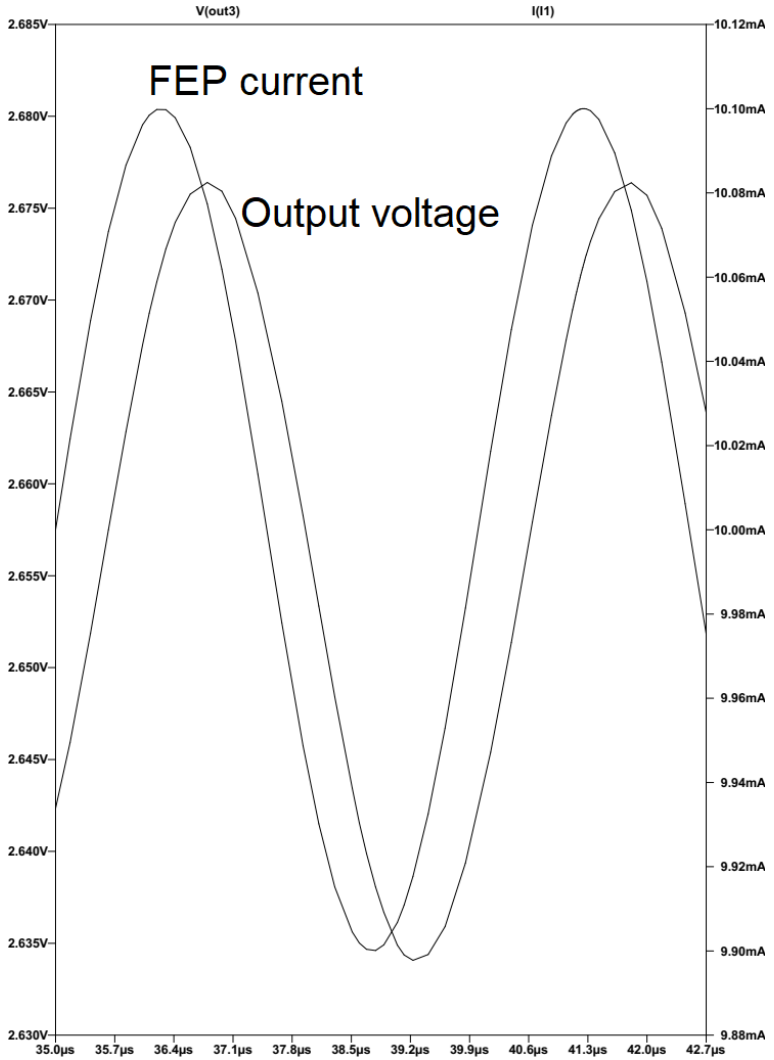
LPF

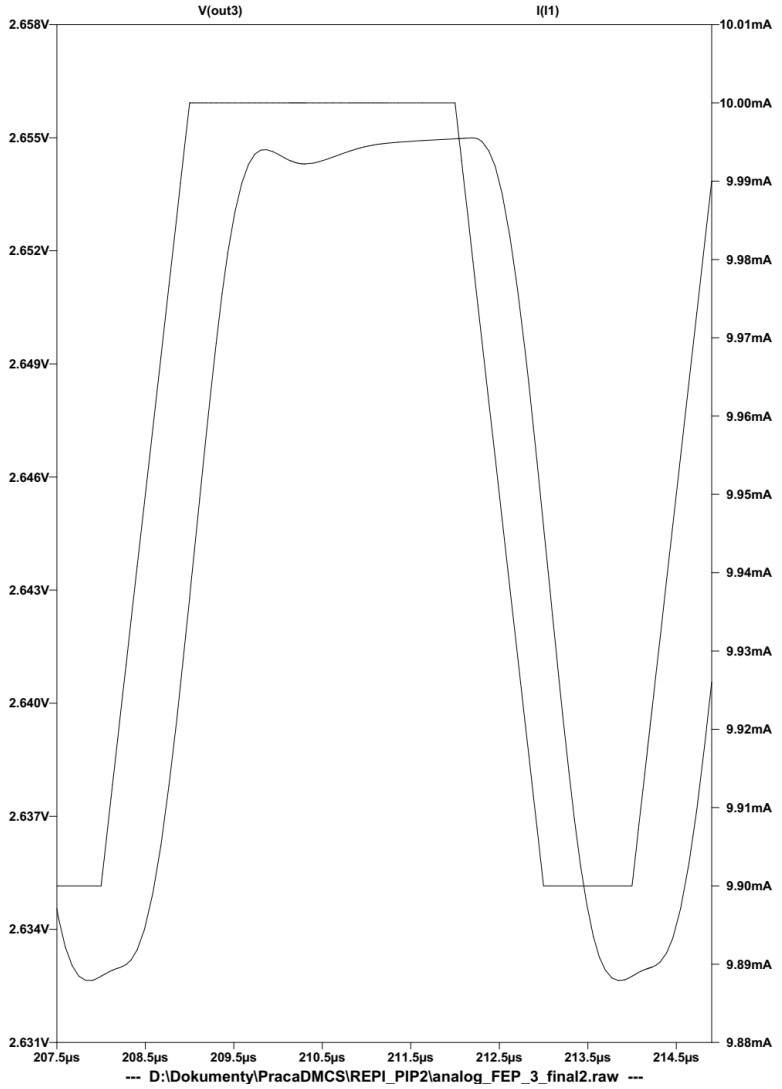
DC gain = -0.5 V/V (-6 dB)

f(-9 dB) = 2.4 MHz
f(-40 dB) = 18.6 MHz

The sub-module simulations and design details

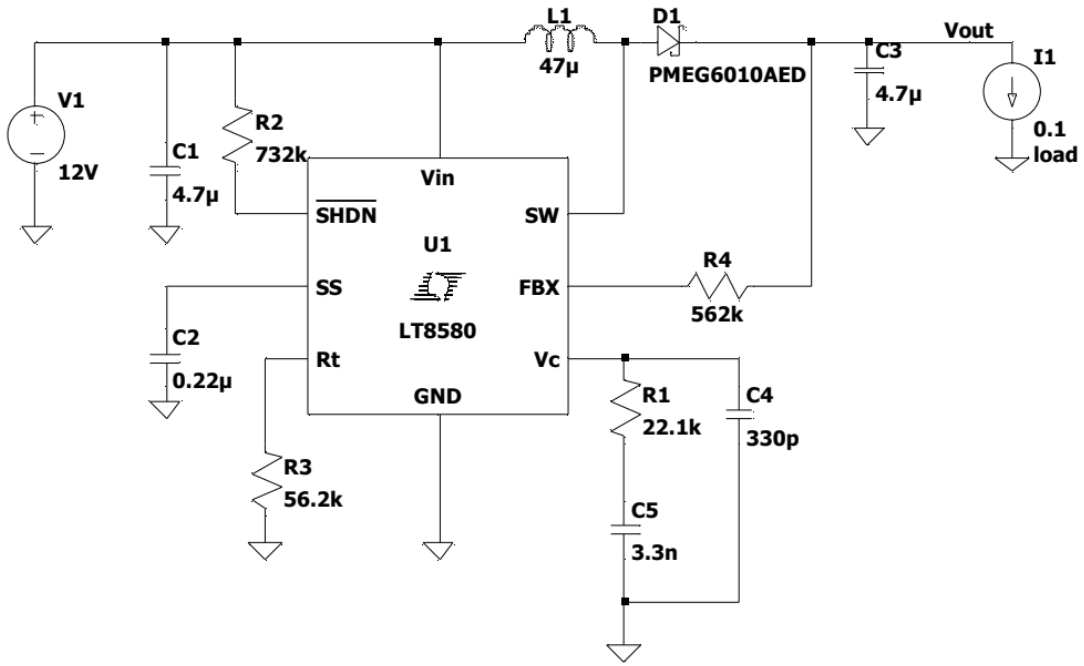
- Signal conditioning path simulated in LTSpice – transient analysis





The sub-module simulations and design details

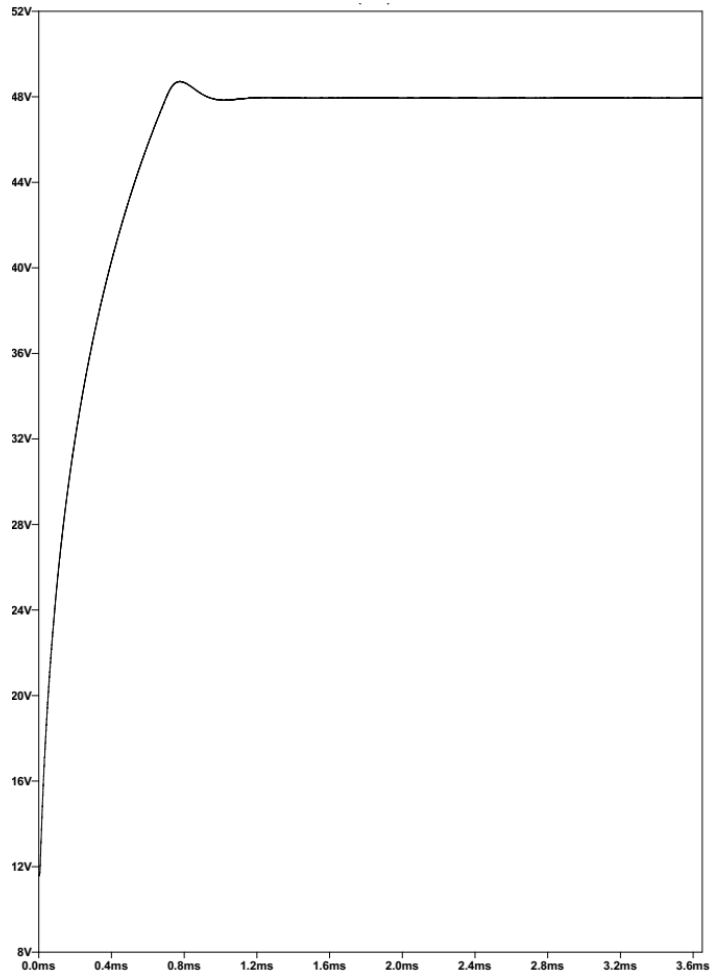
- 12 V to +48 V SMPC simulated in LTSpice – simulated circuit



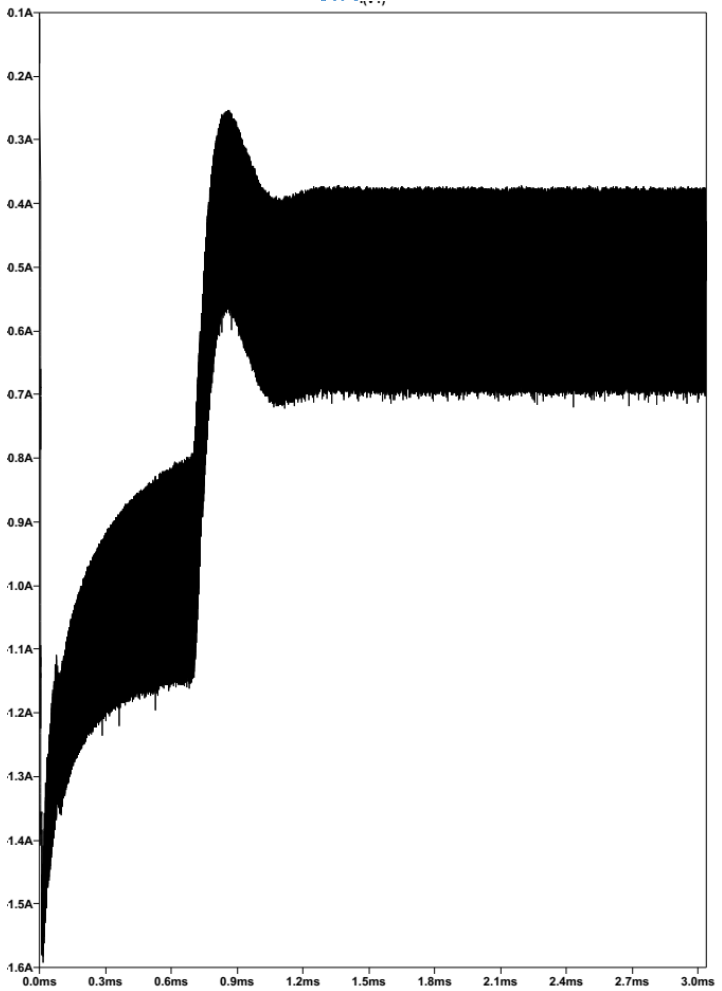
The sub-module simulations and design details

- 12 V to 45 V SMPC simulated in LTSpice – simulation results

V_{OUT}

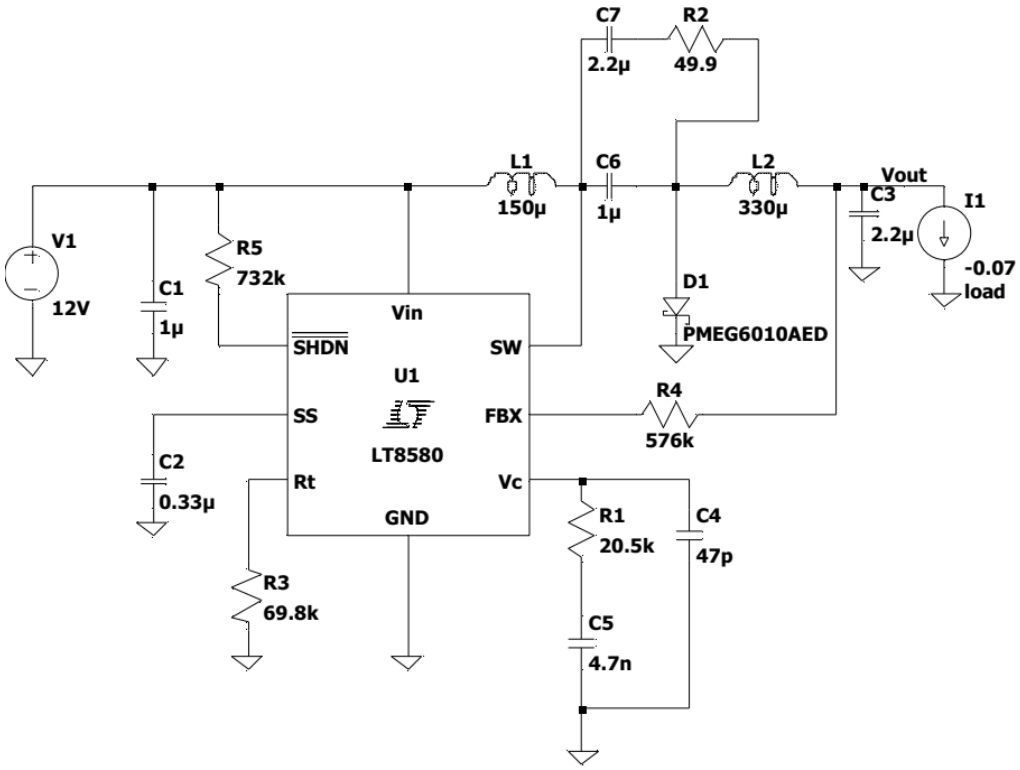


I_{IN}



The sub-module simulations and design details

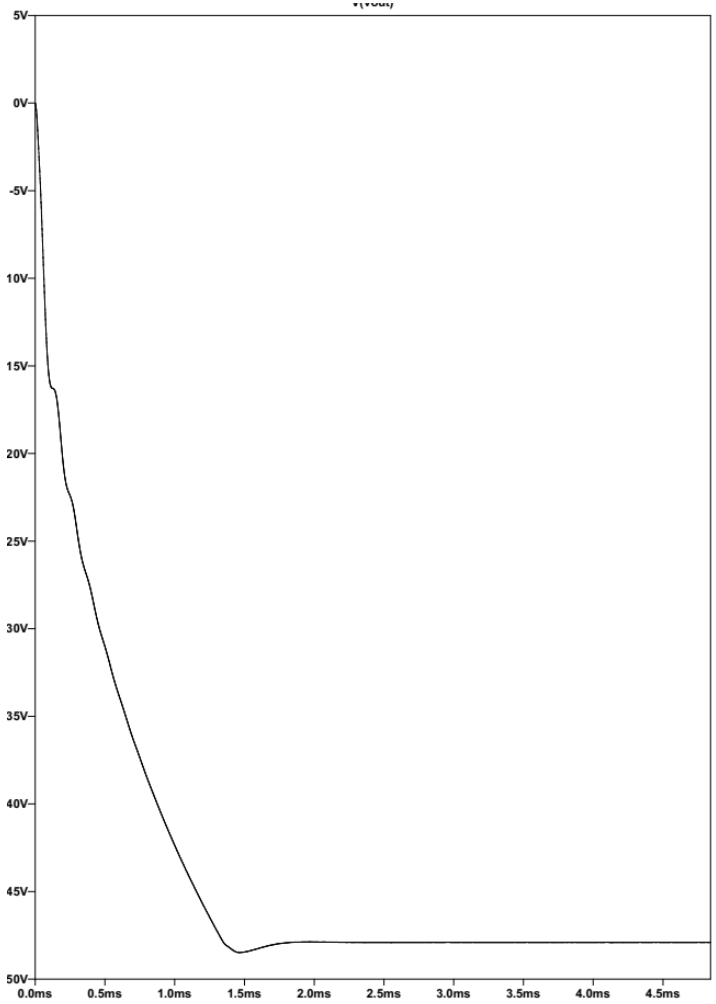
- 12 V to –48 V SMPC simulated in LTSpice – simulated circuit



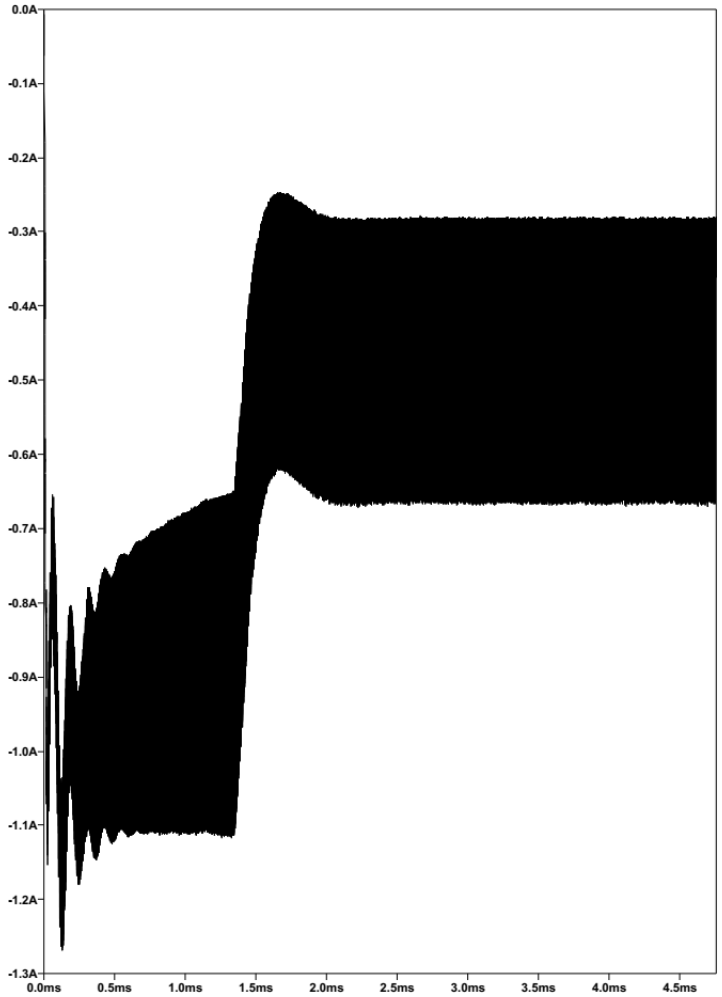
The sub-module simulations and design details

- 12 V to –45 V SMPC simulated in LTSpice – simulation results

V_{OUT}

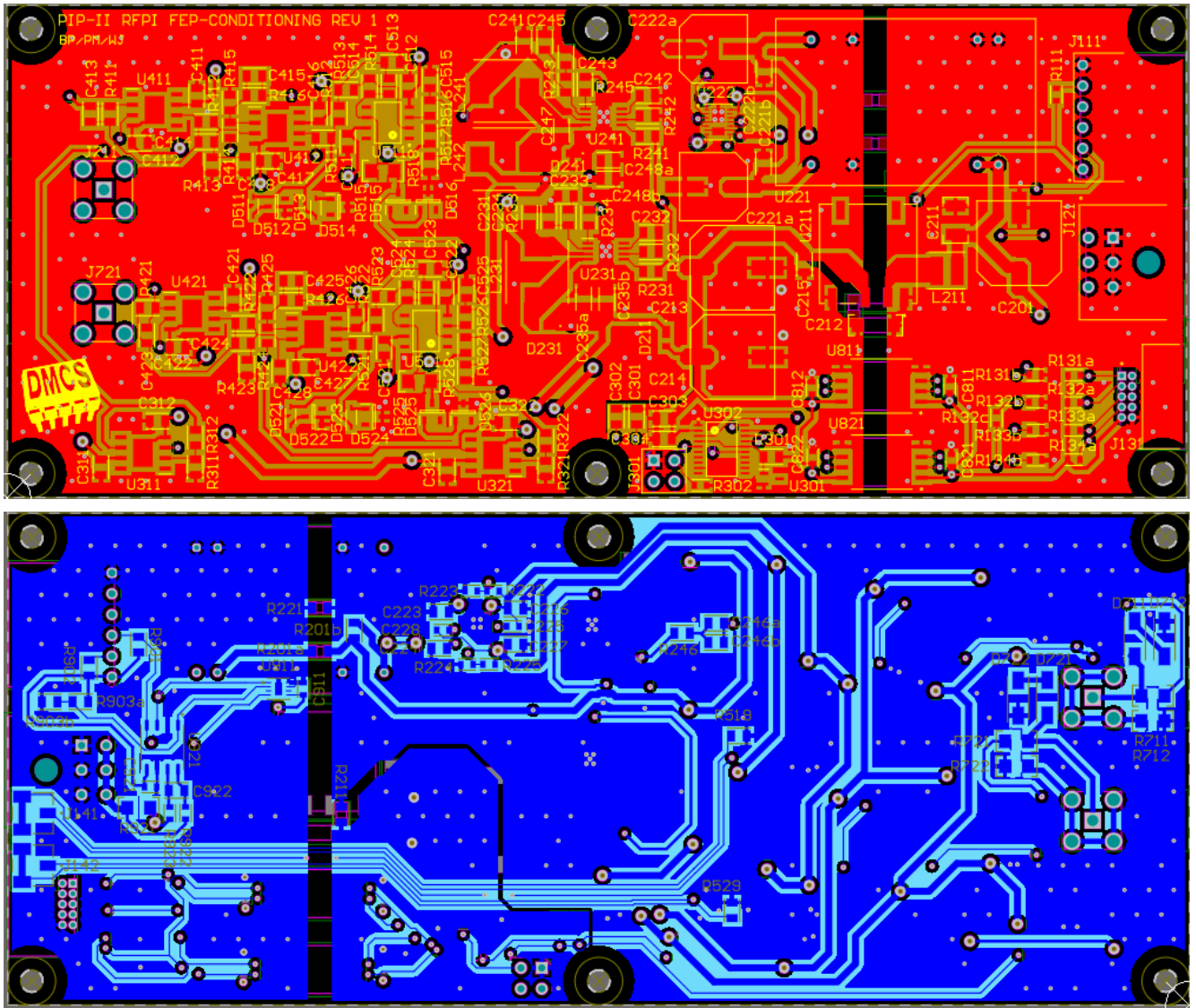


I_{IN}



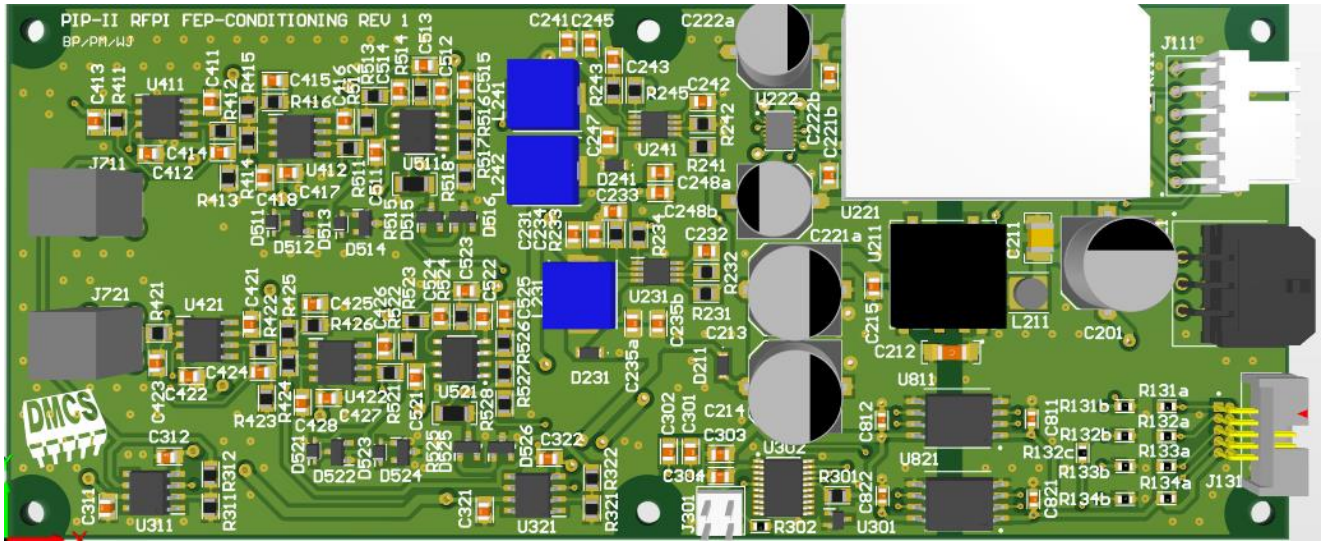
Implementation

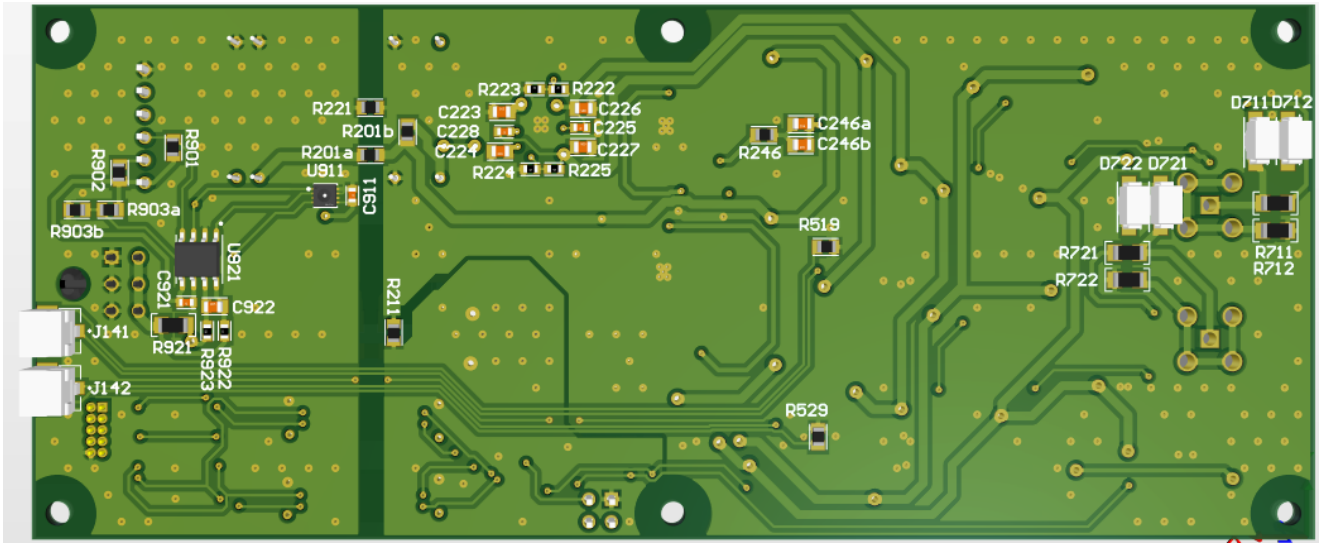
4-layer PCB, dimensions: 144 mm x 60 mm



Implementation

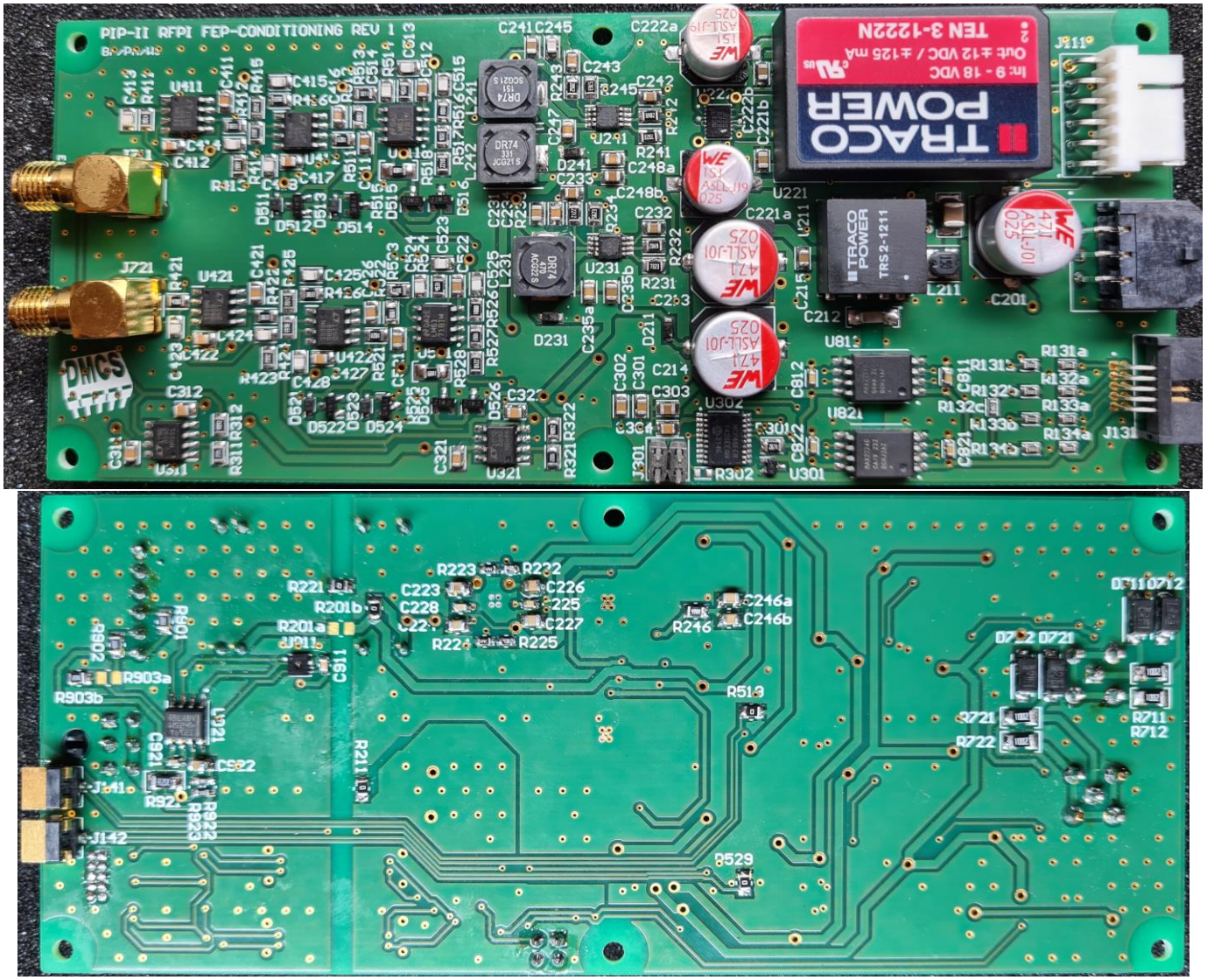
3D model





Implementation

Real view



Test results discussion

- Detection of soldering faults (partially manual soldering)
  - Short circuits
  - Damaged tracks
  - Missing or broken connections
- Operation of the power block and input bias (correctness of voltage levels)
- Output signal conditioning
- Delay between input and output signals
- I^2C communication with temperature and supply current sensors

Test results discussion

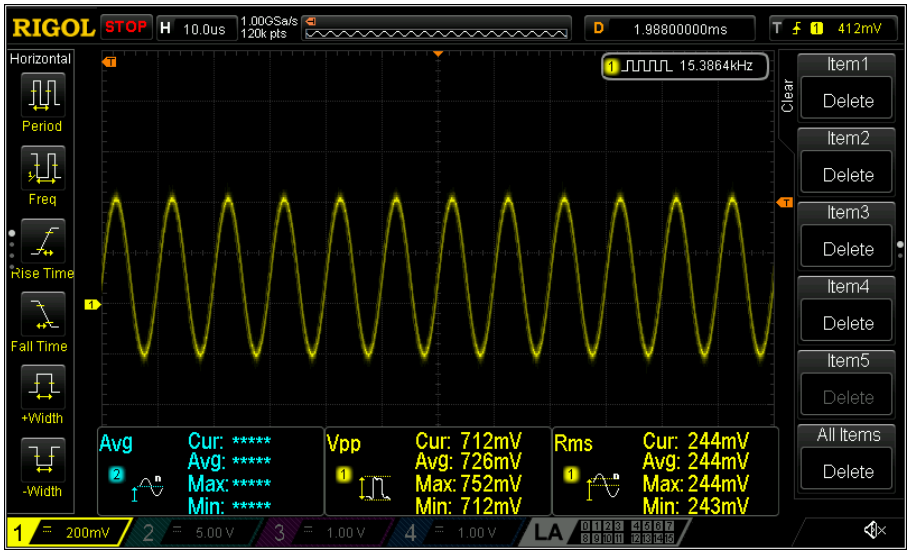
- **Detection of soldering faults, e.g. short circuits, damaged tracks, missing or broken connections**
  - Minor errors were detected on the basis of the vision analysis and corrected.
- **Operation of the power block (correct voltage levels)**
  - The power block works properly
  - Current consumptions are as expected (260 mA for 12 V voltage domain)
  - Output voltages are correct

Test point	Value [V]
5V SMPC output	4.986
±12V SMPC outputs	+11.98/-12.00
LDO outputs	+11.62/-11.84
±48V SMPC outputs	+47.81/-48.25
Reference voltage	4.087
DAC outputs CH1, CH2	2.490 / 2.494
Bias voltages (default) CH1, CH2	25.10 , 25.07

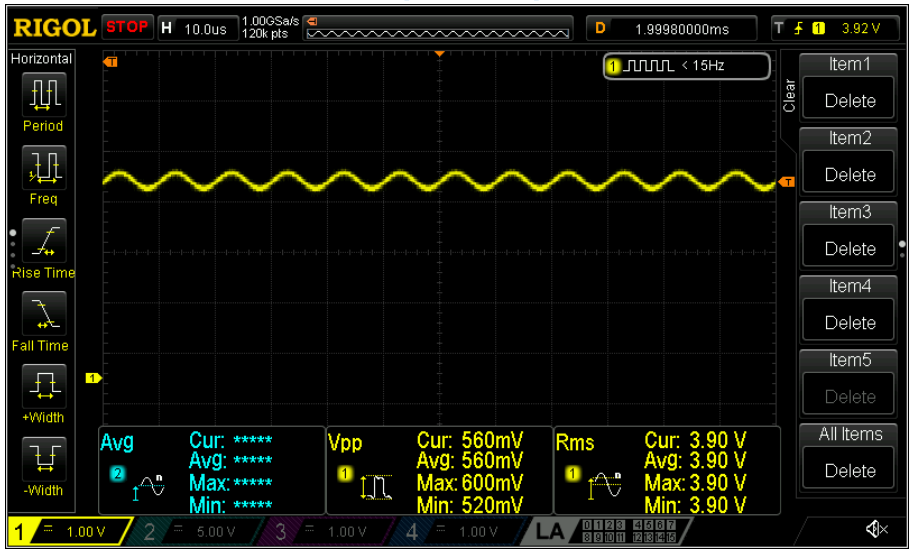
Test results discussion

- **Correctness of output signal conditioning**
  - The correctness of the output signal for 6 input current signal amplitudes (100 kHz)

HV Amplifier OUT (1 mA)



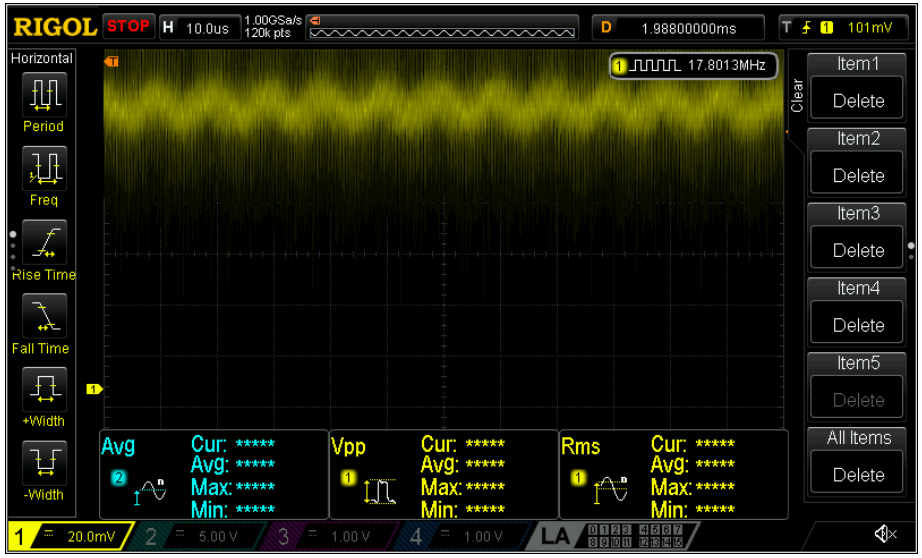
LPF OUT (1 mA)



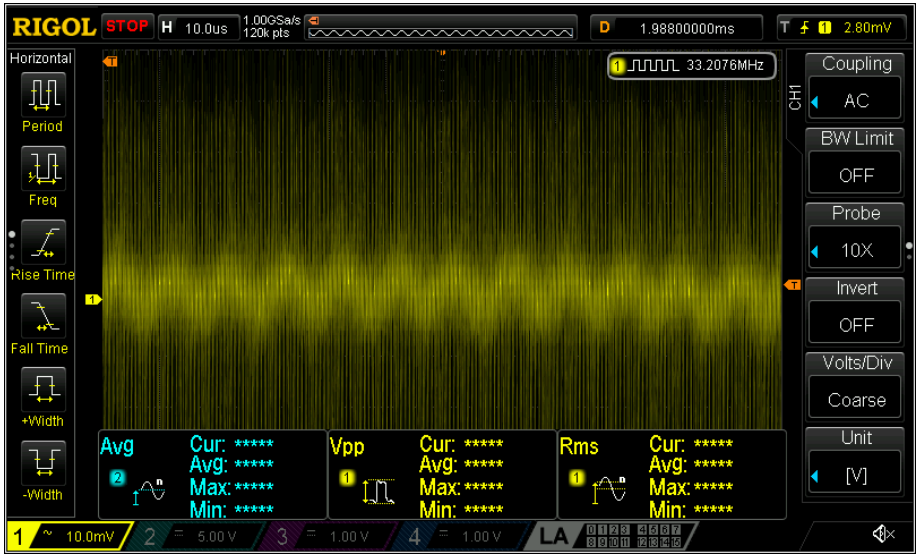
Test results discussion

- **Correctness of output signal conditioning**
  - The correctness of the output signal for 6 input current signals (100 kHz)

HV Amplifier OUT (10 µA)



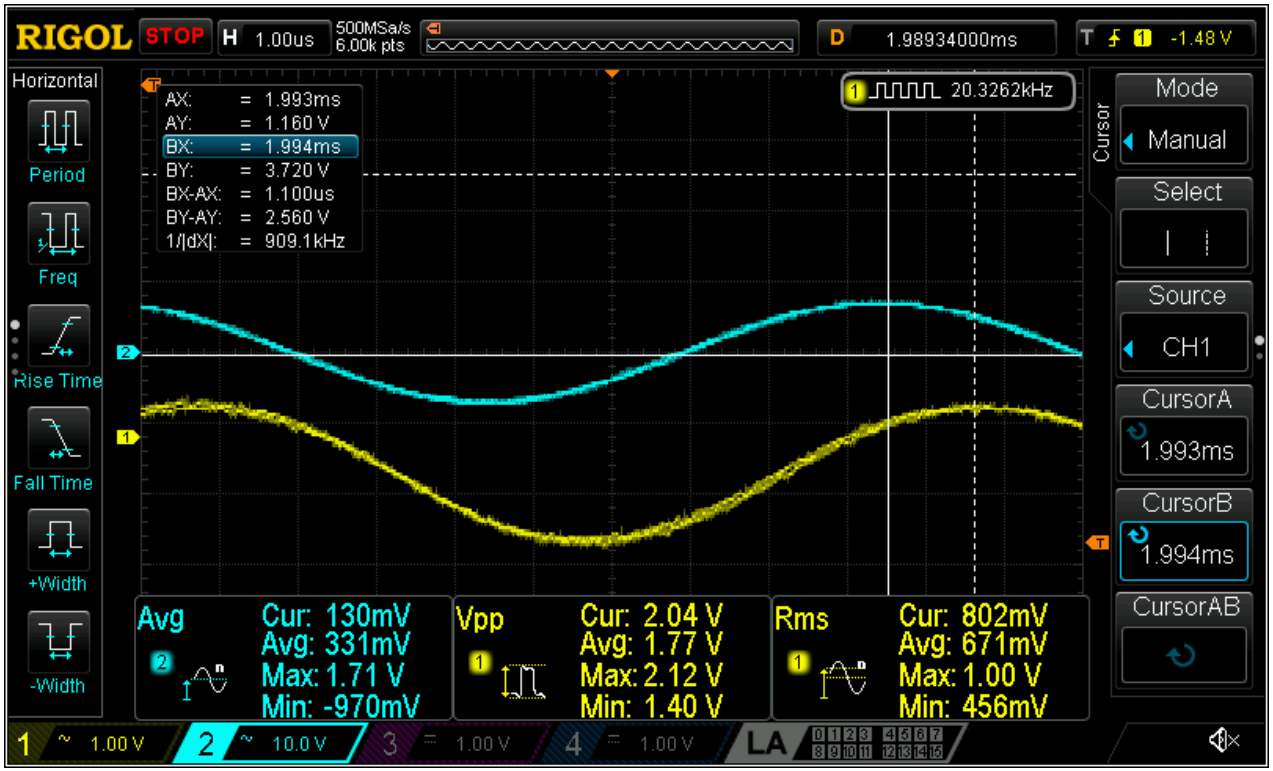
LPF OUT (10 µA)



Test results discussion

- **Delay between input and output signals**
  - The delay between input and output signals for 3 frequencies was measured:

Delay = from 0.23 µs (500 kHz) to 1.1 µs (100 kHz)



Test results discussion

- **I²C communication with temperature and supply current sensors**
  - As part of the tests, the correctness of I²C communication with two sensors was checked:
    - STH31 - Connection with the temperature sensor was established and correct temperature was read.
    - INA219 – Connection with the sensor was established.

Full scale design plans

- The presented solution can be partially adopted in the final design
- Minimization of the delay between input and output signals and noise reduction is needed in the final design
- 2 more channels are needed in the final design

- Changes in schematic diagrams (duplication of some blocks; replacement of HV OPAMPs; addition of EMI suppression filters)
- PCB project redesign

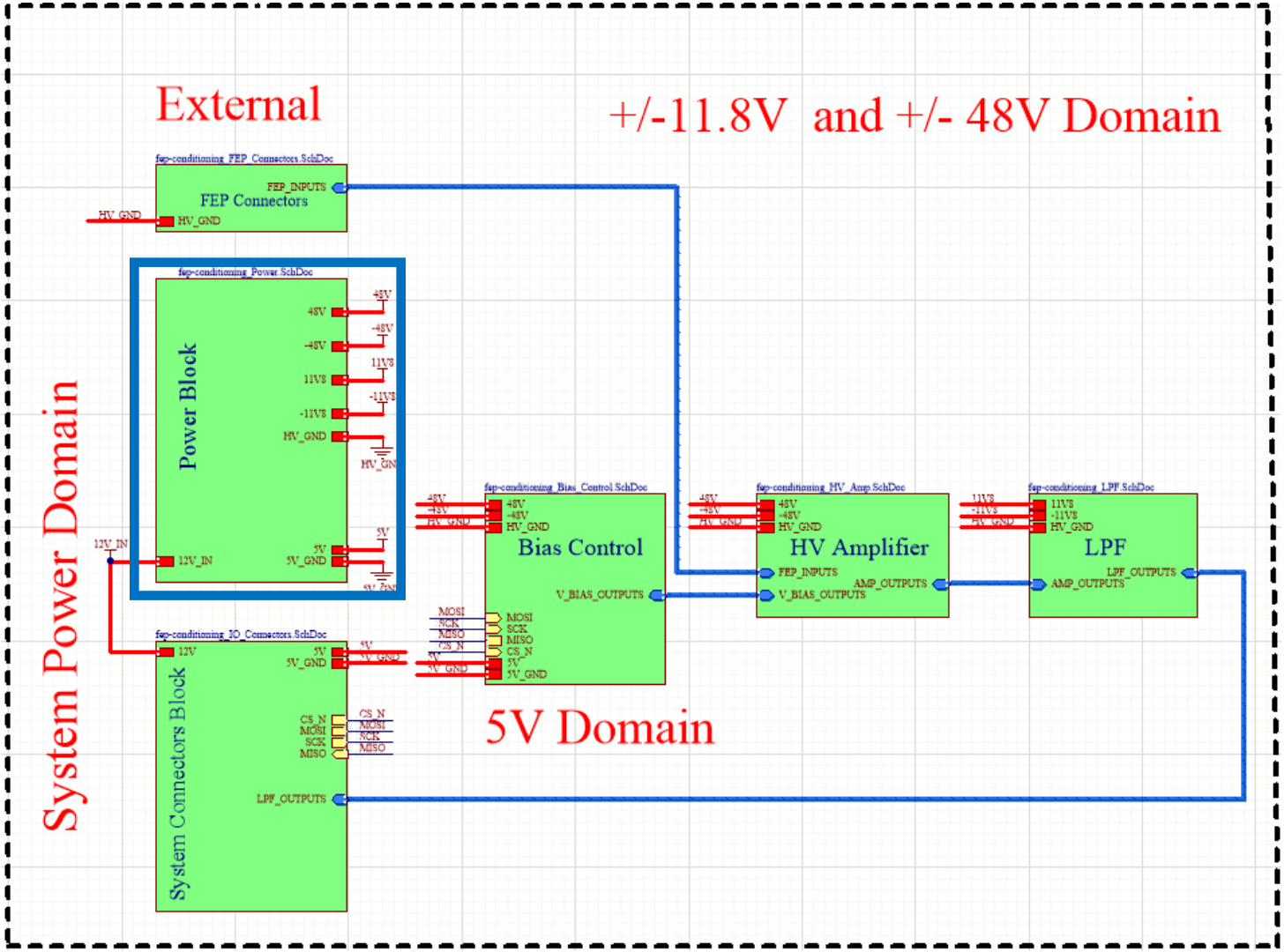
Summary

- Requirements
  - 1 output signals per cavity => 4 output signals per module
  - Response time less then 1 µs
- PoC, implementation and verification
  - PCB supporting 2 probes
  - 4-layer PCB
  - Correct operation of the power block and output signal conditioning
  - Delay between input and output is about 1.1 µs for 100 kHz input signal
- Full scale design plans
  - PCB supporting 4 probes

Thank You

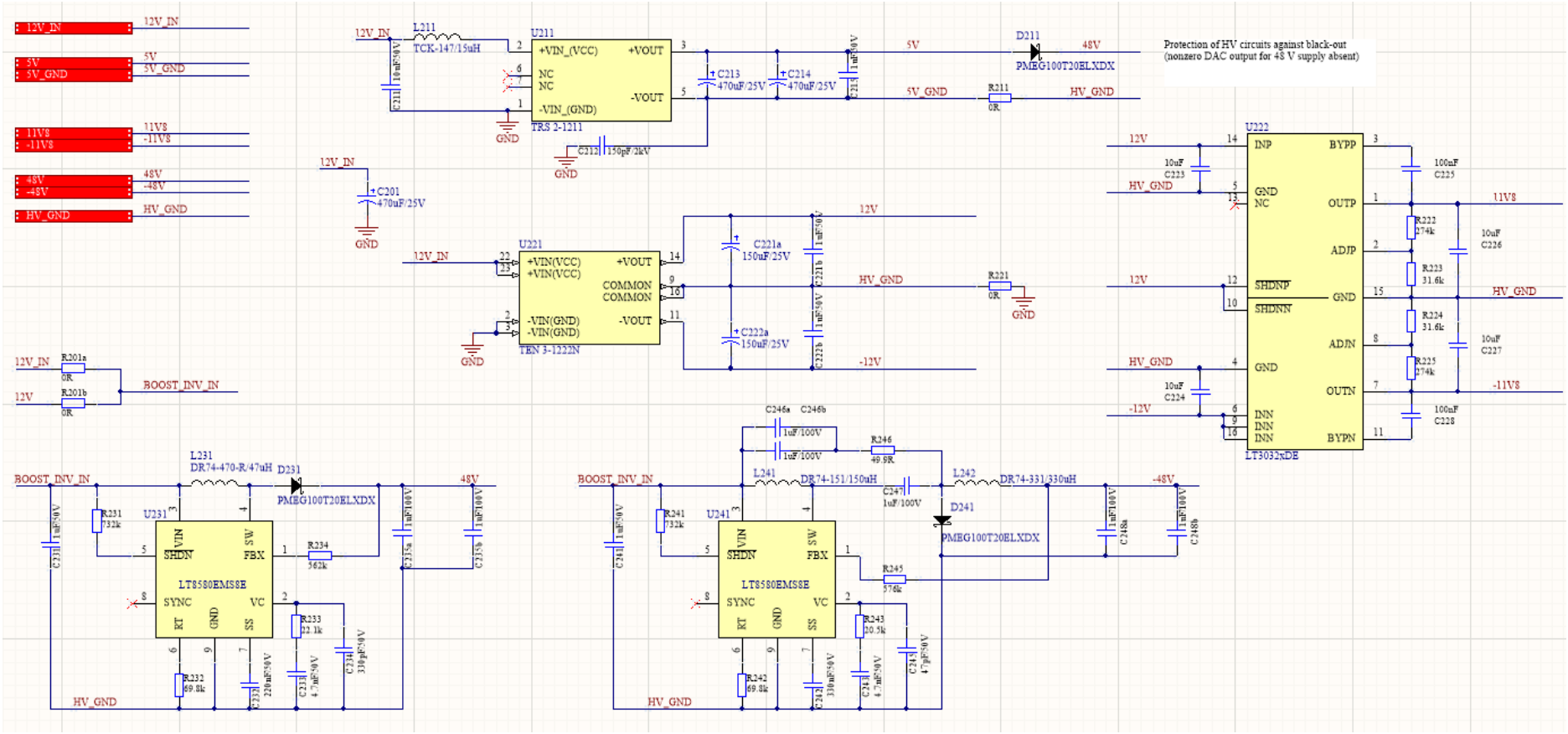
The sub-module design details

Power Block



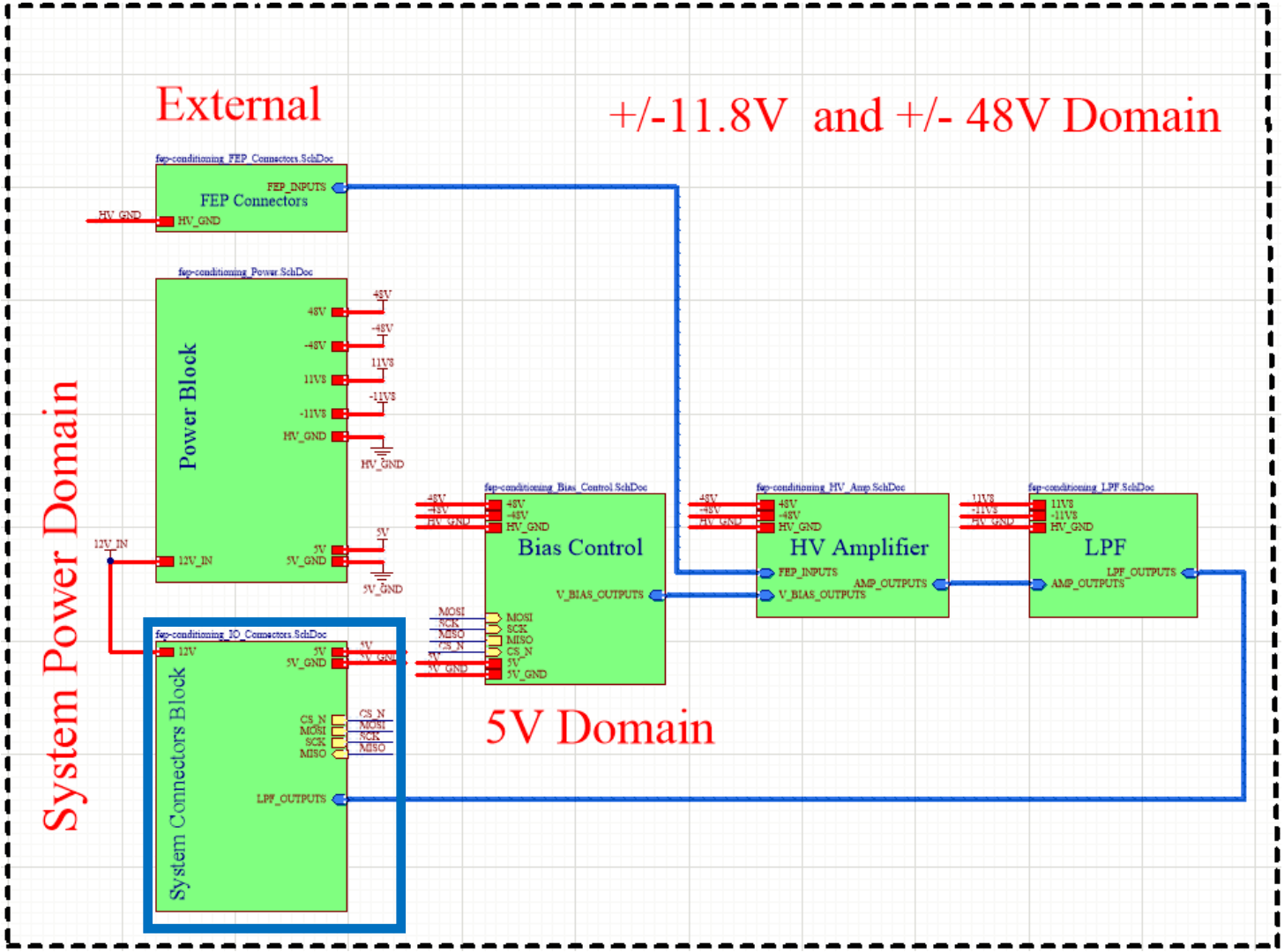
The sub-module design details

Power Block Schematic Diagram



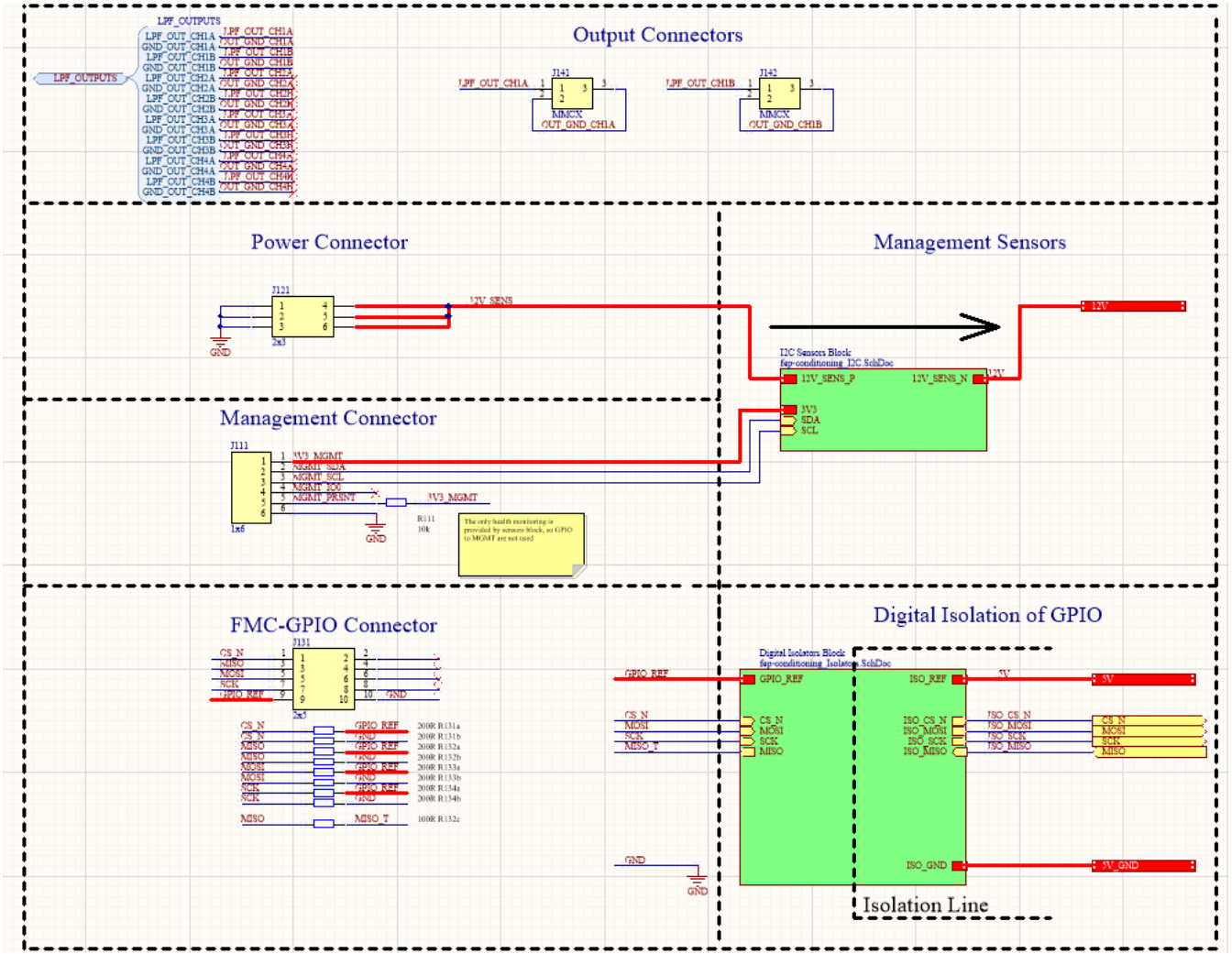
The sub-module design details

System Connectors Block



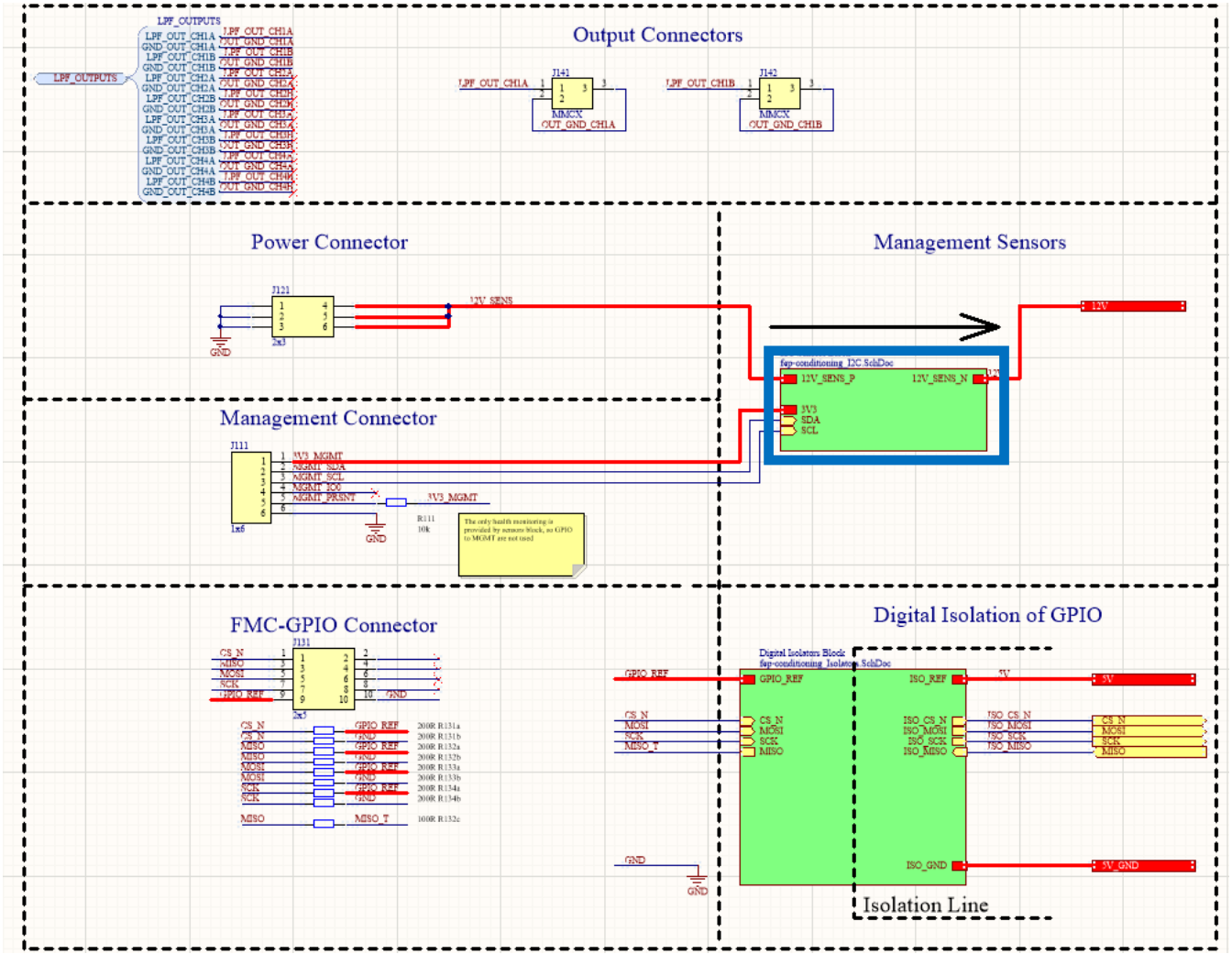
The sub-module design details

System Connectors Block Schematic Diagram



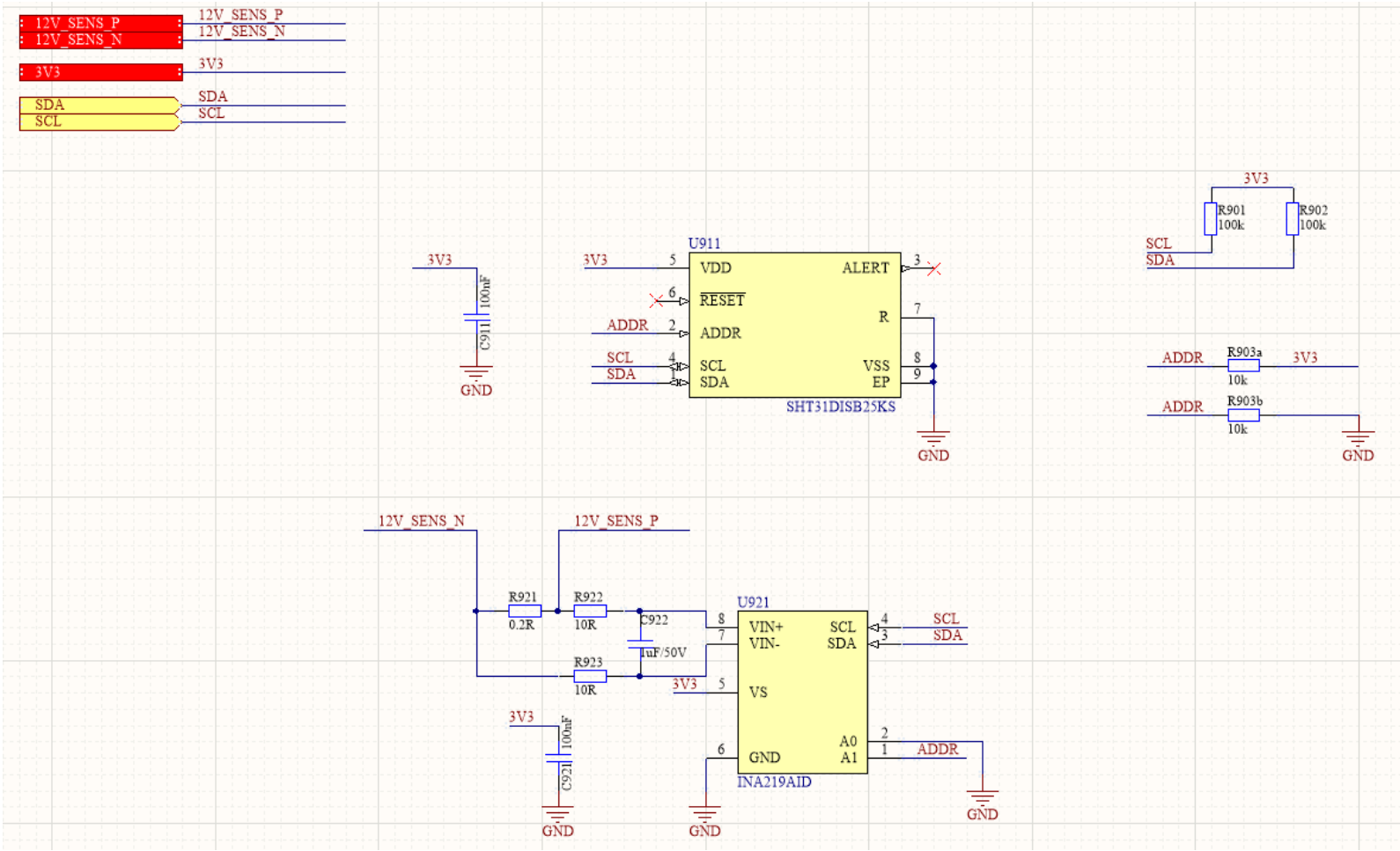
The sub-module design details

Management Sensors



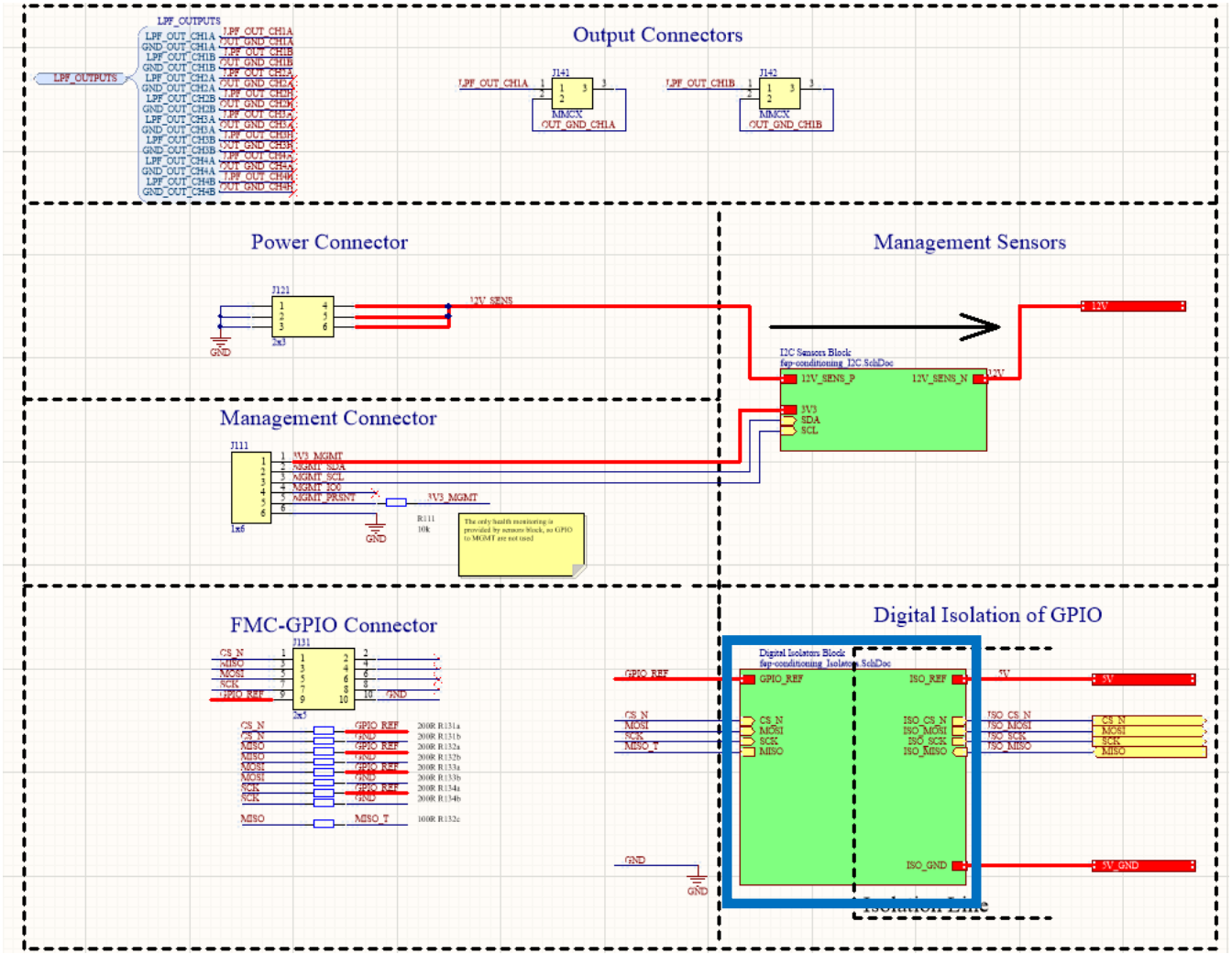
The sub-module design details

Management Sensors Block Diagram



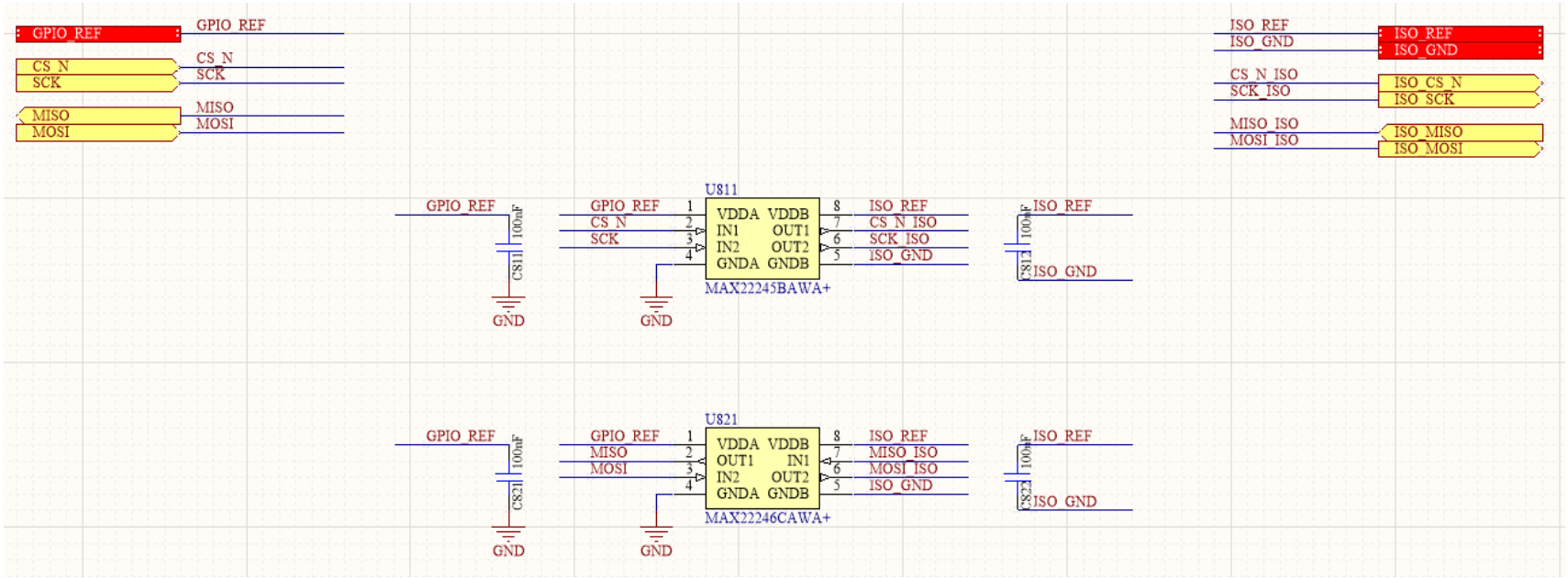
The sub-module design details

Digital Isolation of GPIO



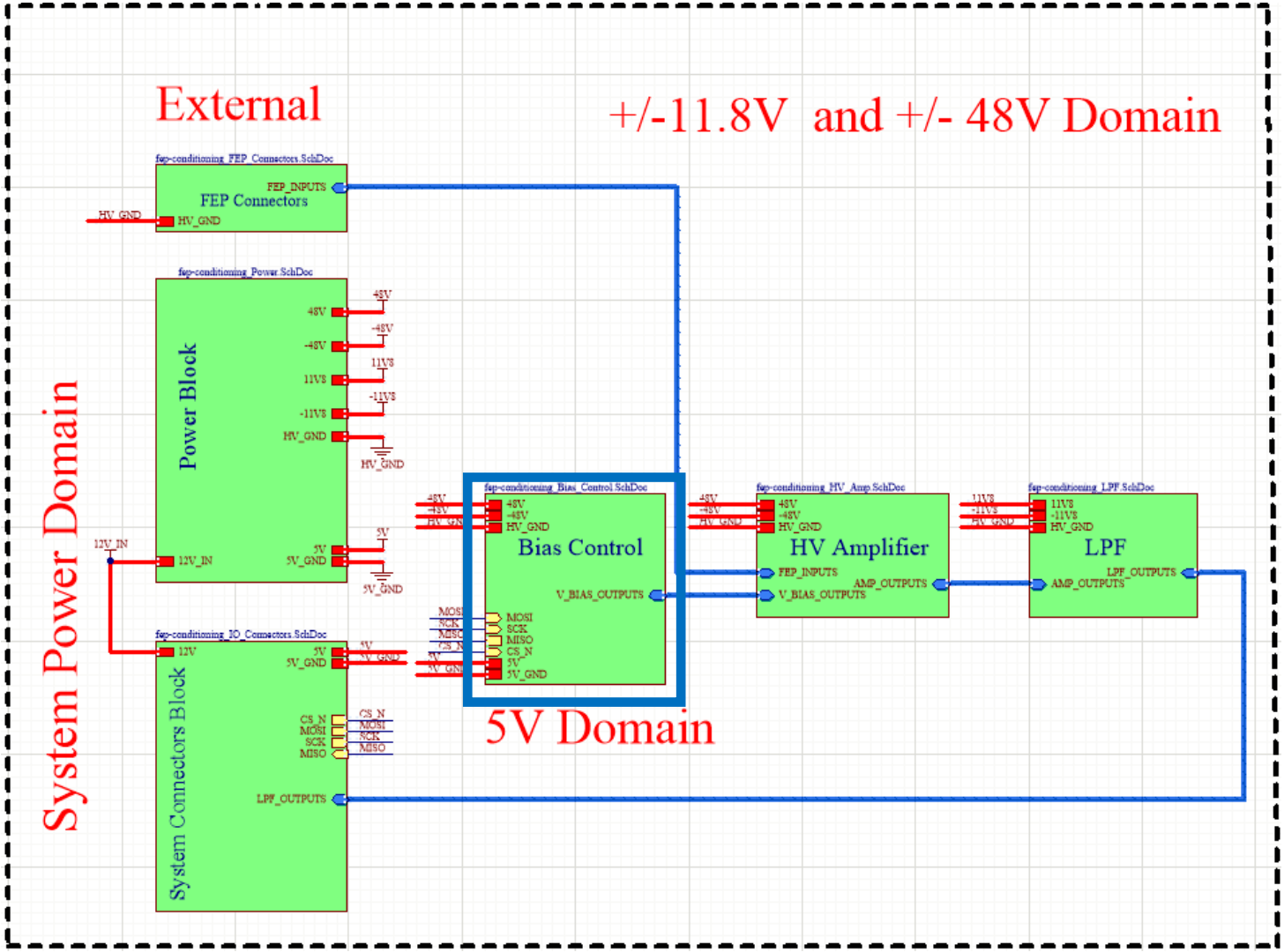
The sub-module design details

Digital Isolation of GPIO Block Diagram



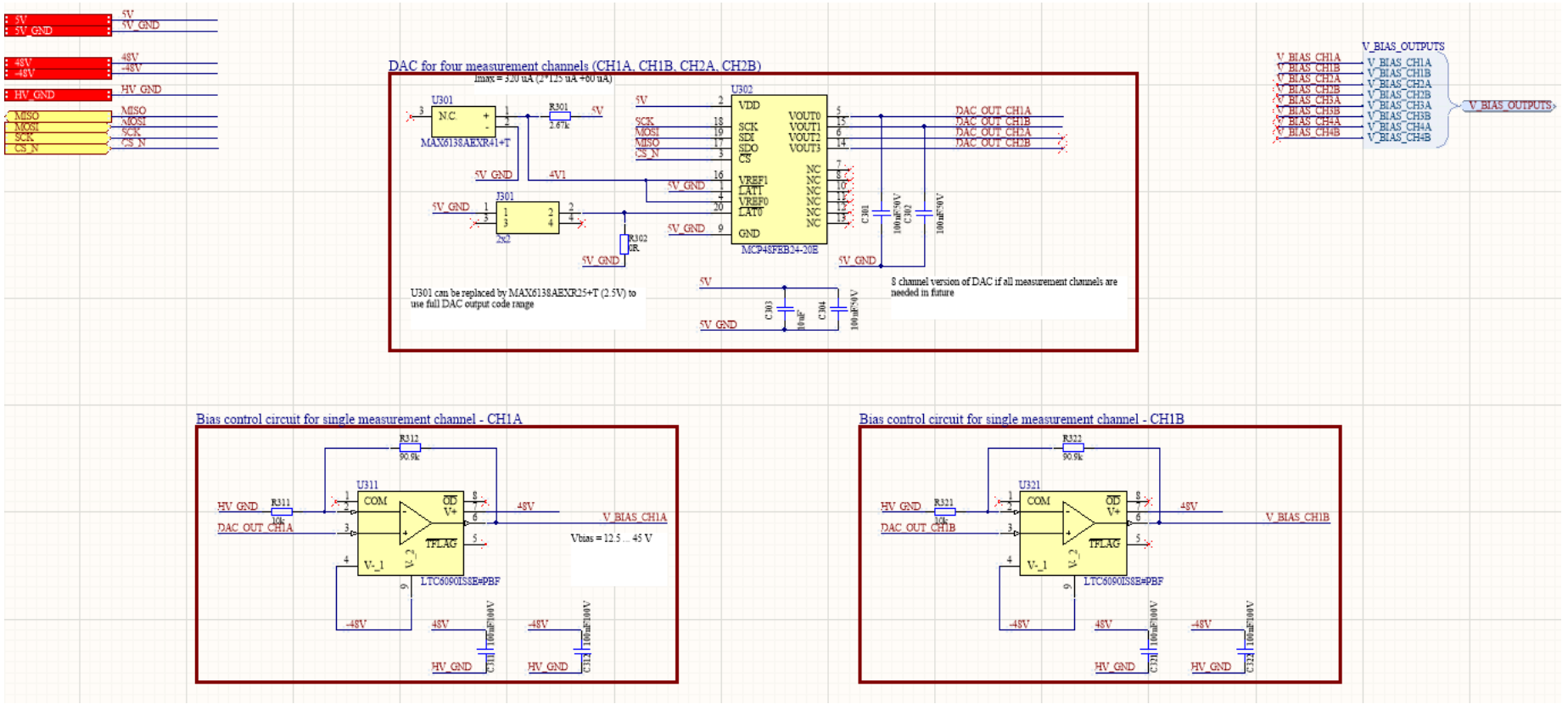
The sub-module design details

Bias Control



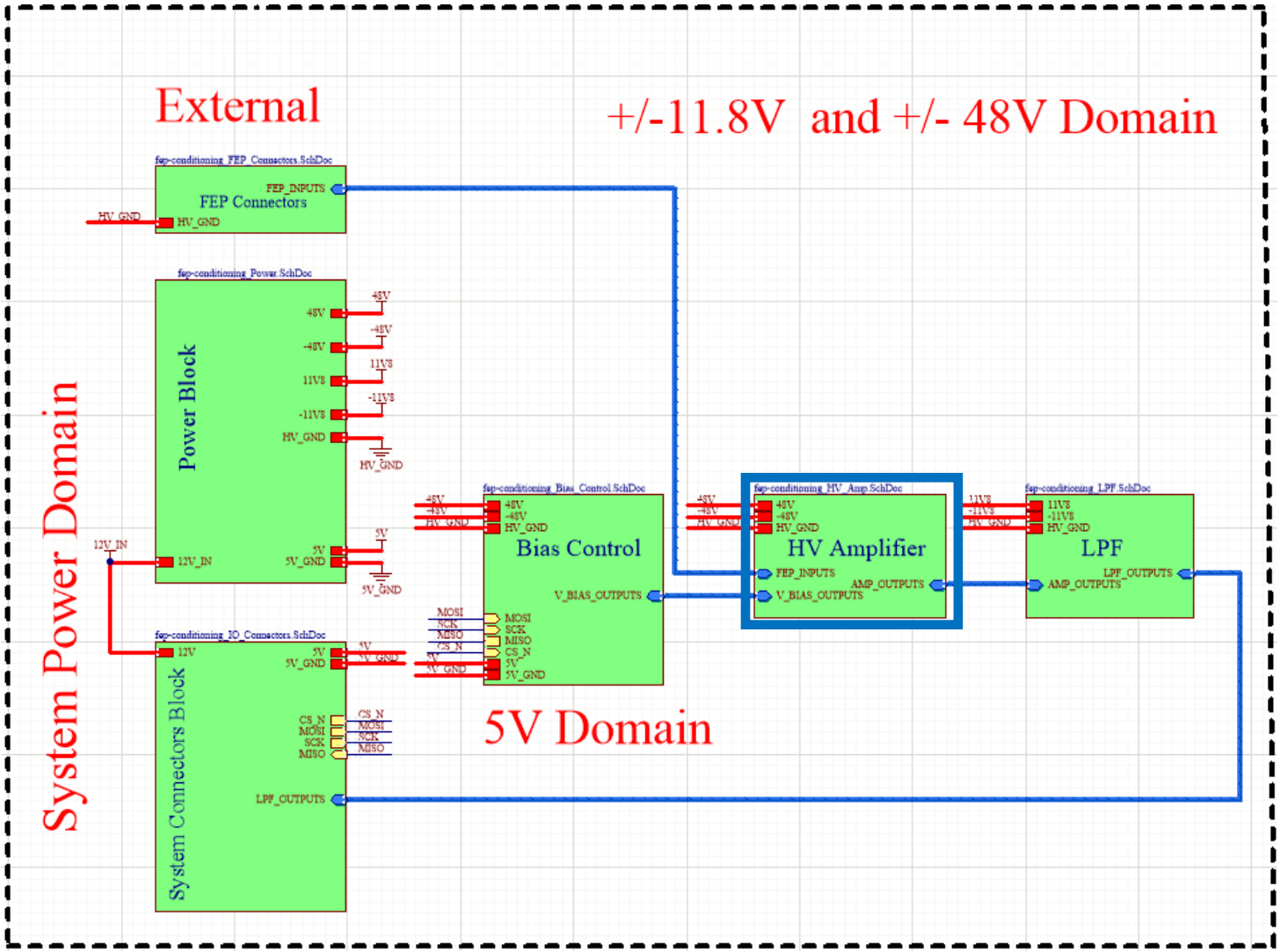
The sub-module design details

Bias Control Schematic Diagram



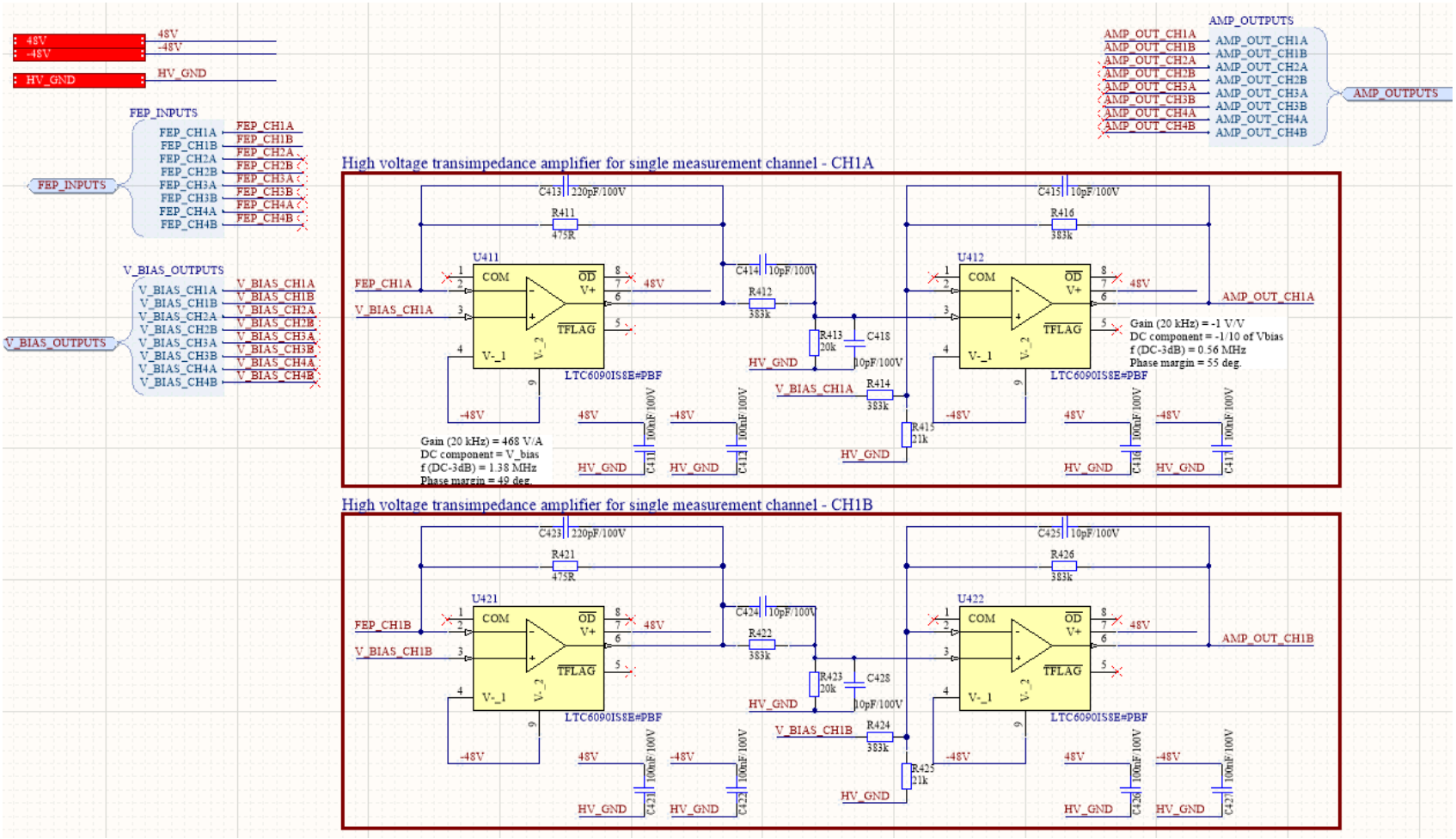
The sub-module design details

HV Amplifier



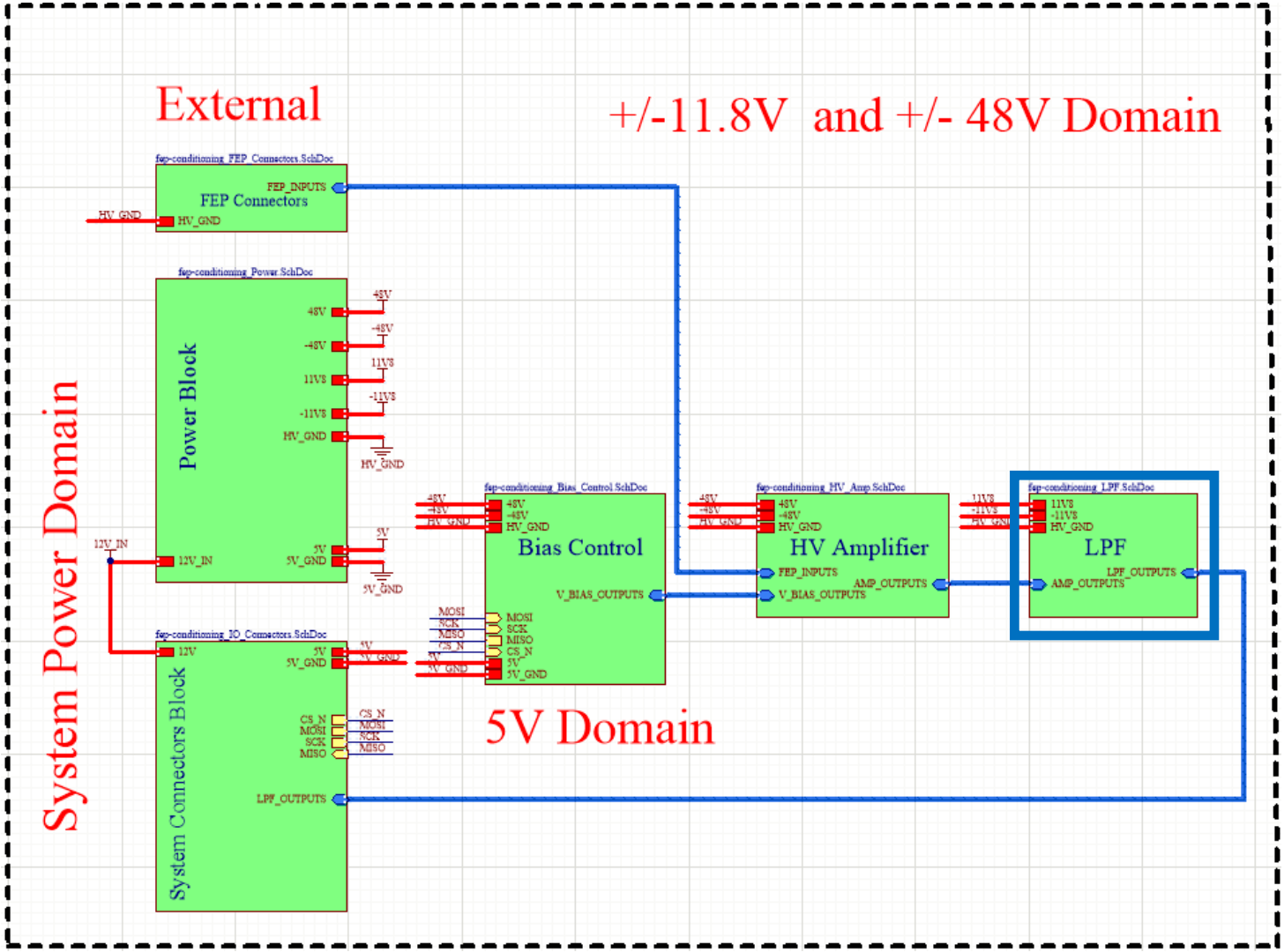
The sub-module design details

HV Amplifier Schematic Diagram



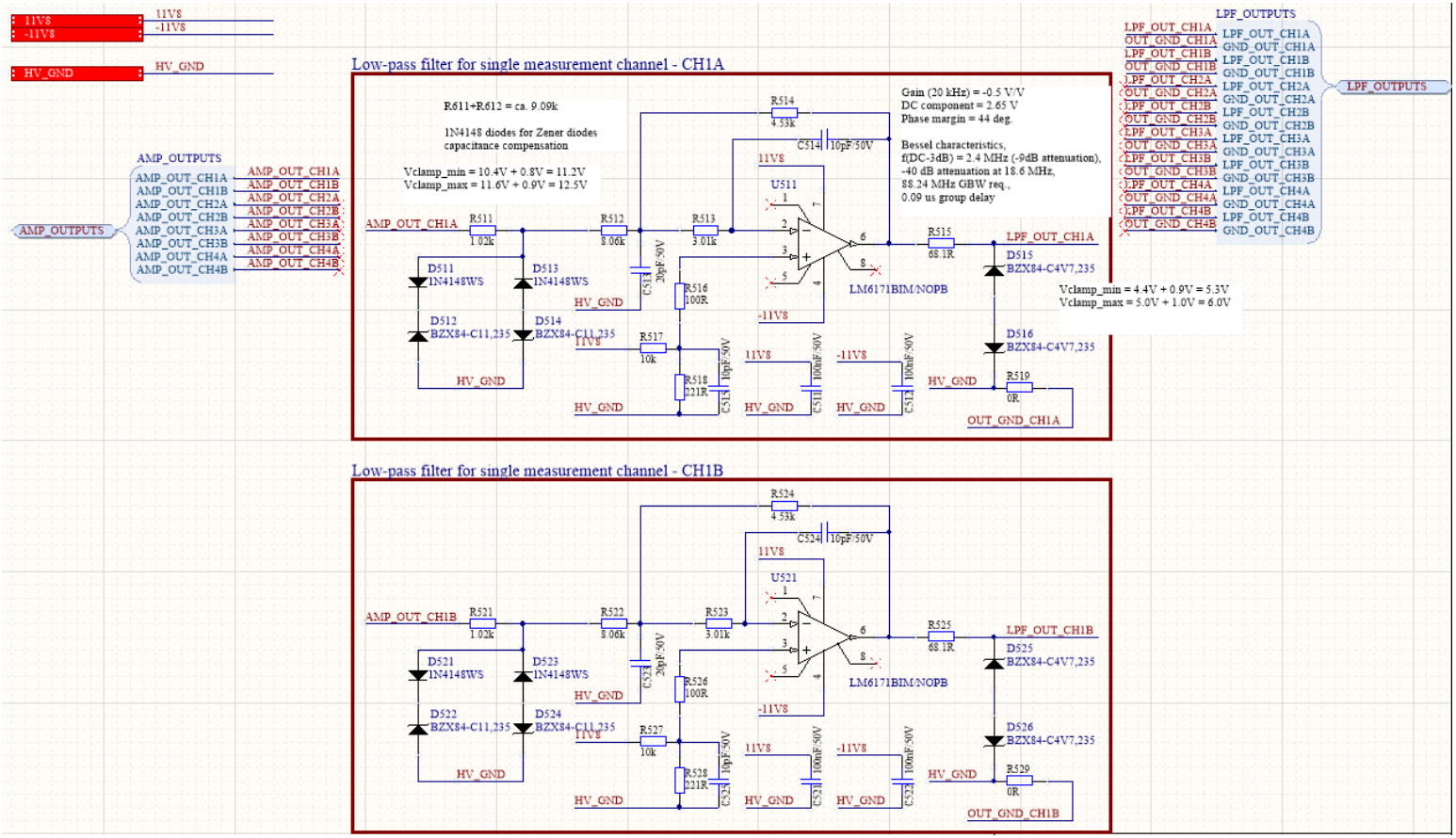
The sub-module design details

LPF Block



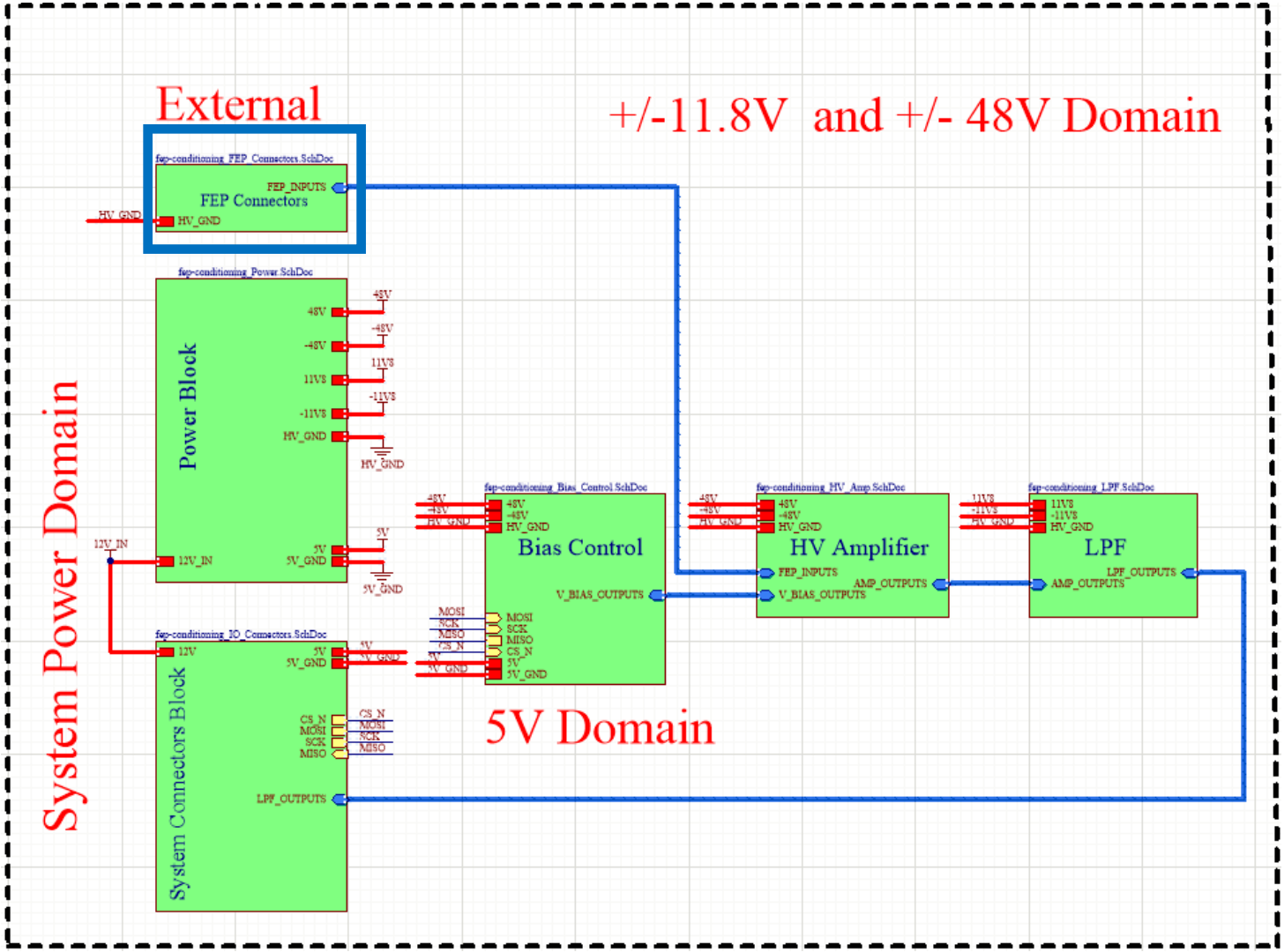
The sub-module design details

LPF Block Schematic Diagram



The sub-module design details

FEP Connectors



The sub-module design details

FEP Connectors Schematic Diagram