DAPHNE uC Software status and plans

Juan Vega
CONIDA-Peru

Fabian Castaño
Universidad de Antioquia-Colombia

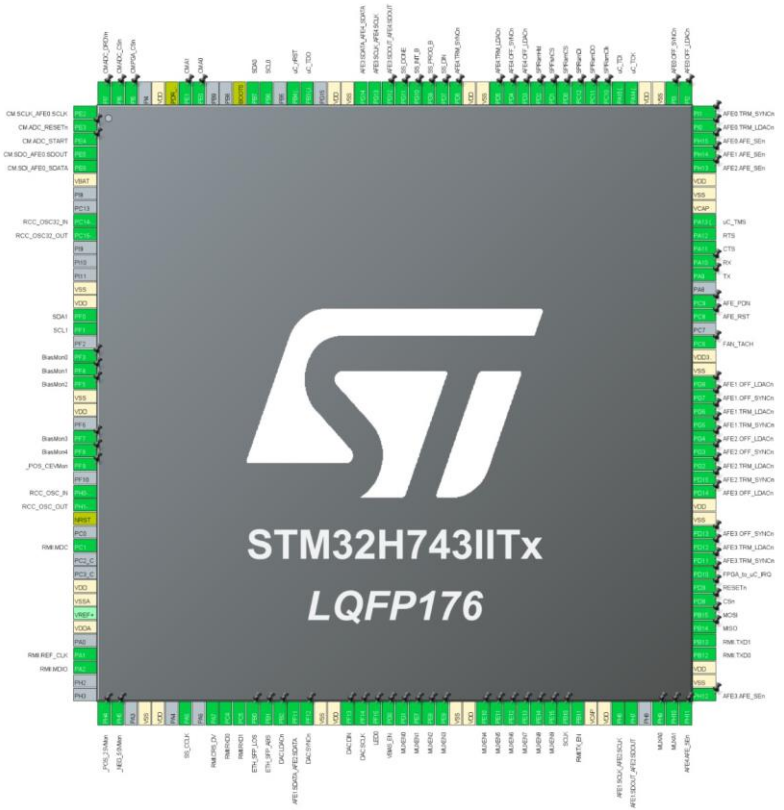
Javier F. Castaño
Universidad Antonio Nariño-Colombia

Electronics WG Meeting

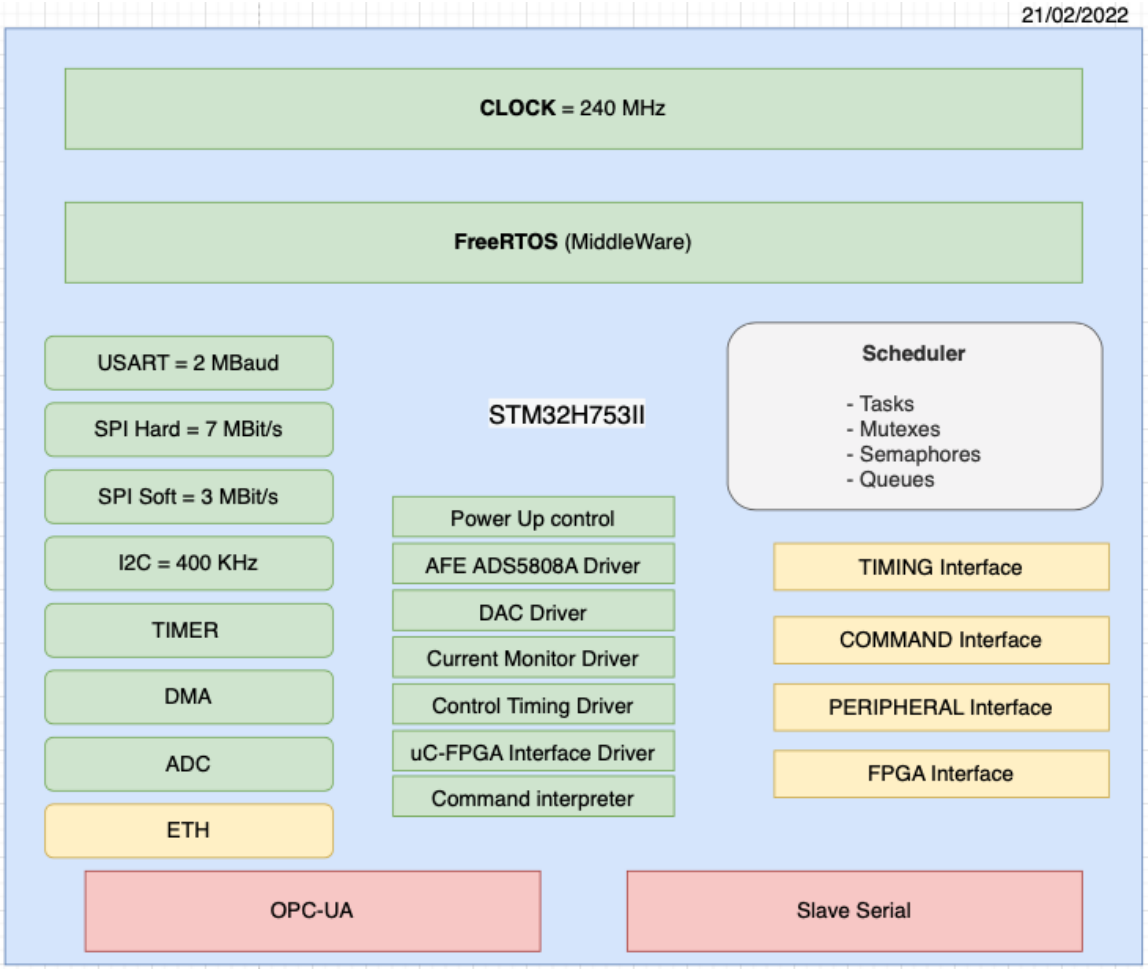
February 21, 2022

DAPHNE - Microcontroller Setup

- Internal CLOCK Config = 240 MHz from external 8 MHz XTAL
- Pinout Configuration (176 pins)
  - 5 AFEs
  - 23 DACs
  - Current and Voltage Monitoring
  - Power Management
  - USB Serial Interface
  - Ethernet Interface
  - Slave Serial FPGA Interface



DAPHNE - Microcontroller Setup



DAPHNE - Microcontroller Setup

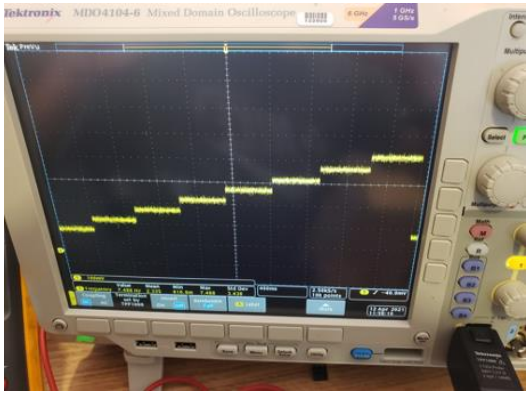
- Inter circuit communication (SPI)
  - SPI interface (Use of DMA to improve speed and performance)
  - Hardware SPI = 7 MHz
  - Software SPI = 3 MHz

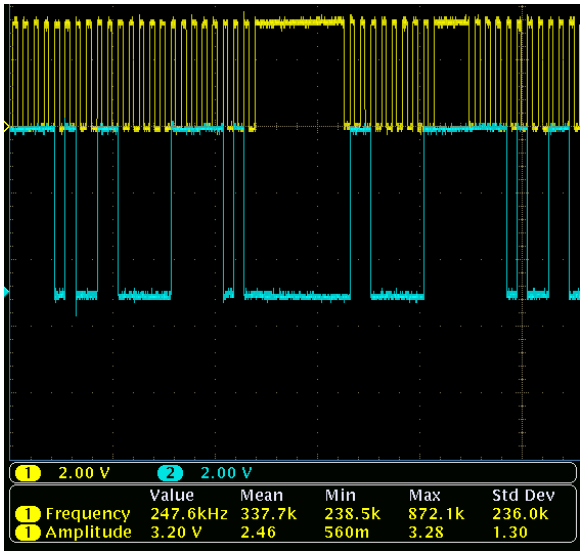
AFE Configuration

DAC Offset and Trim config

FPGA Interface (DAQ 640 data stream)

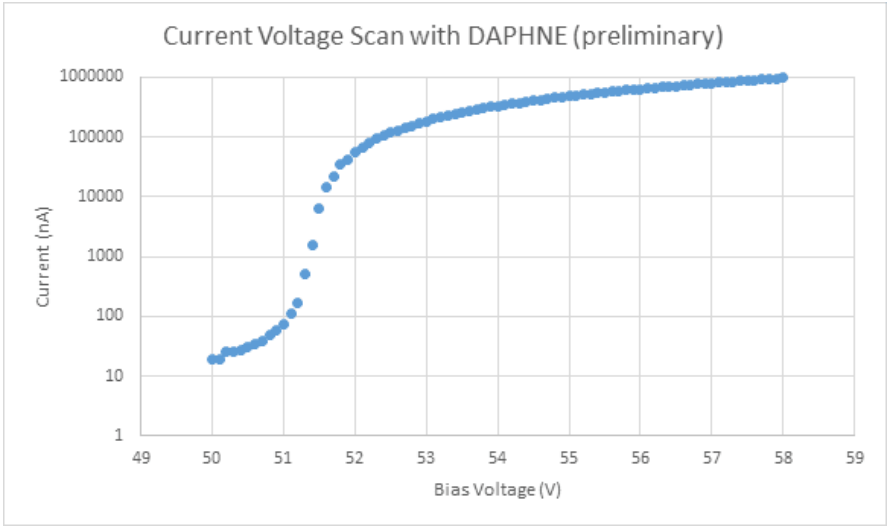
DAC Vbias and CM





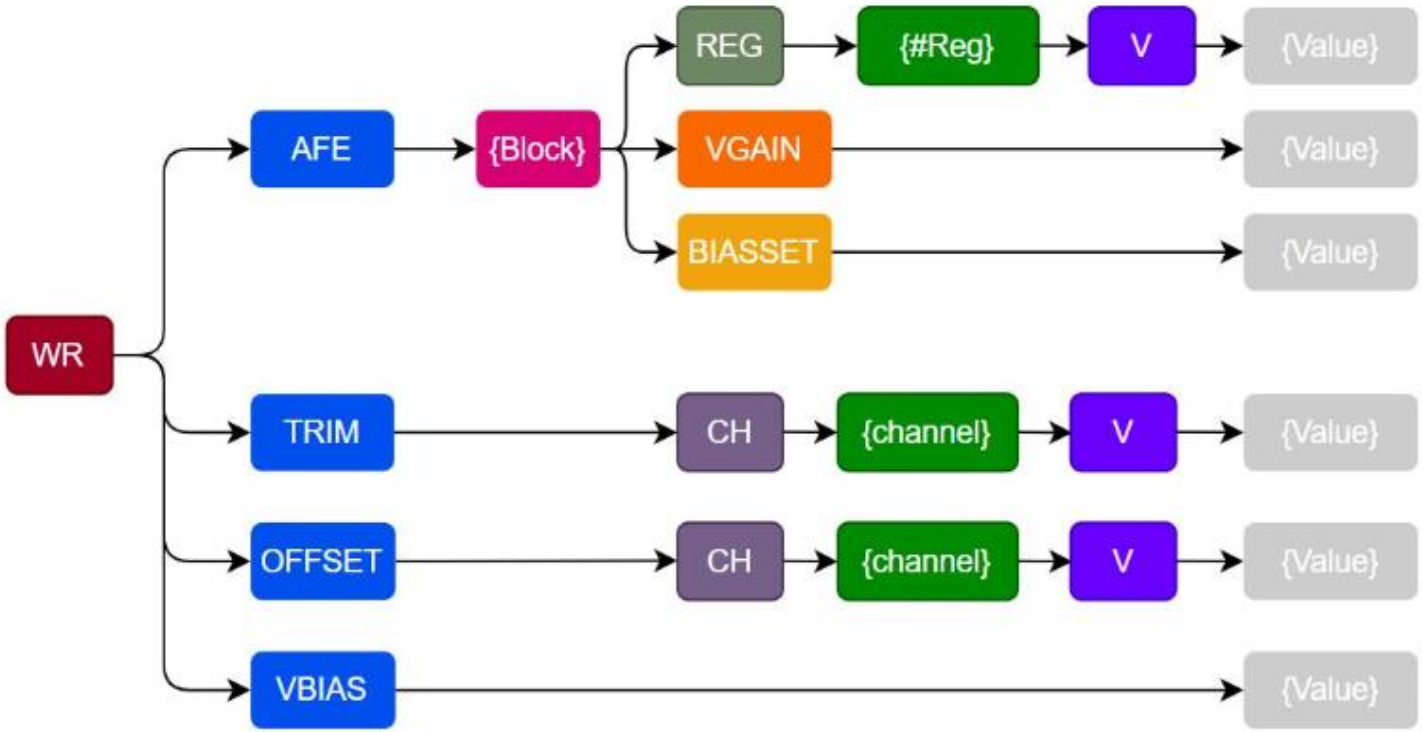
DAPHNE - Microcontroller Setup

- Inter circuit communication (I2C)
  - TIMING Interface configuration (Control driver designed, 62.5 MHz generated and tested)
  - Current and Voltage Monitoring (Control driver designed, tested)



DAPHNE - Microcontroller Setup

- Command Interface (USB-USART High Speed)



COMMANDS AND FUNCTIONS

Commands	Description
WR	Write command
RD	Read command
CFG	Config Functions command
CH	Channel,input parameter, Value range 0 to 39
V	Value, input parameter, decimal format
AFE	AFE section Select, Value Range 0 to 4 or *'ALL'*
REG	AFE Regs select
VGAIN	AFE Gain voltage DAC select
BIASSET	AFE BiasSet voltage DAC select
VBIASCTRL	Bias control Voltage RAW DAC Select
TRIM	Trim DAC Select
OFFSET	offset DAC Select
CM	Current Monitoring Select
FPGA	FPGA Select Device

Functions	Description
RESET	Reset set value: ENABLE or DISABLE
POWERDOWN	PowerDown set value: ENABLE or DISABLE
RAMP	Enable AFE RAMP test
SYNC	Enable AFE SYNC test
SKEW	Enable AFE SKEW test
CUSTOM	Enable AFE CUSTOM test
ONES	Enable AFE all ONES test
ZEROS	Enable AFE all ZEROS test
INITIAL	Enable AFE INITIAL test

ANALOG FRONT SECTION

For the AFE sections, we have 5 blocks:

AFE *0* -> Channels 0 to 7 AFE *1* -> Channels 8 to 15 AFE *2* -> Channels 16 to 23 AFE *3* -> Channels 24 to 31 AFE *4* -> Channels 32 to 39

AFE DEVICE REGISTER (REG)

write to AFE 4 Register 2 the value 3(Decimal)

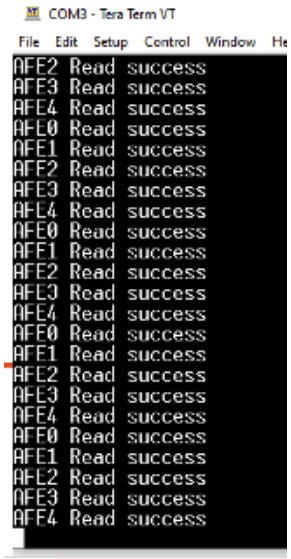
```
WR AFE 4 REG 2 V 3<CR><LF>
```

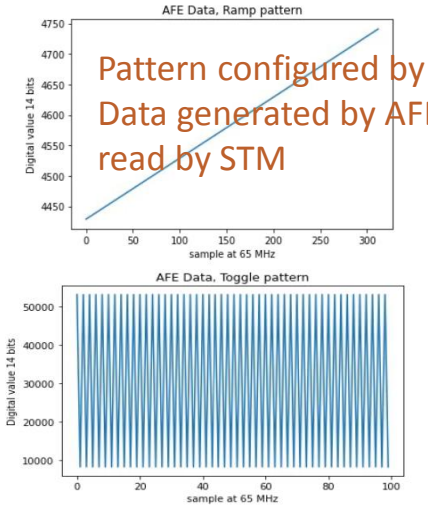
AFE GAIN VOLTAGE(VGAIN)

write to AFE 1 the value 150mV for its Gain Voltage.

DAPHNE - Microcontroller Setup

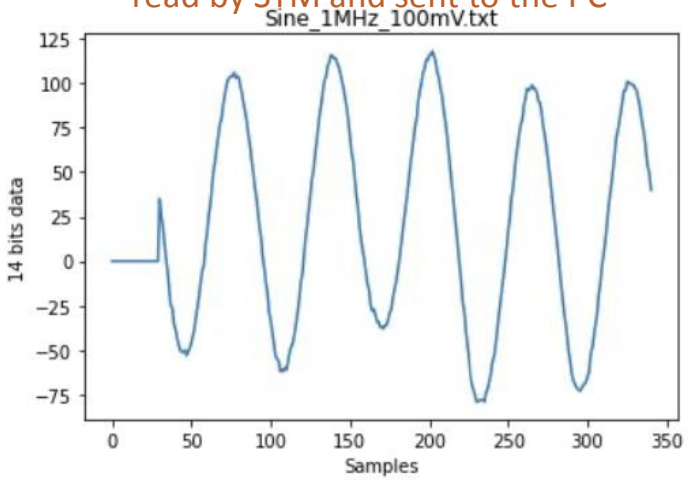
- AFEs and DAC driver implementation
  - Full access AFE driver developed (full memory R/W capability)
  - Full access DAC driver developed
  - STM-FPGA SPI interface (DAQ test purpose)





Pattern configured by STM, Data generated by AFE and read by STM

External signal sample by AFE-FPGA, read by STM and sent to the PC



uC Fast Ethernet Interface

PHY Chip DP83620

Optical Transceiver on SFP Cage

Media converter (cable to optical)

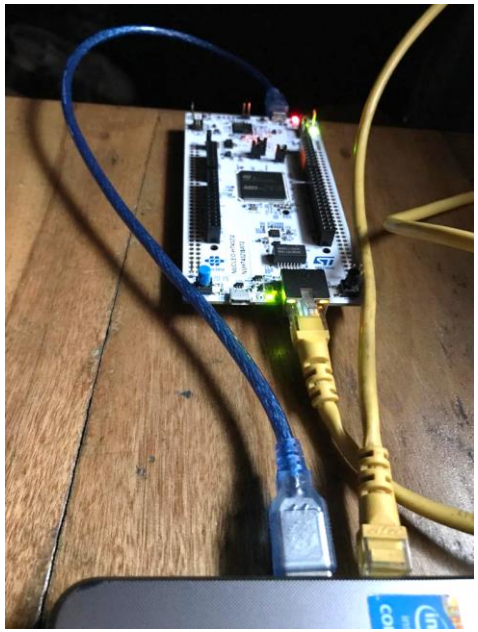
Mistake on pins MDC and MDIO (PHY Chip SMI): solved last week

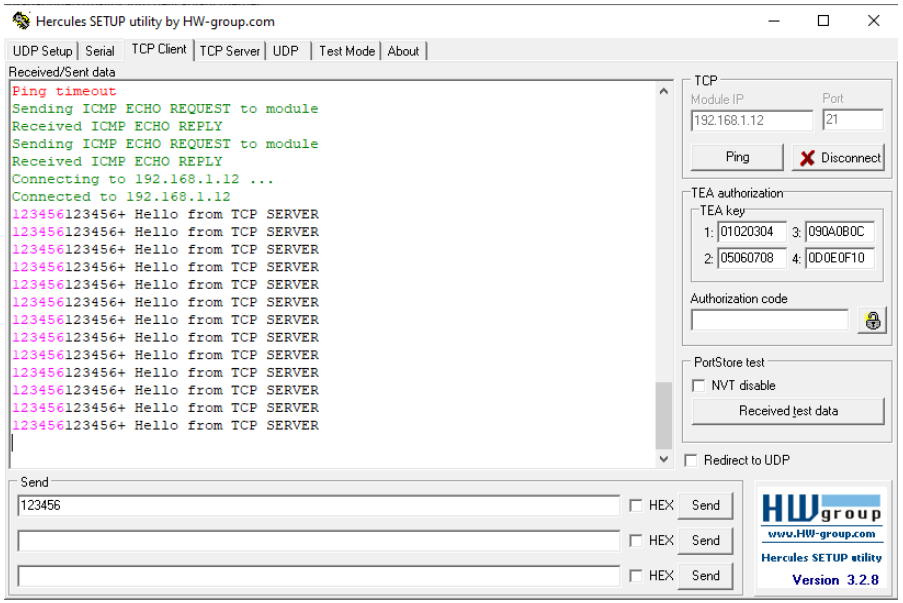
We were able to use the SMI and apply a soft reset to PHY, and perferm writing/Reading operations

The driver has been completed and will be tested this week

DAPHNE - Microcontroller Setup

- Advances in ETH configuration (DHCP with NUCLEO Board)
  - TCP/UDP protocol implementation already done in NUCLEO setup, Already integrated with other peripheral configuration to evaluate collision between instructions





ONGOING WORK

- To finalize the Ethernet communication
- OPC-UA implementation and integration to DAPHNE
- Slave-serial FPGA configuration: Flash memory, slave-serial (SPI-like protocol). Currently on development, to test this week
- In parallel we are analyzing the STM32MP157 migration (to have Gigabit Ethernet capability, doing compatibility tests, using development boards

THANKS!