1. **Overview of the BDE system design, requirements and specifications**
   Cheng-Ju Lin

Q: (page 15) Is the CRP 3*3 meters?
A: Yes.

Q: Will the QA/QC issues of having these extra components, like the patch panel at the slide bearing of the FEMB, be covered in later talks?
A: It will be briefly covered in Shanshan's talk. The patch panel is still under design. We have different design options including merging the two into one. In shanshan's talk, it will have a few bullets highlighting the basic idea to continuously testing the patch panels.

Q: I guess you will qualify the cables and the extra components that are different from the horizontal drift. The performance of the thermal cycling and so on.
A: It has done at a certain level. Once we have the final design, a more careful study will be done. Ultimately, we have a series of tests at CERN studying the Cold Box and ultimately the module-0. So those will be the long term reliability tests.

Q: Does the slightly different design in FEMB mean you need a separate qualification for that (VD FWMB) as well because it got a different connector on them?
A: It's a different connector. It will be tested. The testing procedures of the different connectors will be the same between FD1 and FD2. This is not new. This is the design for SBND. This connector and this type of cables are what SBND is using. (It's been qualified). But for DUNE, we will do our own set of testings.

Q: (page 16) Xueye concerned about the cables used in the test. From her experience using 8 meter cable, they need to use a repeater to get rid of the bit errors.
A: Don't see the troubles when using these cables for the testing in BNL (Shanshan) and Fermilab (David).

Q: (page 18) is grounding the same between FD1 and FD2?
A: Yes. The two grounding uses same strategy. But the implementation is not the same due to the difference that one uses APA and the other uses CRP.

2. **BDE interfaces with FD2 consortia**
   Vladimir Tishchenko

Q: (page 11, 12) What is need to be done to make the decision between the two patch panel designs?
A: We have a preference on design B. It makes the cabling easier. B is low profile can fit into the tight space. We're going to focus on the design B. But we can't make the decision on our own. It have implication on real-estate on the bottom CRP. Need to make sure the patch panel design won't impact the supporting feet of the CRP plane. Also, the patch panel needs to be secured to the composite ring of the CRP. Need to make sure the CRP consortia is OK with the patch panel position, and it's not in the way of any supporting structures that people use to hold CRP doing transport. This placement has impact on the corrugation. Need to design the low profile that it will not interfere with those membrane corrugation. CRP factory prefer design A, less clutter, a single patch panel. We have monthly technical board meeting every month, and hope to make a decision at the end of May. We want to have a decision soon, since it has implication on the prototype effort.

Q: Is there anything special about the connection of the cable shield on the patch panel?

A: No connection between the shield and the patch panel. There is connector. Medal part (of the patch panel?) needs to be grounded. (not really sure about this question?)

Q: (page 7) Does the 7 design translate into multiple design for CE boxes and FEMB boards?
A: CE boxes and FEMB boards are all the same.

Q: Is CE Boxes grounded?
A: Yes. The reference is provided by the CE flanges. The power cable is connected to CE box enclosure at one end, and the other end is connected to the CE flanges. There is connection between CE boxes and adapter boards. So CE boxes enclosures connect to the common reference of the adapter boards, through the screws and the 96-pin sockets.

Q: Any chance to ruin the connectors of the CE boxes?
Aa: Possible. But the box is relatively light. It's easy to insert box into the connectors.

Q: Is it easy to remove the CE box?
A: Yes. Release the screws and pull the box out. No special tools needed. During five installation, there's been no damage so far. For DUNE, there is no plan to move CE boxes multiple times.

Q: (page 25) What is the baseline assumption on the number of the PDS fibers/cables? What are the mitigation conservative number that you assumed? If it's the most conservative case, is the risk level really high?
A: We have the cable numbers provided by PDS on the most conservative counts. There's enough room in the penetrations to allow the fibers to go up. The part that needs to be defined better is where they come up. PDS doesn't align well with the penetration. Their fibers come up at several different locations. We need to define well with the PDS group.

3. BDE and CRP interface
Cheng-Ju Lin

Q: Where is that CRP filter box set
A: It's mounted on the composite frame

Q: (page 11) Do you have time margin for repairing? Do you expect a good yield?
A: Before shipping to CRP factory, all FEMB will be tested cryogenically. After the install, will make sure all channels work and noise level as expected. If there is a problem, have spare FEMB onsite for replacement. Assume Matt has a time margin for debugging.

Q: Need to install the cables underneath? Won't have enough space when installing the last one?
A: Yes, will install the cables from underneath and one side. It's a big problem on the last row installation. A team are working on solving the problem. One idea is that for the last row it will install half CRP unit.

Q: Are you responsible for the cable trays that go along the cryostat wall and feedthroughs?
A: No. It's I&I's responsibility.

4. Cryostat penetrations and FD2 installation
Manhong Zhao

Q: (page 3) What are the access holes?

A: ….

Q: For the mini-SAS cable from FEMB to the patch panel, are these commercial parts or customized?
A: They're commercial. Can be bought on Digi-key. We will make modifications to improve the shielding based on SBND. It's commercial cable but we will wrap some shielding outside.

Q: Will the commercial cables behave the same in room temperature and cryo case?
A: Cables in SBND ordered from 3M. They have good QA/QC. We tested most of the cables during the prototype and early pre-production. All cables passed the cold test without issue. For HD and VD, will perform cold test on 10% of the cables. Based on the past experience, the risk is low.

Q: About shielding, how do you wrap the cable?
A: The wrap is sleeve. The original shield of the cable on the edge has not been tightly closed. When you wrap the cable, the edge conductor might exposed. We put sleeve with closed tape wrapped around at both end. Those tape will be cured at higher temperature and has been test in cryo without any issue.

Q: How do you make sure the connection to the patch panel is correct?
A: We follow a cable map. We program each FEMB with unique ID. The ColdDATA has a (?) built in that can be used.

Q: How is thermal balance between the cold part and warm part? Will there be ice built up and condensation water go to electronics?
A: The crate is heated up by heaters. That regulates the temperature. Past experience on protoDUNE and MicroBOONE, the heater has never been turns on. There is no ice. Thermal simulations have been done with the current cryostat penetration, and the crossing shape spool piece design. The location of the flanges on the cryostat makes it very close to room temperature.

Q: Do you consider extreme condition when the heater won't be sufficient?
A: The heater is kept. The temperature monitor will go through the interlock system, DUNE safety system. If there is argon purge, it will trigger the system and turn on the heater. The heater voltage and the plan has been simulated by Manhong.

Q: (page 6) How do you make sure the small pieces hardware and cabling installation goes well when installing from upside down?
A: Two patch panels make it easier. But It is require some work. It's a good suggestion. Need to have a procedure or orientation. Two people work together. One holds cables and the other doing the screwing. Have looked into other design to make the install easier such as doing it after detaching the path panels.

Q: 3 SHV in patch panel in design A not design B?
A: No need to have SHV on the patch panel anymore.

5. Lessons learned from ProtoDUNE-1
David Christian

Q: Considering the ASIC cold testing, when will be that?
A: We plan to test everything cold. Currently, chips passed room temperature test also pass the cold test. If that continuous to be the case, we will change plan to only test some chips cold.

The good yield of testing the room temperature chips needs to be so high that we can stop testing everything cold. We don't have a milestone on making the decision.

6. prototyping status and plan
Roger Huang

Q: Will module-0 be ready for FDR? Need to understand the plan leading up to FDR
A: FDR will be the fall and winter before CD2/3 in march 2023. No module-0 for FDR. May have result from CRP2B, and will have some physics results from HD. Could have data from the cold box 4 for the FDR. Need to have the FDR resolved well ahead of CD2/3. Otherwise will delay a year or more.

Q: Will there be a plan to flip the CRP2B upside down and exercise ..?
A: CRP2B will be half the CRP5. There is no plan to ship CRP2B to CERN. The cold box will be mostly used to test the two top CRPs.

7. ASIC lifetime studies
Jianming Bian

Q: Is the test done for very high number thermal cyclings?
A: We don't plan to have many thermal cyclings in DUNE. It takes an hour for a proper thermal cycling, so it's a bit hard to do the test. Data shows that a few cycle doesn't affect the results. Some cold electronics used in the test have been done hundred times of thermal cycling, and no issue has been observed. During DUNE, unless there is a major disaster that the experiment won't go on, the cryostat won't be drained. In real experiment, the filling procedure is even stricter than what have in the test.

8. QA/QC Plan
Shanshan Gao

Q: Have you started to put these into a QC plan?
A: Yes.

Q: (page 28) do you specify other precautions taken during testing to prevent ESD damages?
A: We have short documents, such as grounding. Need to put all into a complete one. These ASICS are sensitive to ESD damages. We have extra precautions to handling them. Have designed the system with extra safety to protect the ASICS. Latest ASICS test doesn't suffer from the ESD. Will work with the experts to have ESD handling procedures documented.

Q: Every FEMB will be tested in liquid nitrogen. If due to mechanical failure, or due to thermal cycling, is there enough evidence from protoDUNE to indicate that just one trip to the cold for every board is enough ? Did you see broken capacitors or broken tracks that due to taking FEMB down to cold?
A: We did a lots of test on several boards with multiple thermal cycles. We didn't see any issues caused by thermal cycling. No specific thermal cycling study has been done because it's time consuming for each thermal cycling.

Q: Is there any test spots in the FEMB front board, such as the output voltage..?
A: Yes. There is signal into FEMB used for monitoring and verifying the functionality of the FEMB, that can be done FEMB installed.

Q: Is there a QA for the CRP interface?
A: As FEMB is installed on the CRP, we will do individual FEMB testing at warm. Then the plan is to submerge the half CRP unit in cryogenic liquid. And then test all the FEMBs prior shipping to south DaKota.

Q: Do you have a process and procedures defined of what you're going to do at every step when something fail the QC process? Will you replace, debug or ship somewhere to have debug?
A: We haven't defined these. It's a good suggestion. If there is broken FEMB, it will be sent to BNL/LBNL for debugging and evaluation.

9. Procurement strategy, cost and schedule
Cheng-Ju Lin

Q: Can you explain the 30% labor cost? It seems low. A similar table from FD1 would be helpful for comparison.
A: The labor cost doesn't include the designing and engineering. All we have is supplying the people to do the test.

Q: If comparing the production fee between FD1 and FD2, what is it?
A: While FD1 have more components to test, should be similar.

Q: According to the current electronics shortage, do you expect there will be an increase on the costs, or schedule slip?
A: This is an issue for FD1 because they need to start early. The plan is to purchase all the FPGAs for the FD1 at CD3A. For FD2, we update the quotes with the market. We don't inflate the cost trying to anticipate where the price might be getting. The cost is based on the actual quotes. It is a risk. If the cost is beyond the budget, we will need to pull the contingency to cover the cost difference. We're paying close attention to the lead time too. For FD2, we need to wait a bit longer before taking any actions.