Overview of BDE System Design, Requirements and Specifications

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Lawrence Berkeley National Lab

FD2 BDE Preliminary Design Review
25 April 2022

Thank you for taking time to serve on the FD2 BDE PDR Committee

Your assessments and recommendations are important to us

Documentation for this Review

REVIEW DOCUMENTATION (list in xlsx):

DUNE FD2 Conceptual Design Report (Chap 4: Charge Readout Electronics)

Requirements and Specifications

Interface Documents

Grounding:

- LBNF/DUNE grounding rules
- Detector grounding rules
- FD2 Bottom Drift Electronics grounding diagram

ASICs:

- LArASIC (Datasheets, Simulation, and MOSIS Reticle)
- ColdADC P2 (Datasheet, Simulation, Testing)
- COLDATA (Datasheet, Design changes, and Testing)

Frontend Motherboard (FEMB) Schematics, Layout, and BOM

Warm Interface Electronics Crate (WIEC):

- Flange board PCB schematic
- WIEC backplane schematic (PTB)

Power and Timing Card (PTC) schmatics, layout, and BOM

Warm Interface Board (WIB)

Mechanical Drawings:

- WIEC assembly drawing
- CE feedthrough flange drawings
- Cross-shaped spool piece
- CE crossing tube and cable support
- CE enclosure box for FEMB

Cable and Wire Documentation:

- Cold bias voltage SHV cables
- Cold miniSAS patch cable (from FEMB to patch panel)
- Cold control, clock, and readout cable
- Cold power cable
- Warm power cable between PTC and Power Supply (PL506)

Production Testing:

- QC test-board schematics (multi-ASICs)
- ASICs Production and QC plans
- ESD Protection Procedures
- Sample LArASIC QC test report

ProtoDUNE-1 lessons learned (updated doc available soon)

Institutional MOUs: FD1, FD2

Link to the documentation page is provided on the Review homepage

https://indico.fnal.gov/event/53072/page/2862-review-documentation

A spreadsheet with links to EDMS is also available

Agenda for this Review

Agenda

Mon 25/04 | Tue 26/04 | Wed 27/04 | Thu 28/04 | All days

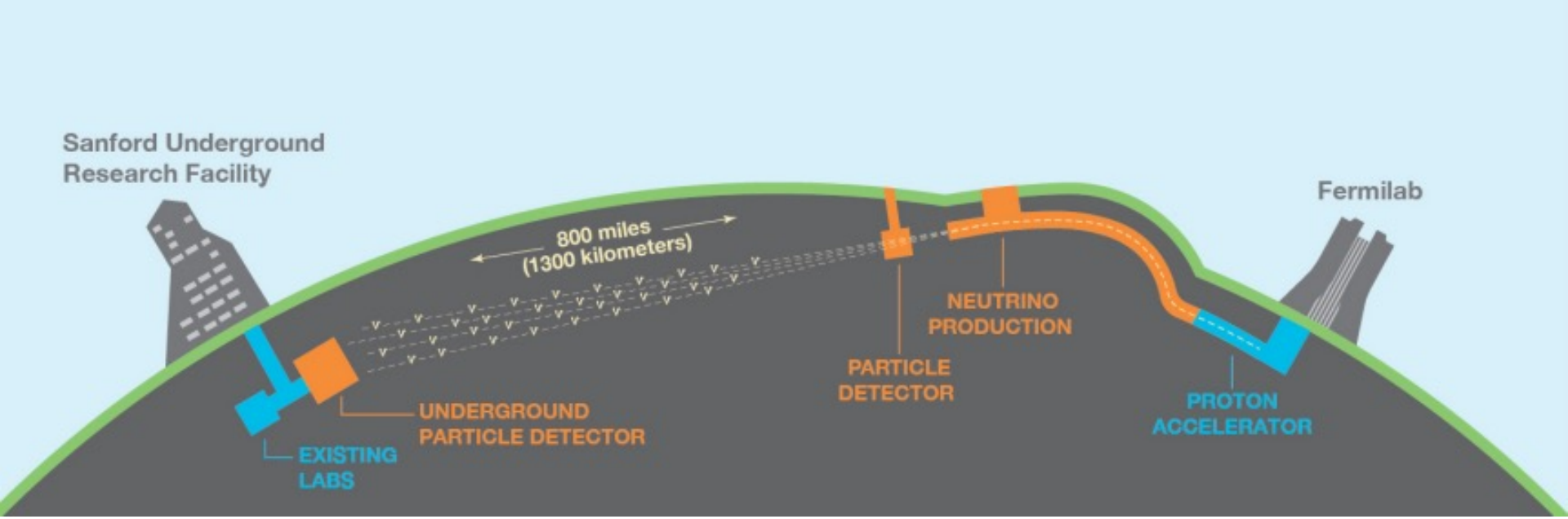
Print | PDF | Full screen | Detailed view | Filter

08:00	**Overview of BDE system design, requirements and specifications**	*Cheng-Ju Lin*	
	Zoom, Remote	08:00 - 08:30	
	BDE interfaces with FD2 consortia	*Vladimir Tishchenko*	
	Zoom, Remote	08:30 - 08:50	
	BDE and CRP interface	*Matthew Worcester*	
09:00	*Zoom, Remote*	08:50 - 09:20	
	Cryostat penetration and FD2 installation	*Manhong Zhao*	
	Zoom, Remote	09:20 - 09:40	
	Discussion		
	Zoom, Remote	09:40 - 10:00	
10:00	**Lessons learned from ProtoDUNE-1**	*David Christian*	
	Zoom, Remote	10:00 - 10:20	
	Prototyping status and plan	*Roger Huang*	
	Zoom, Remote	10:20 - 10:40	
	ASIC lifetime studies	*Jianming Bian*	
	Zoom, Remote	10:40 - 11:00	
11:00	**Break**		
	Zoom, Remote	11:00 - 11:30	
	QA/QC Plan	*Shanshan Gao*	
	Zoom, Remote	11:30 - 12:00	
12:00	**Procurement strategy, cost, and schedule**	*Cheng-Ju Lin*	
	Zoom, Remote	12:00 - 12:30	

Focus of the Review

- FD2 Bottom Drift Electronics is using the same electronics (with minor modifications) as FD1. FD1 TPC electronics have gone through a Preliminary Design Review
- For this review we will focus on the differences between FD2 BDE and FD1:
  - Interfaces
  - Installation of FEMB on CRP
  - MiniSAS cable and patch panels
  - Cryostat penetration
  - FD2 installation
- The prepared talks are selected to address the charge questions

Deep Underground Neutrino Experiment (DUNE)

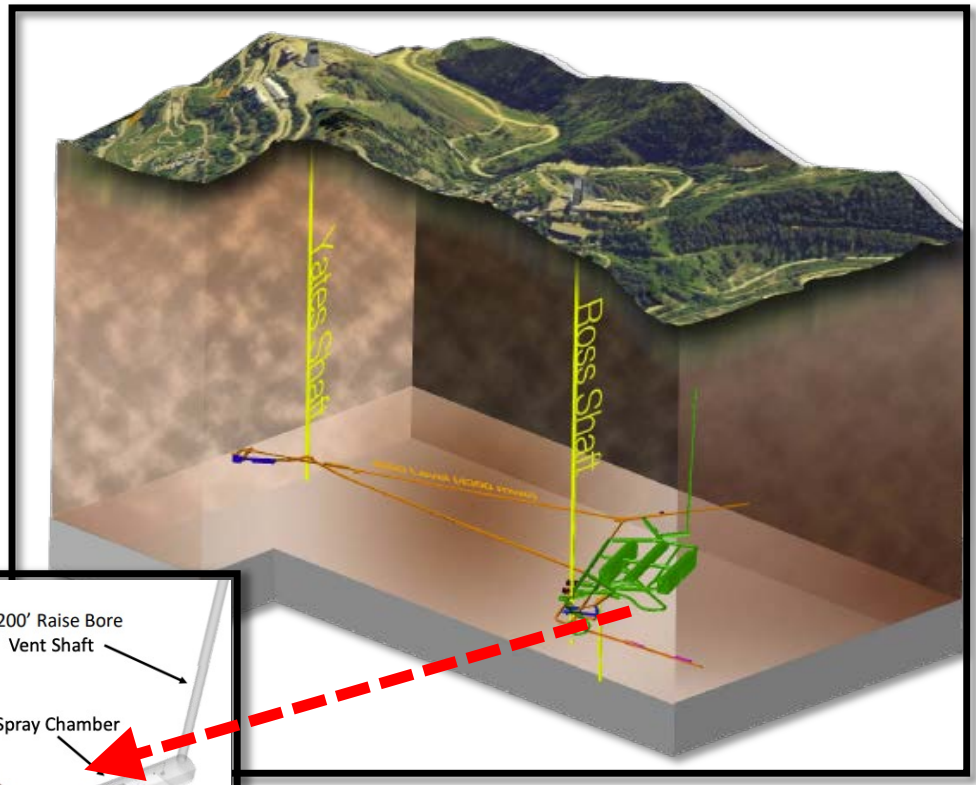


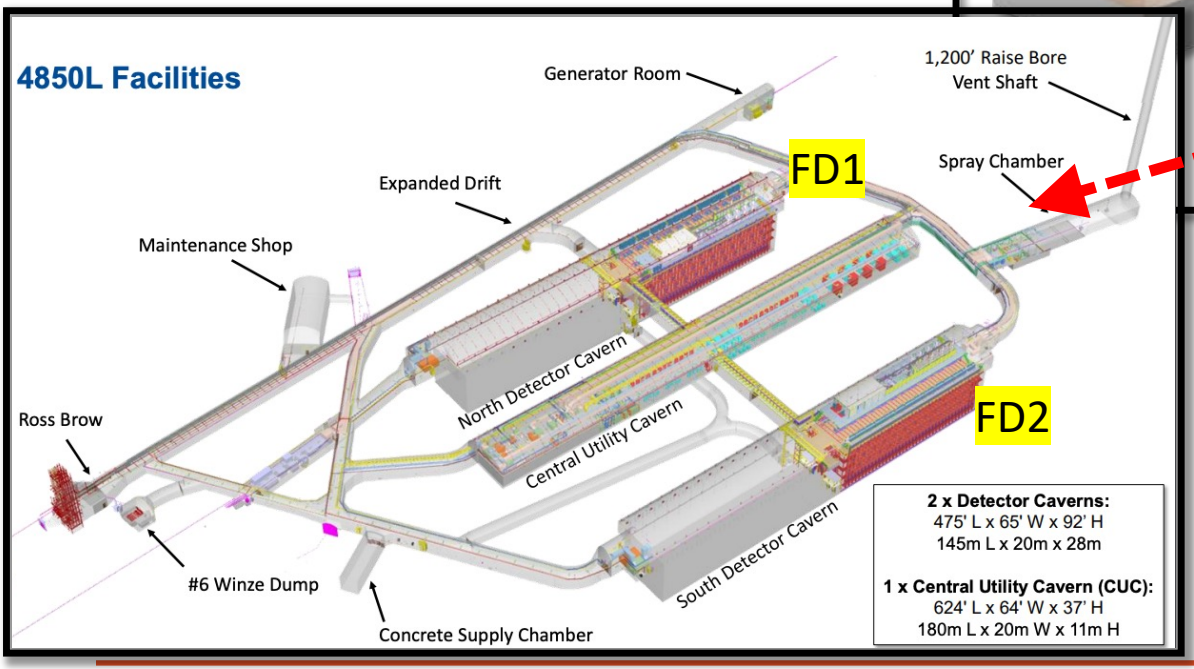
- Future flagship neutrino oscillation experiment
- Three major components: neutrino beamline, near detector, and liquid Argon far detector modules
- Broad physics program: BSM studies supernovae, solar neutrinos, three-flavor oscillation measurements
- >1300 people, > 200 institutions, 33 countries + CERN

DUNE Far Detectors

Four 10-kTon (fiducial) liquid argon detectors

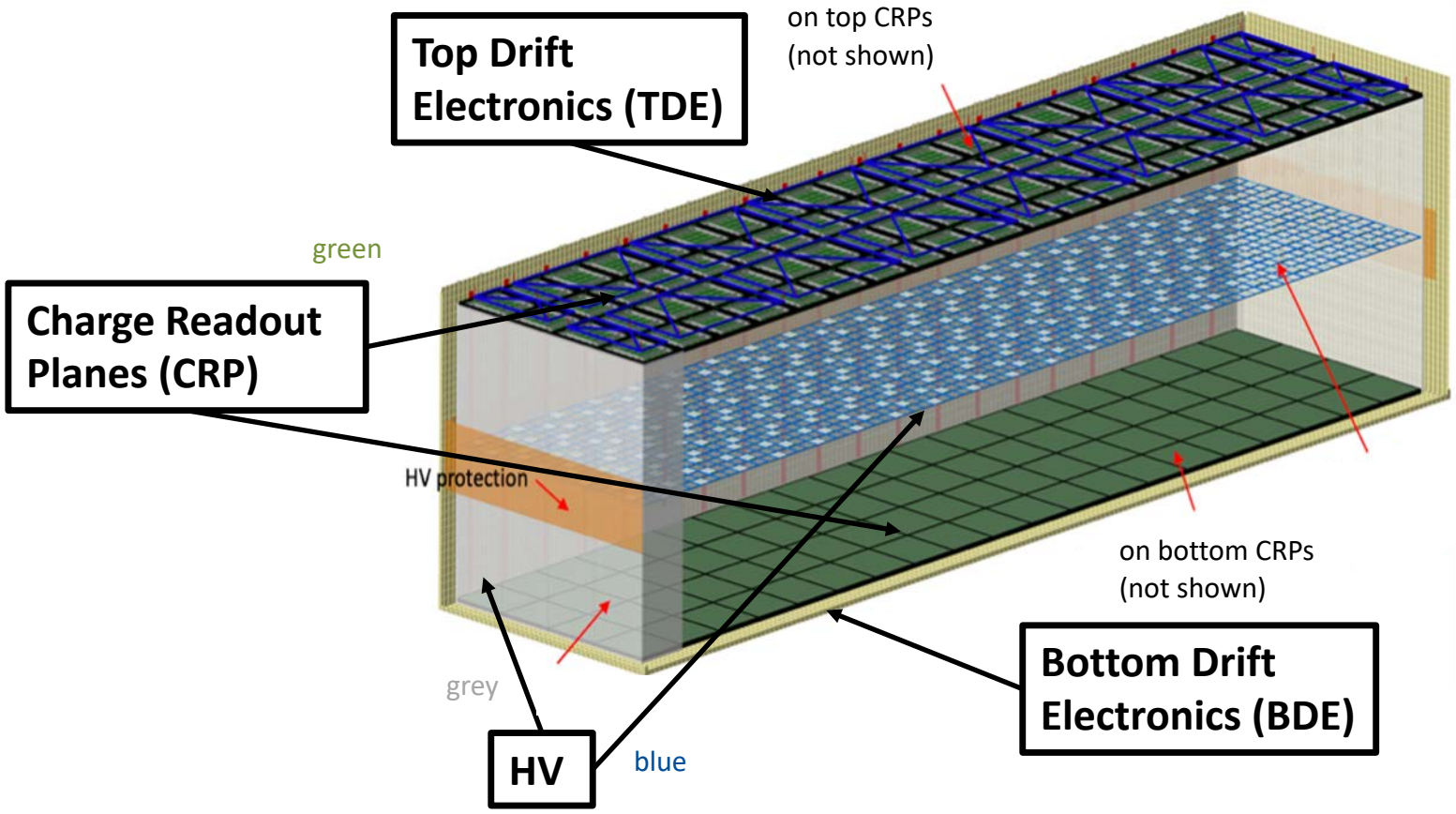
~1500m underground





BERKELEY LAB DUNE

DUNE Far Detector #2

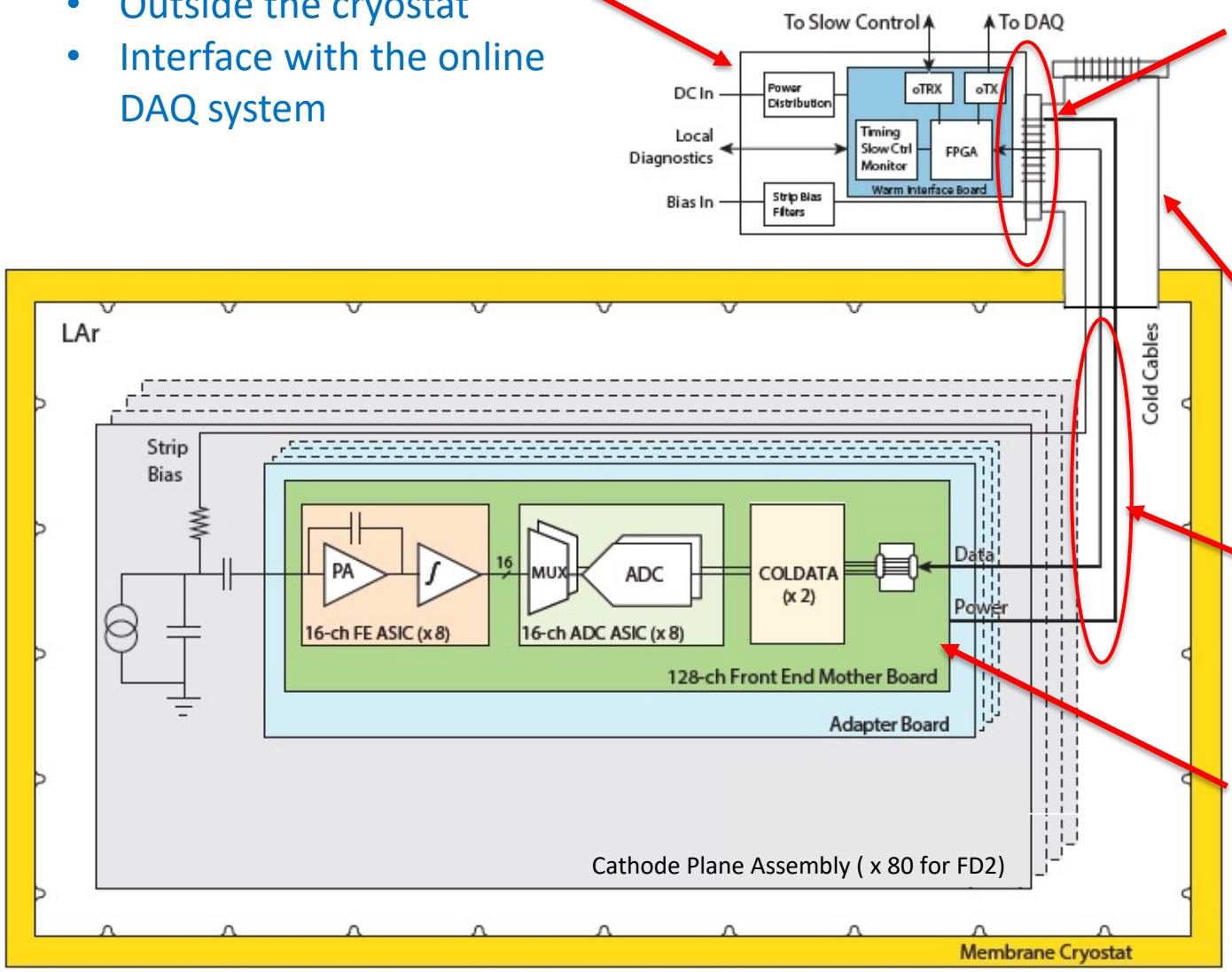


Readout electronics for the 80 CRPs on the bottom drift volume are the same as the readout electronics for FD1

FD2 Bottom Drift Electronics

Warm interface electronics:

- Outside the cryostat
- Interface with the online DAQ system



CE Flange:

- On top of the cryostat
- Connect cold cables to the Warm Interface Electronics

Signal feedthrough:

- 14” conflat
- Cable strain relief

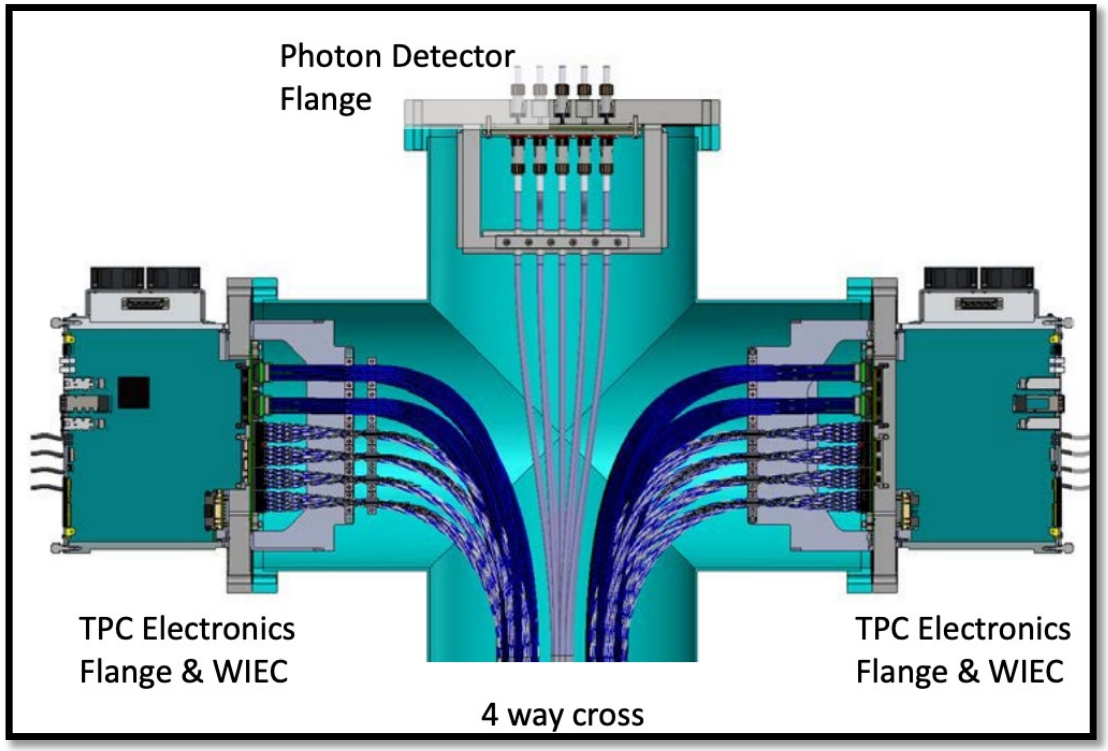
Cold cables: Low voltage and data cable to Frontend motherboard

Frontend Motherboard (FEMB): 128 channels of digitized wire readout enclosed in CE box

Cryostat Penetrations

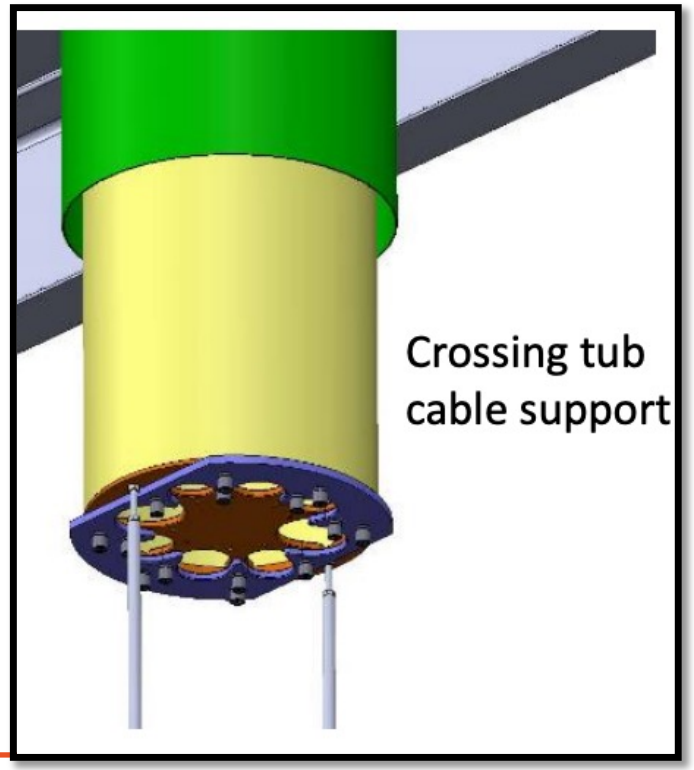
Cryostat penetrations:

- 40 penetrations for FD2
- Each penetration holds two Warm Interface Crates → 2 CRPs

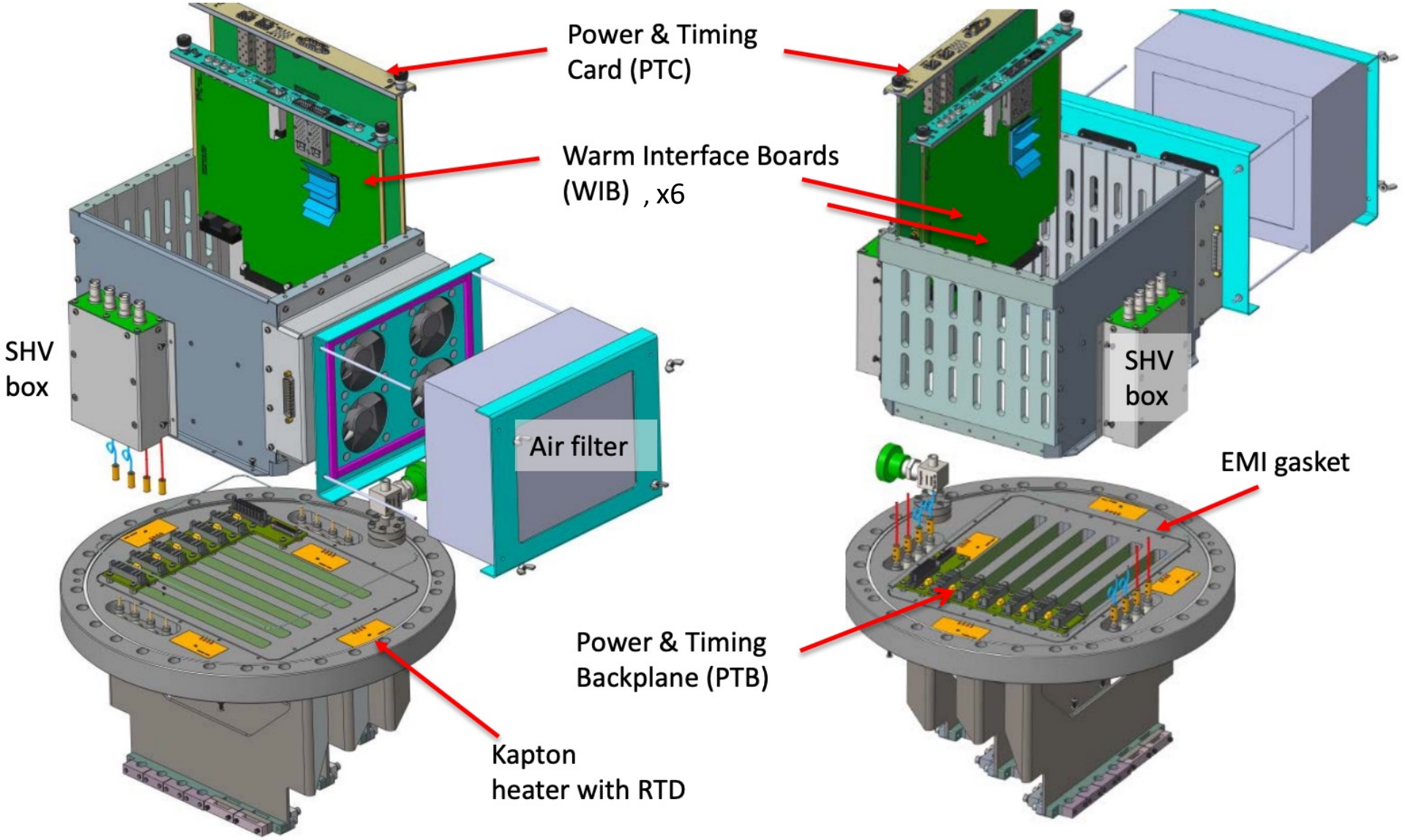


CE Crossing Tube Cable Support:

- At the bottom of the penetration inside the cryostat
- Nominal design is based on FD1
- Exploring alternative design to simplify FD2 installation (see M. Zhao's presentation)



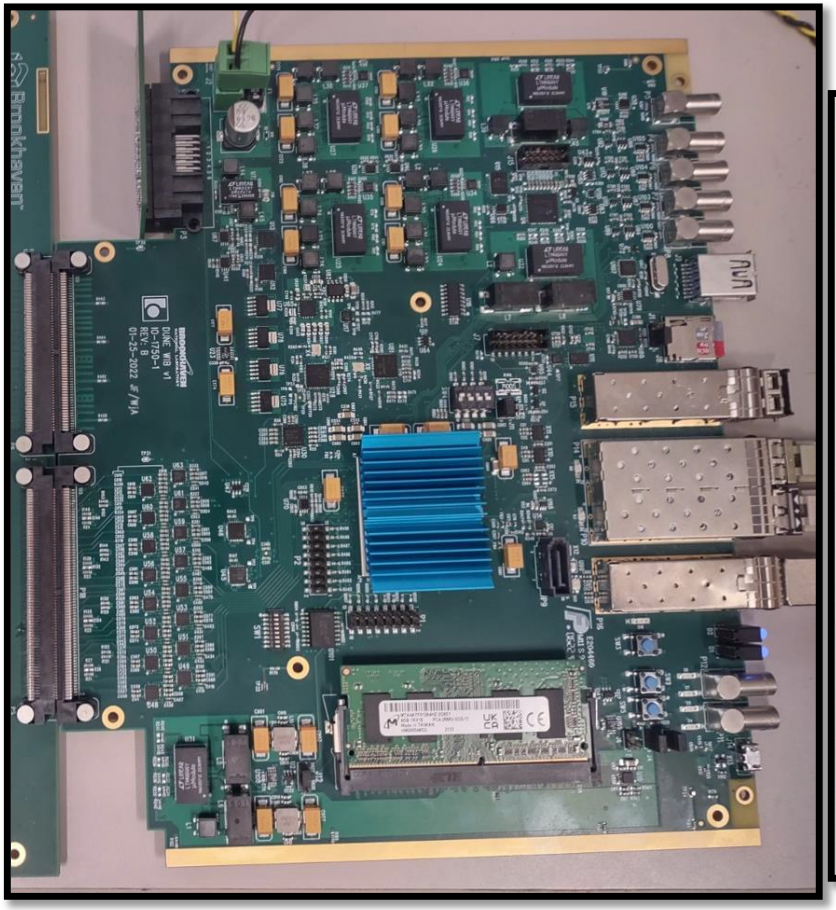
Warm Interface Electronics Crate Assembly



Readout Electronic Boards

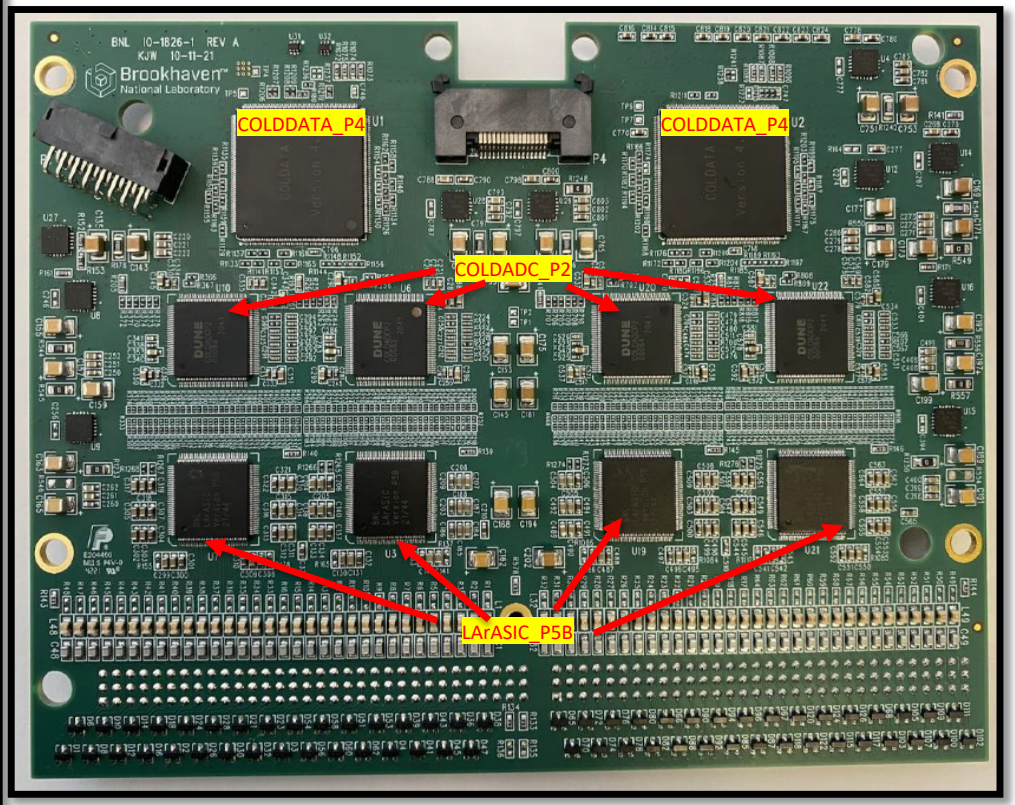
Warm Interface Board (WIB):

- 6 WIBs per WIEC
- Each WIB communicates/powers four FEMBs
- Xilinx Zynq Ultrascale+ FPGA (ZU6CG)



Frontend Motherboard (FEMB):

- 24 FEMBs per CRP
- Each FEMB has three types of custom ASICs:
  - LArASIC P5B (preamp+shaper) x 8
  - ColdADC P2 (2 MS/s digitizer) x 8
  - COLDATA (data serializer + control) x 2



Frontend Motherboard (FEMB)

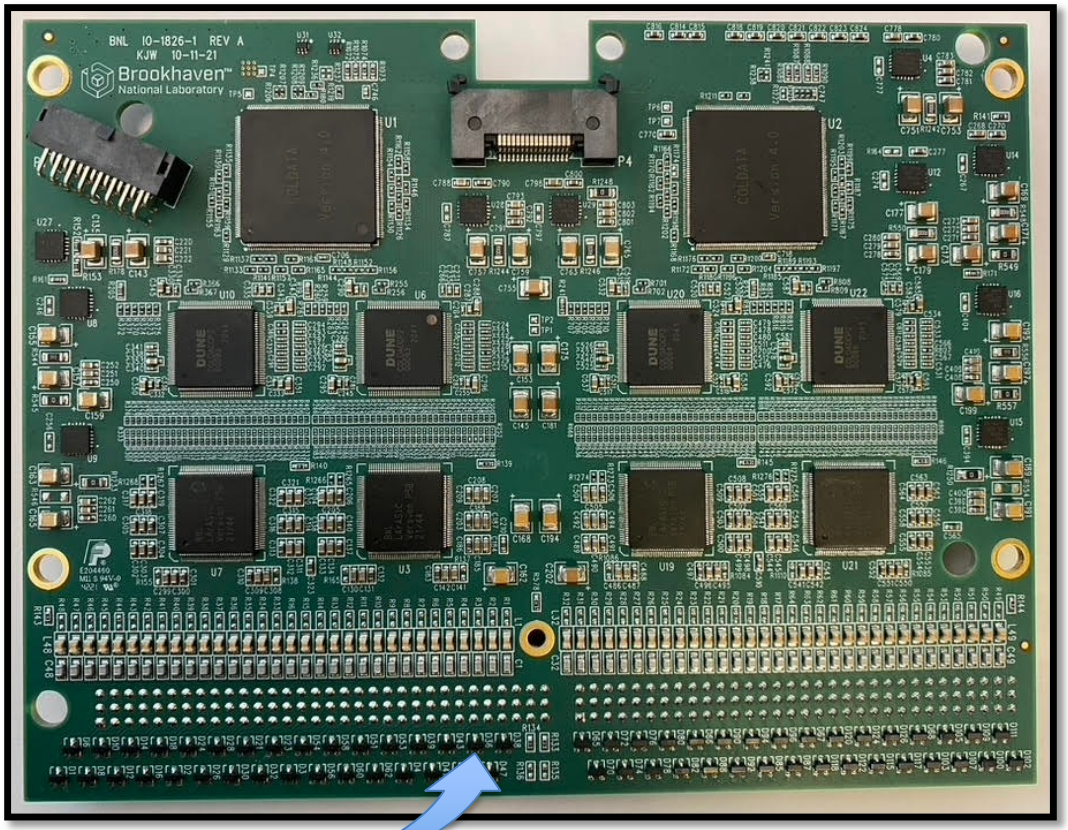
Summary slide from J. Fried's FEMB Presentation (FD1 PDR; Feb 2020)

[LINK to Indico page for DUNE PDR (TPC Electronics ASIC/FEMB)]

Summary

- ProtoDUNE FEMB
  - Running for over 1 ½ years with no failures after commissioning
- ColdADC + FPGA FEMB Prototype
  - Currently in production to be tested on AP7
- LArASIC + ColdADC + COLDATA
  - COLDATA mezzanine schematics are currently under development
    - Will be used to study FEMB clock scheme for data cable
  - Current study of a NON-Mezzanine version of FEMB are very promising

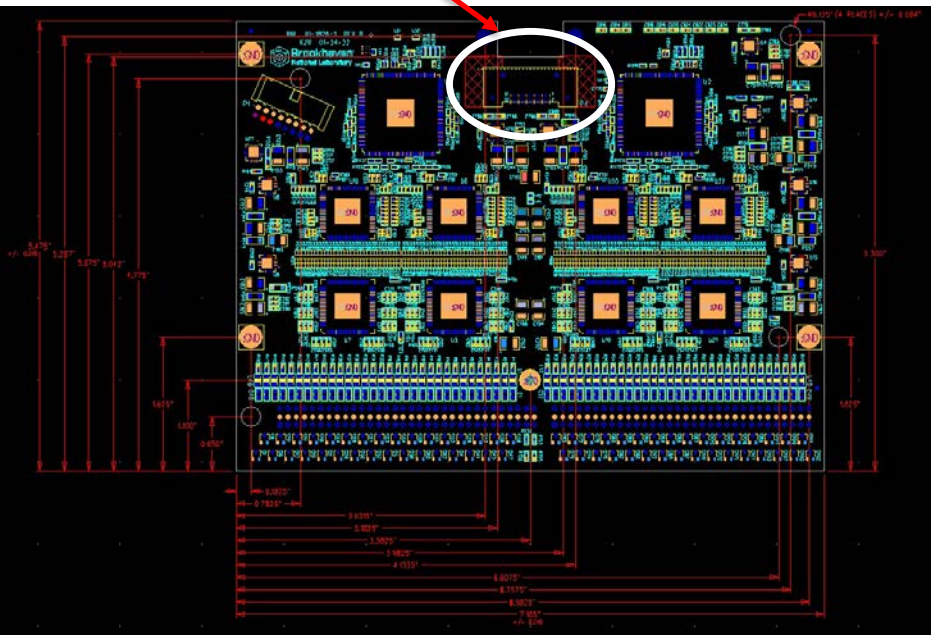
FD1 Monolithic FEMB



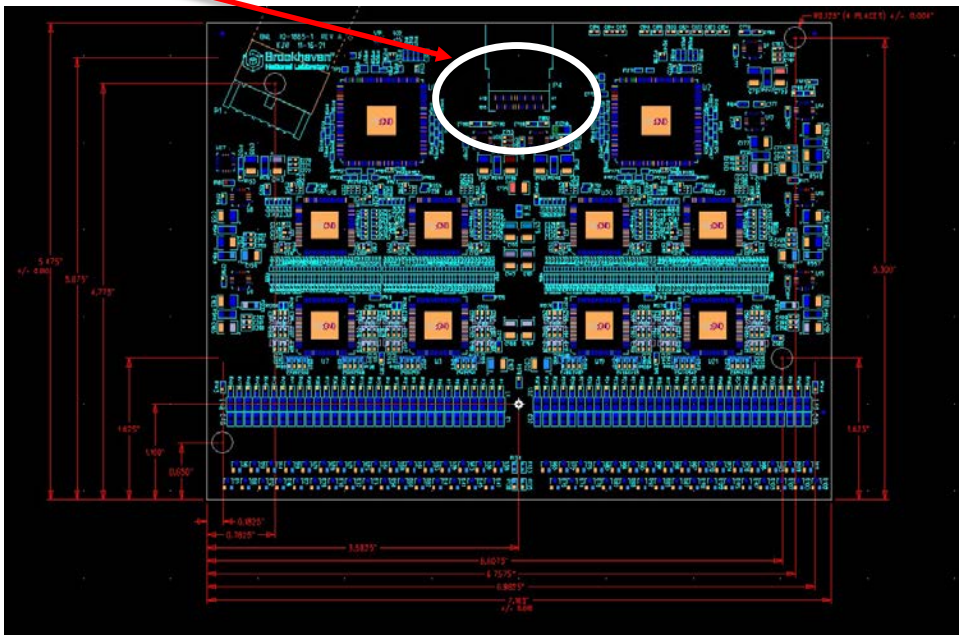
A feasibility study back then is now the baseline design for DUNE

FD1 vs FD2 FEMB

- FD2 FEMB design is available but has not been fabricated
- The main modification for FD2 is on the signal connector.
  SAMTEC (FD1) → MINI-SAS (FD2)



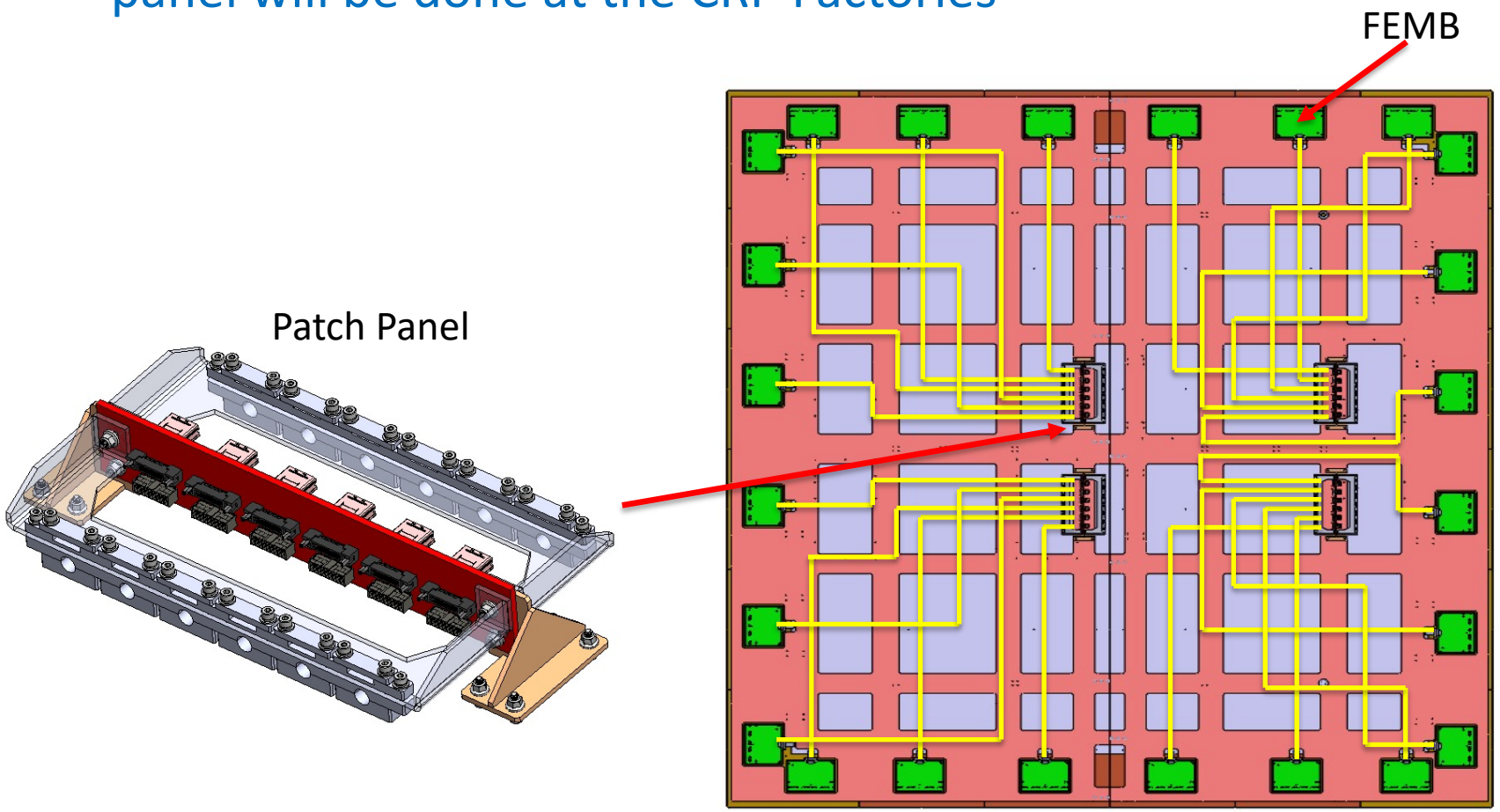
FD1 Monolithic FEMB Layout



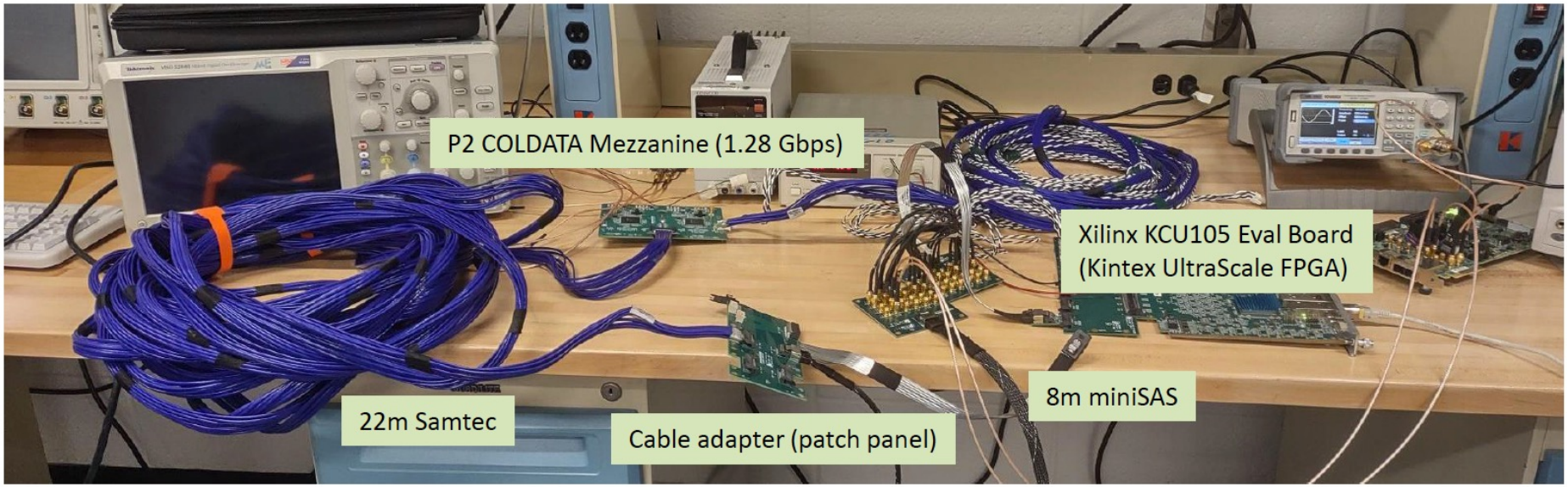
FD2 Monolithic FEMB Layout

CRP Cable Patch Panel

- To simplify cable installation inside FD2 cryostat, plan to use patch panels (See M. Zhao's presentation for more info)
- Installation of patch panels and cables from FEMB to the patch panel will be done at the CRP Factories



Bit Error Rate Measurements



Length	Combination (1.28 Gbps)	BER	RX Pattern
30m	CM + 22m Samtec + ADT + 8m mini-SAS + KCU105	1.073E-14	PRBS 15-bit
29m	CM + 22m Samtec + ADT + 7m Samtec + KCU105	9.555E-15	PRBS 15-bit
37m	CM + 22m Samtec + ADT + 7m Samtec + ADT + 8m mini-SAS + KCU105	2.368E-15	PRBS 15-bit

Note: there is 1m SMA cable that is not taken into account for total length

- BER test was done at room temperature, expect to see better performance at cold temperature

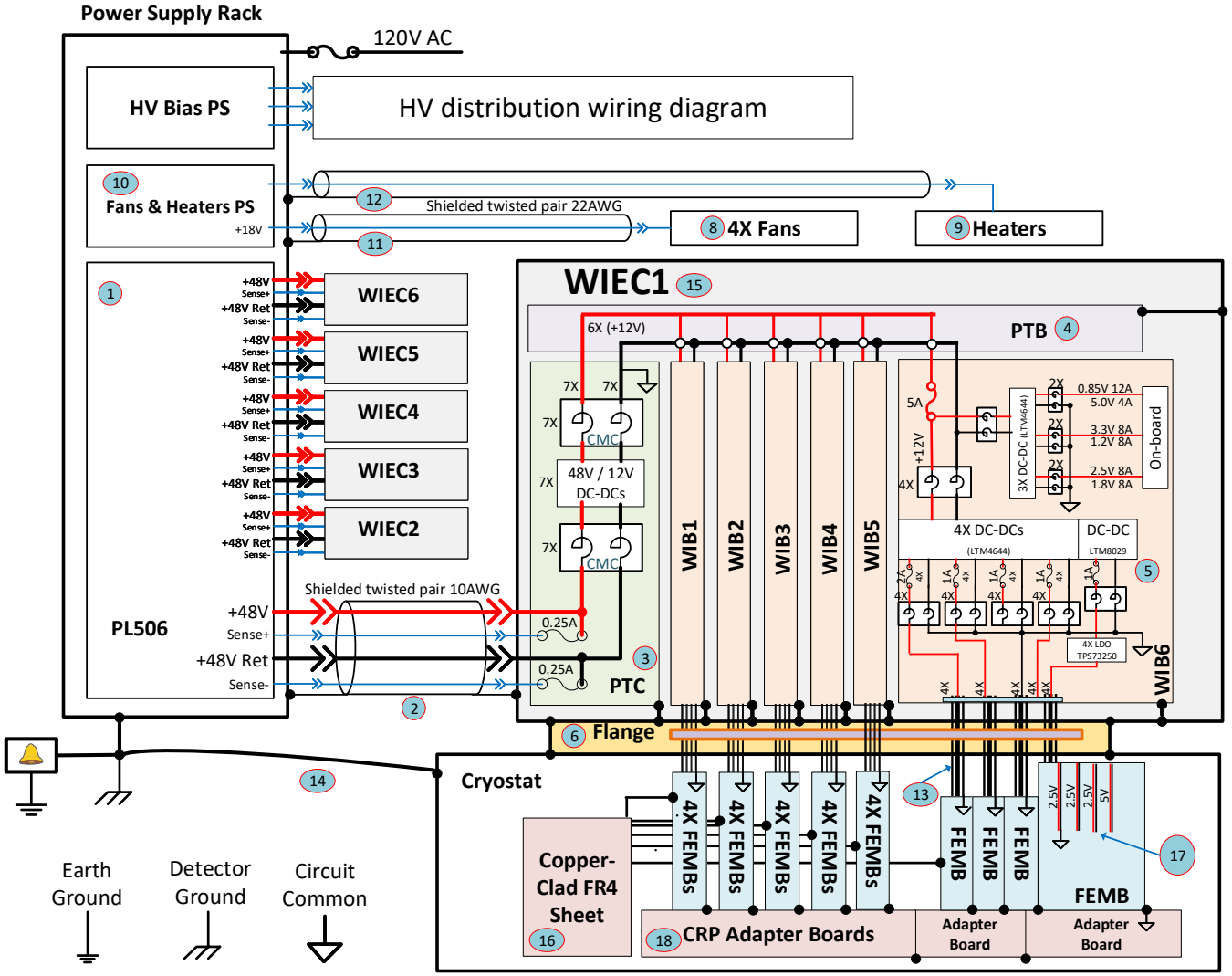
For FD2 BDE, the nominal cable length is ~25 m

FD2 BDE Stats

BDE Subsystem	Quantity for FD2
# of CRP to instrument with BDE	80
Total # of readout channels	245,760
# of cryostat penetrations	40
# of Warm Interface Crates	80
# of Warm Interface Boards	480
# of Power and Timing Cards	80
# of Frontend Motherboard	1920
# of LArASIC ASIC	15,360
# of ColdADC ASIC	15,360
# of COLDATA ASIC	3,840

FD2 BDE Grounding Diagram

Following guidance from the Grounding & Shielding Committee as documented in [EDMS#2095958]

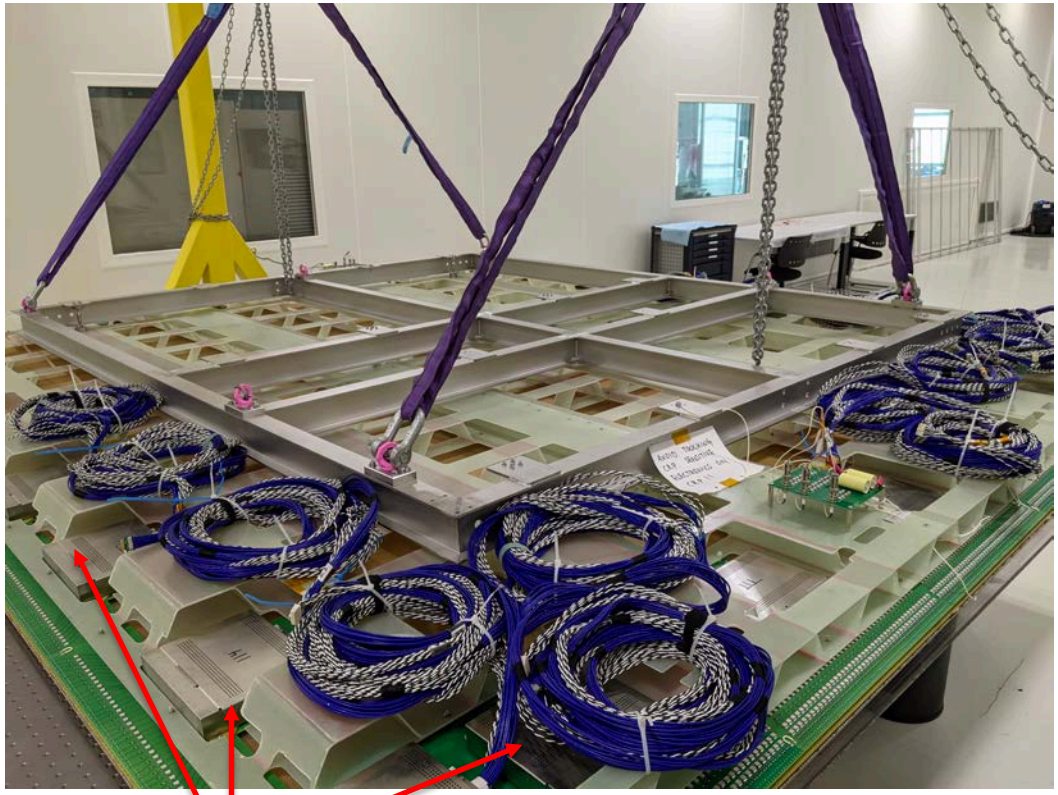


1: Weiner PL506 Power Supply
2: 48V power cable
3: PTC (Power and Timing Card)
0.25A Fuse P/N: 3404.0006.11
Choke P/N: PLT10HH501100PNL
4. PTB (Power and Timing Backplane)
5: WIB (Warm Interface Board Version 3.0)
5A Fuse P/N: 3404.0017.11
2A Fuse P/N: 0468002.NR
1A Fuse P/N: 0468001.NR
Choke P/N: PLT5BPH5013R1SNL
6: Flange Board
7: FEMB (Monolithic Front End Motherboard)
8: Fans box
Fans are electrical isolated from WIEC
9: Heater
Heater is electrical isolated from WIEC
10: Fans & Heater power supply
11: Fans power cable (shielded)
12: Heater power cable
13: 7m cold power cable
14: Grounding cable
15: Warm Interface Electronics Crate (WIEC)
16: Copper sheet underneath the CRP composite frame
17: Voltage measured at FEMB
18: Adapter boards for the FEMBs to plug into
Note: Each adapter board takes 1 or 2 FEMBs, but adjacent boards are electrically and mechanically interconnected

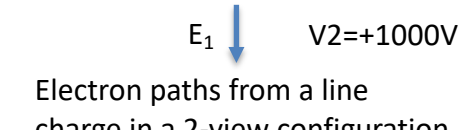
Notes
(1) Fans and heaters are isolated from WIEC
(2) PTB is mounted with the brass standoffs as a grounding connection
(3) The grounding connection between WIBs and WIEC is through front panels and side bars
(4) The grounding connection between PTB and WIEC is through front panels and side bars
(5) Flange (and flange board) is the place that the FEMB circuit common is referenced to the cryostat (detector ground)

Prototyping at CERN Cold Box

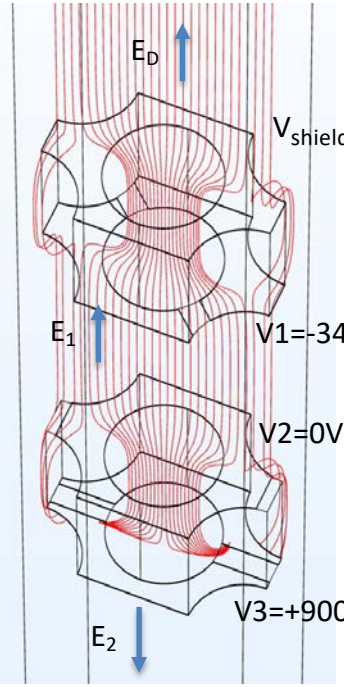
- CRP#1 was a hybrid design (half TDE, half BDE)
- Successfully operated in the CERN cold box last fall/winter



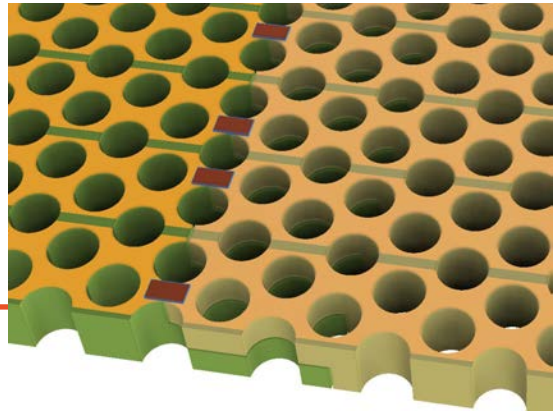
Same FEMB as FD1



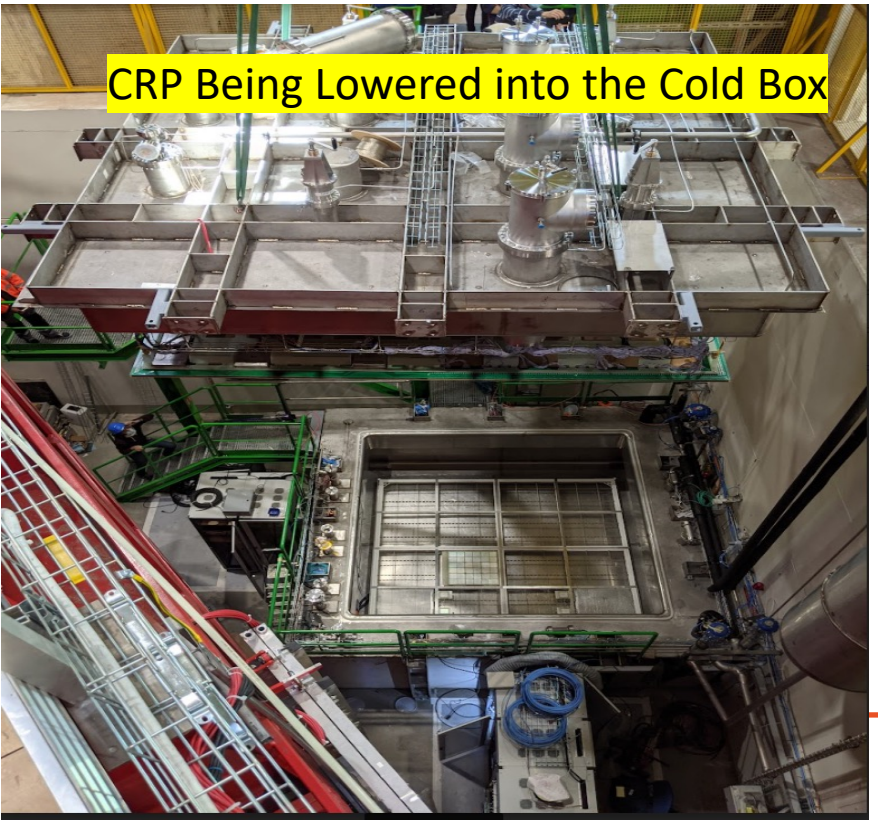
Electron paths from a line charge in a 2-view configuration

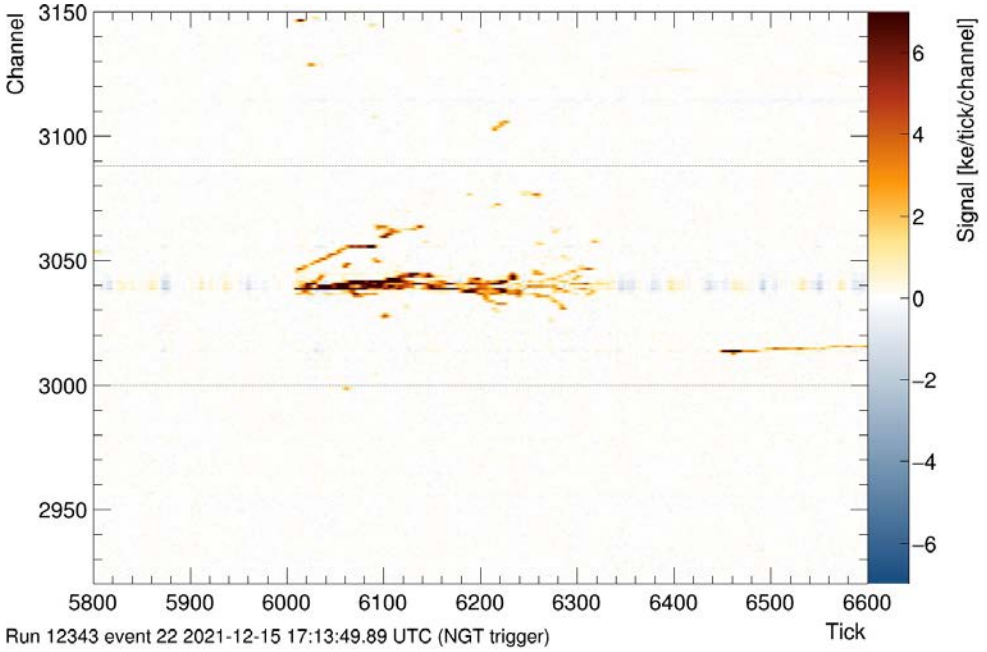


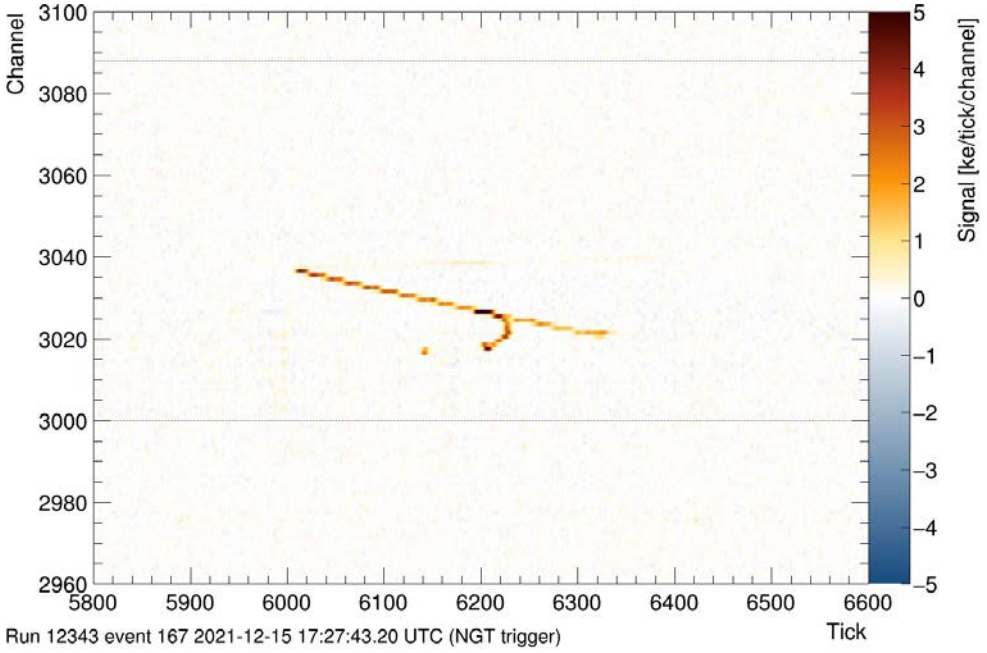
Electron paths in a 3-view configuration with a shield plane facing the cathode.



CRP#1 Cold Box Test at CERN







BDE Requirements/Specifications

Executive Board held requirements for FD1-HD are also valid for FD2-VD

TDR ID	Name	Primary Text	Value
SP-FD-2	System noise	The total system noise seen by each wire should be no more than 1000 enc of noise. It is expected that random noise on the FE amplifier will be the dominant contribution to the total system noise.	<1000 electrons
SP-FD-13	Front-end peaking time	The FE peaking time shall be set so as to optimize vertex resolution.	1 microsecond (goal: adjustable to be able to take advantage of lower noise if the noise depends on peaking time)
SP-FD-14	SP signal saturation level	~500,000 electrons	~500,000 electrons (goal: Adjustable so as to see saturation in less than 10% of beam-produced events)
SP-FD-19	ADC sampling frequency	The ADC sampling frequency shall be set so as to extract maximal information without unnecessarily increasing data rate.	~ 2MHz
SP-FD-20	Number of ADC bits	The ADC shall digitize the charge deposited on the wires with 12 bits precision	12 bits
SP-FD-21	SP cold electronics power consumption	The SP CE power consumption shall remain below 50 mW/channel	< 50mW/channel
SP-FD-25	Non-FE noise contributions	All non-FE noise contributions shall be much lower than the targeted system noise level	<< 1000 electrons

BDE Requirements/Specifications

- Most Technical Board held requirements for FD1 TPC Electronics are also valid for FD2 Bottom Drift Electronics
- Combination of requirements, design choice and specifications

TDR ID	Name	Primary Text	Value
SP-ELEC-2	Gain of the SP TPC elec. front-end amplifier	Gain of the front-end amplifier	10 mV/fC (adjustable in the range of 5-25 mV/fC)
SP-ELEC-3	SP TPC elec system synchronization	Maximum time difference between ADC samples on different wires	16 ns
SP-ELEC-4	Number of channels per SP TPC elec front-end motherboard	Number of channels in each front-end motherboard	128
SP-ELEC-5	Number of links between the SP TPC elec FEMB and the WIB	Maximum number and speed of links used for data transmission between the FEMB and the WIB	4 at ~ 1.28 Gbps
SP-ELEC-6	Nunber of SP TPC elec FEMBs per WIB	Number of FEMB connected to each WIB	4
SP-ELEC-7	Data transmission speed between the SP TPC elec WIB and the DAQ backend	Each WIB should transmit data to the DAQ backend at a speed of 10 Gbps	10 Gbps

BDE Requirements/Specifications

- Additional requirements or specifications under consideration at the CE Consortium level
- Listing sample requirements here. See EDMS#2590797 for a complete list
- Data transmission:
  - FEMB can drive signal over cold cable > 25m (open eye diagram)
- ADC linearity requirements: INL, DNL and ENOB
- Warm interface crates, WIB, and PTC requirements:
  - WIB calibration
  - Clock jitter from WIB to FEMB
  - PTC output voltage ripple, etc.
- Power supply requirements:
  - Current and voltage requirements
  - Noise ripple, V/I readback rate, etc.
- Offline physics requirements:
  - ADC overflow logic
  - Double pulse resolution
  - Saturation recovery
  - Channel-to-channel cross talk, etc.

Design Review Status

FD2 BDE is using the same electronics as FD1 with some minor modifications. All FD1 TPC electronics subsystem have gone through at least the Preliminary Design Review:

- PDR: TPC Electronics ASIC/FEMB (27-28 Feb 2020)
  https://indico.fnal.gov/event/22423/
- PDR: Cold Electroncs WIB and System (17-Mar to 7-Apr 2020)
  https://indico.fnal.gov/event/22807/
- CDR: FD2 Bottom Drift Electronics (28 May 2021)
  https://indico.cern.ch/event/1038739/
- FDR: TPC electronics ASICs (21-21 Jul 2021)
  https://indico.fnal.gov/event/49771/
- PRR: LArASIC (7-8 Mar 2022)
  https://indico.fnal.gov/event/53072/

Recommendations from BDE CDR (i)

Eight recommendations from the Conceptual Design Review (28-June-2021):

1) **Verify signal performance and reliability in warm and cold of the patch panel for validation in FD2-VD cold box tests:**

   Signal integrity has been verified in benchtop studies. The patch panel design will be tested on CRP#2B (half CRP) in LN_2 in early fall. Integration test on a full-size CRP in FD2-VD cold box is scheduled for late 2022

2) **Continue to advance ASIC/FEMB production and validation for ProtoDUNE-II-HD and FD2-VD cold box tests:**

   Production version of FEMBs have been tested. First batch of FEMBs for APA#1 are at CERN for ProtoDUNE-2-HD. Will fabricate the FEMBs for FD2-VD cold box test after the completion of the production run for ProtoDUNE-2-HD

Recommendations from BDE CDR (ii)

3) Work with DAQ, TDE, and PDS to understand the implications of the choices of the timing system before preliminary design:

Decision for BDE is to use the same timing system as FD1

4) Have the Grounding & Shielding committee review and sign off on the cold box grounding plan before fall 2021:

Grounding & Shielding Committee reviewed the grounding plan for the VD Cold box #1. We are continuing to work with the Grounding & Shielding Committee as we update the grounding scheme for BDE

5) Continue to explore optimization of the channel count for each CRU for FD2-VD cold box testing:

FD2 Tech Board approved the optimized CRP strip count. The nominal CRP now has 3072 channels

Recommendations from BDE CDR (iii)

6) **Work with CRP, HV, TDE to solidify an agreement on bias and termination voltage/cabling scope before preliminary design:**

   Agreement is for HVS Consortium to handle all bias supplies

7) **Work with CRP, HV, TDE, and DAQ to develop interface documents before preliminary design:**

   Interface documents are available. Most interface documents are still in draft form

8) **Many activities are planned at CERN this year, please provide a list of needed personnel resources by early summer 2021:**

   2.25 FTE of scientific personnel are permanently based at CERN starting in May 2022. During peak installation for HD and VD, additional scientists and engineering personnel will be onsite

FD2 BDE Risk Registry

- Four BDE risks in the registry
- Mostly to cover personnel shortage concerns
- Will likely add a few more risks to address problems that may encounter during FD2 installation (e.g. items damaged during installation)

RI-ID	Title	Probability	Cost Impact	Schedule Impact
RT-131-FDC-FD2-007	FD2 BDE Insufficient un-costed labor at SURF for installation	30 %	97 -- 194 -- 292 k$	0 months
RT-131-FDC-FD2-019	FD2 BDE Insufficient personnel to perform QC of cold electronic components during production	30 %	25 -- 50 -- 75 k$	1 -- 2 -- 3 months
RT-131-FDC-FD2-022	FD2 ASICs production delay	30 %	70 k$	0 months
RU-131-FDC-FD2-005	FDC Fluctuations in the exchange rates cause variations of the costs of detector componen	100 %	-750 -- 750 k$	months

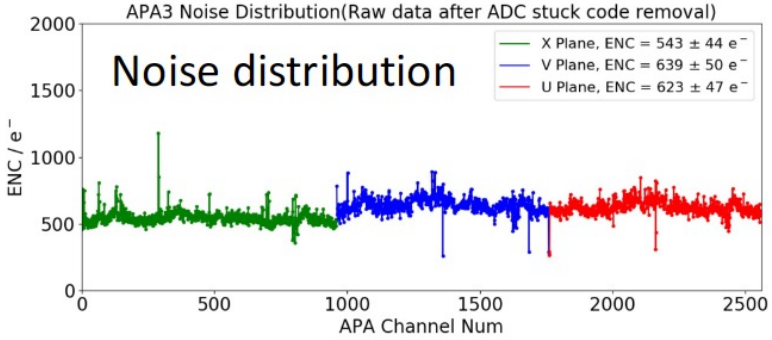
- In addition, there are a number of risks for FD1 TPC electronics that are relevant for FD2 (e.g. redesigning boards due to unavailability of parts). Those risks are not included separately in FD2 to avoid double counting risks

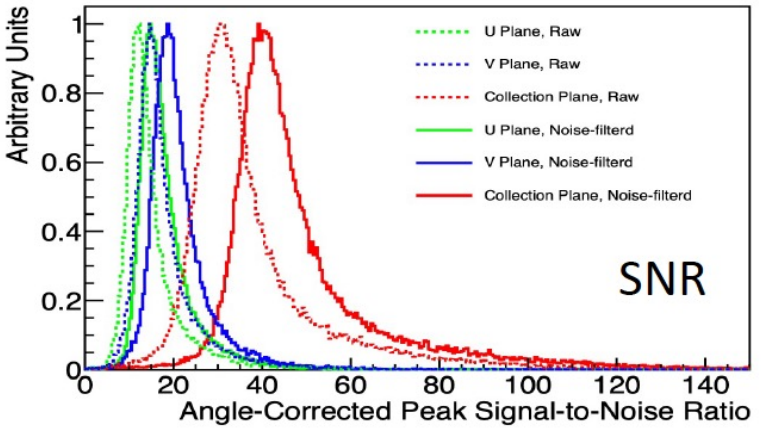
Thank You !

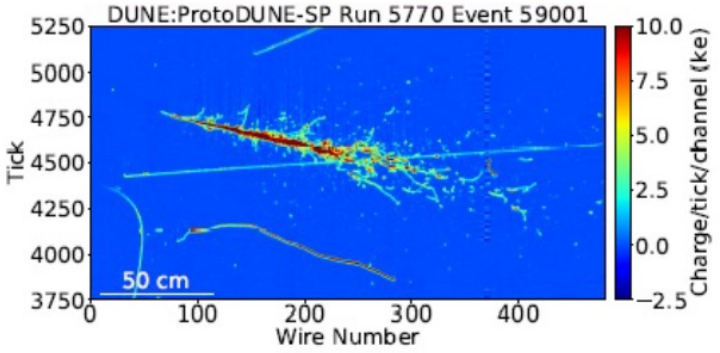
BACKUP SLIDES

ProtoDUNE Run-1 Performance

- **High yield**
  - 99.74% (15320 of 15360) of TPC channels are active
    - Only 4 inactive cold electronics channels when commissioning started
    - 2 more inactive cold electronics after >1 year running
- **Low noise**
  - 92.83% TPC channels are good with excellent noise performance
    - Raw data: Collection ENC ~560 e^-, Induction ENC ~670 e^-
- **Good stability**
    - No measurable degradation is observed over a year
- CE is demonstrated as the promising technology towards DUNE LArTPC
  - Final design will be verified in ProtoDUNE-SP RUN-II in 2022





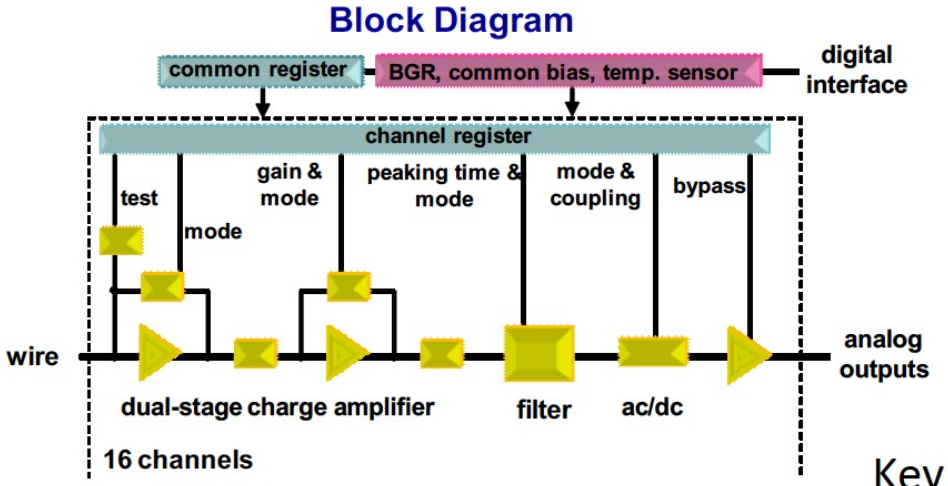


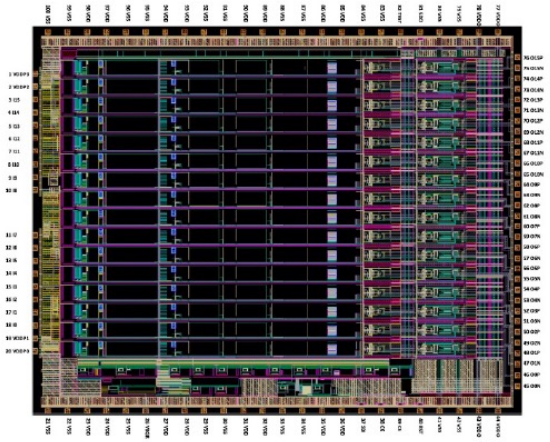
A 6 GeV/c electron candidate

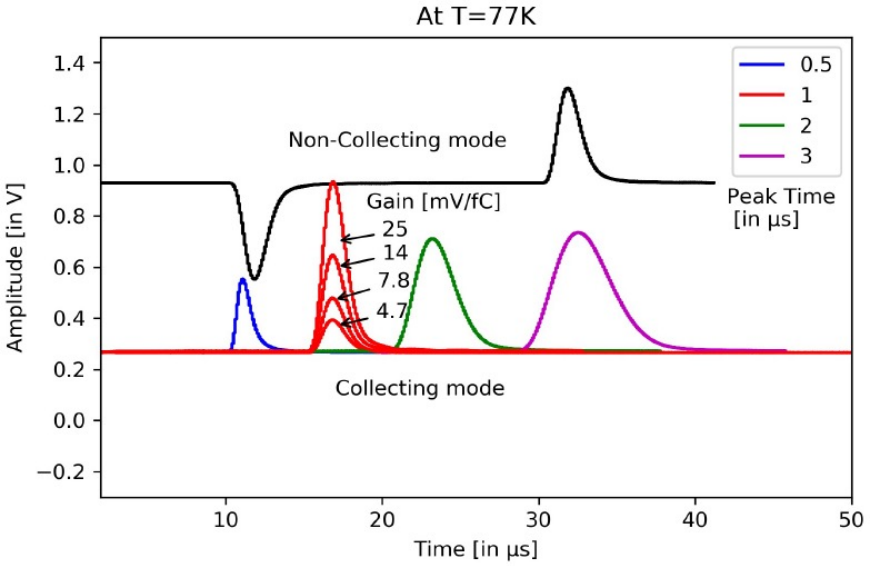
BERKELEY LAB DUNE

LArASIC ASIC

16-ch programmable charge amplifier working at 77-300K for neutrino experiments







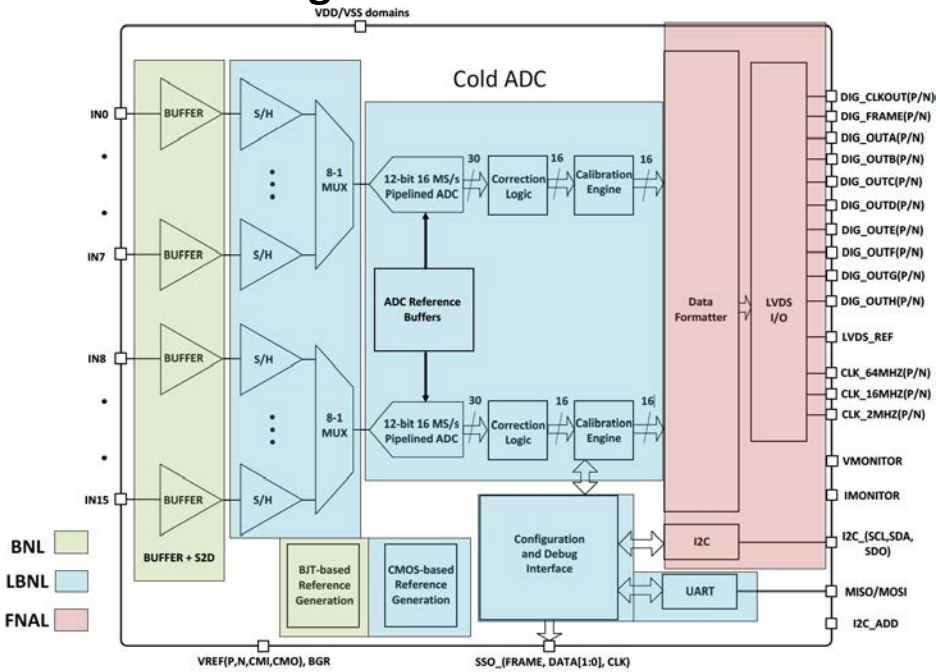
Measured waveforms at cold

Key Features

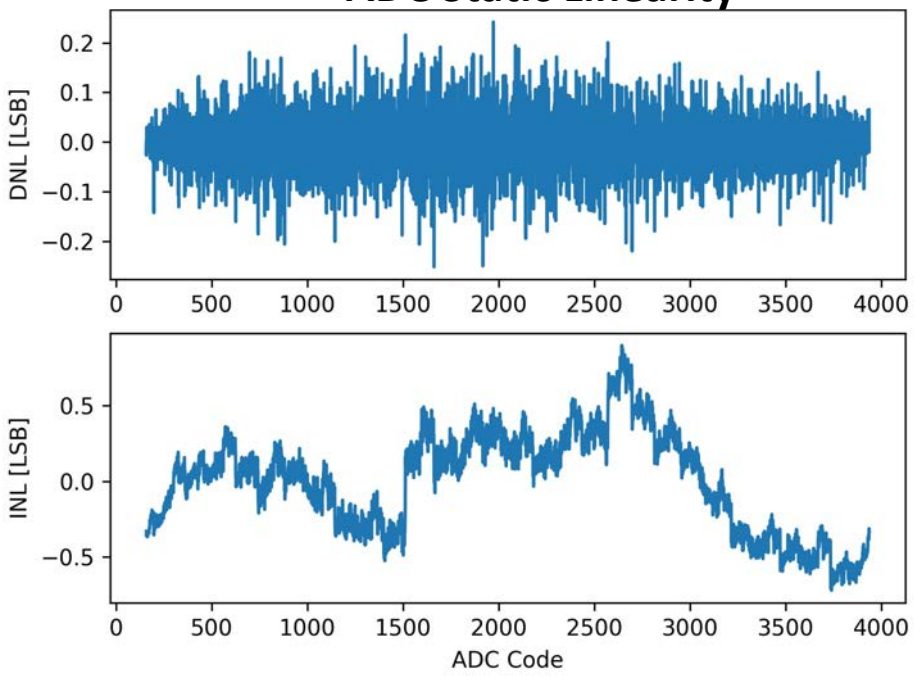
- Two-stage charge amplifier, high-order filter (5th)
- Adjustable reset quiescent current settings
- Adjustable gain: 4.7, 7.8, 14, 25 mV/fC
- Adjustable peaking time: 0.5, 1, 2, 3 µs
- Selectable collection/non-collection mode
- Rail-to-rail analog signal processing
- Bandgap referenced (BGR) biasing circuits
- Integrated temperature sensor
- Integrated 6-bit adjustable range pulse generator
- SPI interface for 144 configuration registers
- Technology CMOS 0.18 µm, 1.8V
- Leverages the existing cold models

ColdADC ASIC

ADC Block Diagram



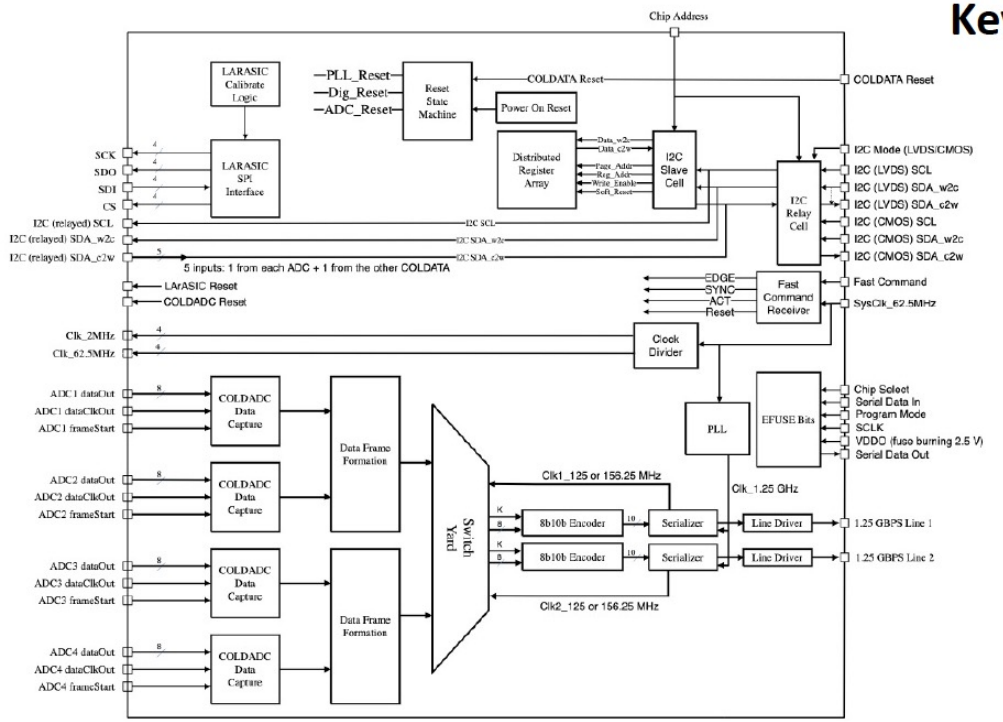
ADC Static Linearity



Key Features

- 16-channel, 12-bit 2MS/s digitizer ASIC for 77-89K
- Two 15-stage piped-line ADCs
- Designed by joint team from LBNL, FNAL, and BNL
- Low-noise and long lifetime operation in LAr
- 65nm CMOS process, 9 metal stack
- Digital self-calibration for interstage gains
- Chip size: 6860 μm x 7610 μm

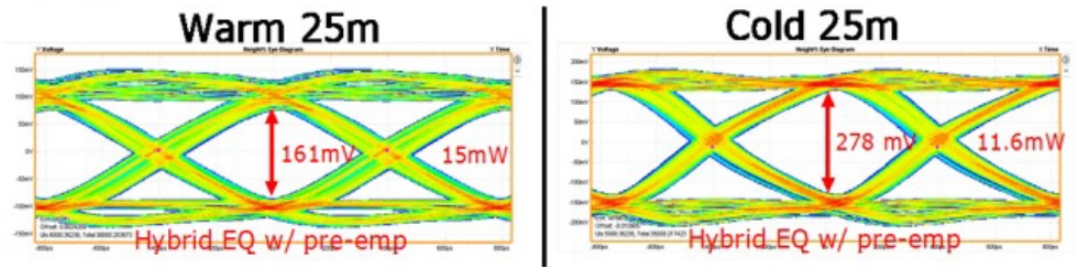
COLDATA ASIC



Key Features

- Designed by Fermilab and SMU
- Design for cryogenic, long lifetime operation
- Control 4 ColdADCs and 4 LArASICs
- Accept data from 4 ColdADCs
- Format ADC data (truncate to **12 or 14** bits) & pack into an array of 8-bit words
- Combine packed arrays from pairs of ADCs into 2 output data frames
- Encode the output data using 8b10b
- Drive the output data to a WIB at 1.25 Gb/s
- Digital-On-Top design methodology
- 65nm CMOS process, 9 metal stack
- Chip size: 7730 µm x 7730 µm
- Leverages the existing cold models

BER < 10^{-15}



Line driver eye diagram measurement result