

Interfaces with other subsystems

DUNE Preliminary Design Review:
Bottom Drift Electronics
April 25-27, 2022
V. Tishchenko

Purpose

This talk addresses Charge Question 2:

Have interfaces with other detector components been addressed and documented? Do risks of design changes in other systems have appropriate mitigation strategies?

- BDE – Bottom Drift Electronics
- CCM – Configuration Control and Monitoring system (part of DAQ).
- CE Box – Cold Electronics Box
- CRP – Charge Readout Plane (consists of two CRUs)
- CRU – Charge Readout Unit
- DAQ – Data Acquisition System
- DDSS – DUNE Detector Safety System
- FEMB – FrontEnd MotherBoard
- FPGA – Field Programmable Gate Array
- HVS – High Voltage System
- PTB – Power and Timing Bus
- PTC – Power and Timing Card
- SC – Slow Control system
- TDE – Top Drift Electronics
- WIB – Warm Interface Board
- WIEC – Warm Interface Electronics Crate


Interfaces with other detector components

FD2-VD Interface matrix: <https://edms.cern.ch/document/2620747>

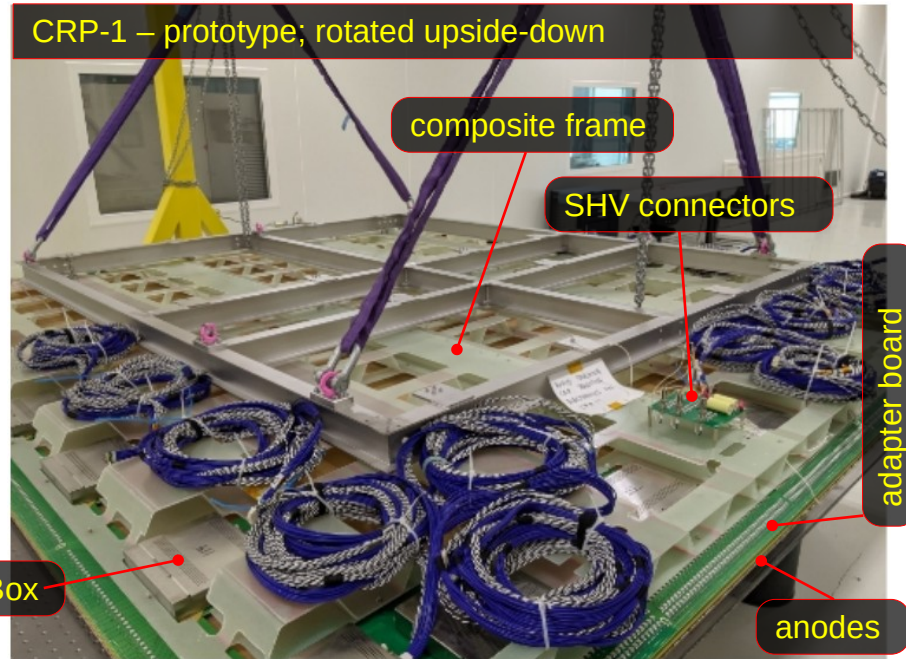
System	Interface Document	
	# & link	status
CRP	2618995	in work
TDE	2618997 (no interface)	
PDS	2618994	in work, advanced
HVS	2726647	in work
DAQ/SC	2694691	released
CALCI	2618996 (no interface)	
FD2-COM	no interface	
I&I	2694691	in work
DDSS		future

Interface with CRP

<https://edms.cern.ch/document/2618995>

 <p>DUNE Interface Document:</p> <p>Vertical Drift CRP/ Bottom Drift Electronics</p>			
Document identifier:		Created:	Page: 1 of
EDMS id 2618995		Modified:	Rev. No.:

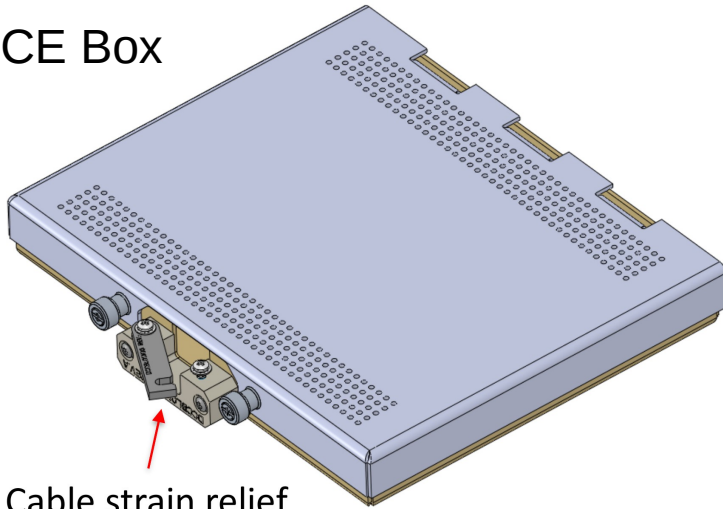
<p>DUNE Interface Document:</p> <p>Vertical Drift CRP / Bottom Drift Electronics</p> <p>This document formalizes the interface between the DUNE FD2-Vertical Drift Charge Readout Planes (CRP) and Bottom Drift Electronics (BDE) consortia. It defines the interfaces for both CRP and BDE to complete the design, fabrication and installation of their subsystems. This document describes the elements of the scope of each subsystem at the interface between them.</p> <p style="text-align: center;">https://edms.cern.ch/document/2618995</p>		
Prepared by:	Checked by:	To be approved by:
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Distribution List		



- Each Bottom CRP is read out by 24 FEMBs
- Each FEMB is enclosed in a metallic CE box for electromagnetic shielding and mechanical protection
- CE Boxes are mounted to Adapter Boards
- Each FEMB is electrically connected to Adapter Board via two 96-pin three-row connectors
- Each FEMB uses two sets of cables - power cables and signal cables.
- For each CRP there are either three (design option A) or six (design option B) SHV cables that are used to provide the bias voltage to anode planes.
- Mechanical Interface
- Electrical Interface

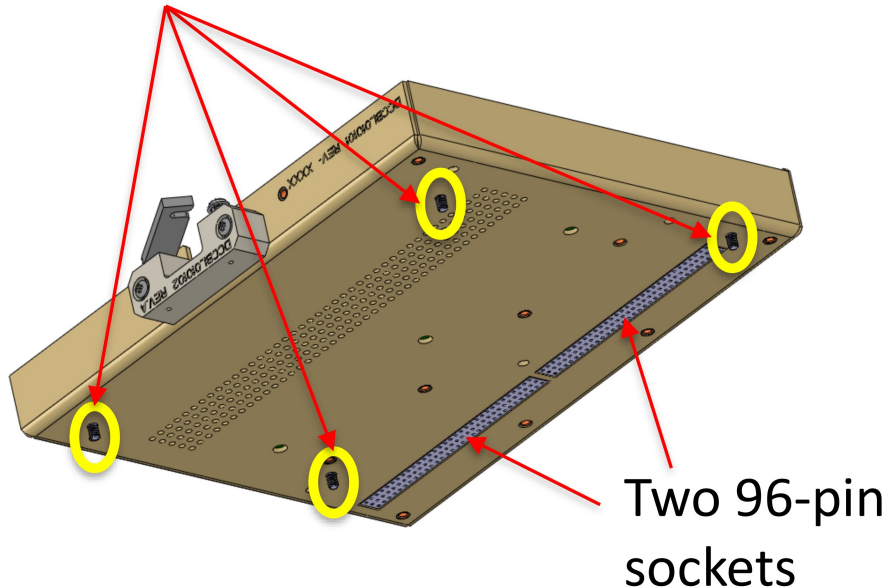
FEMBs, CE Boxes and CRP

CE Box



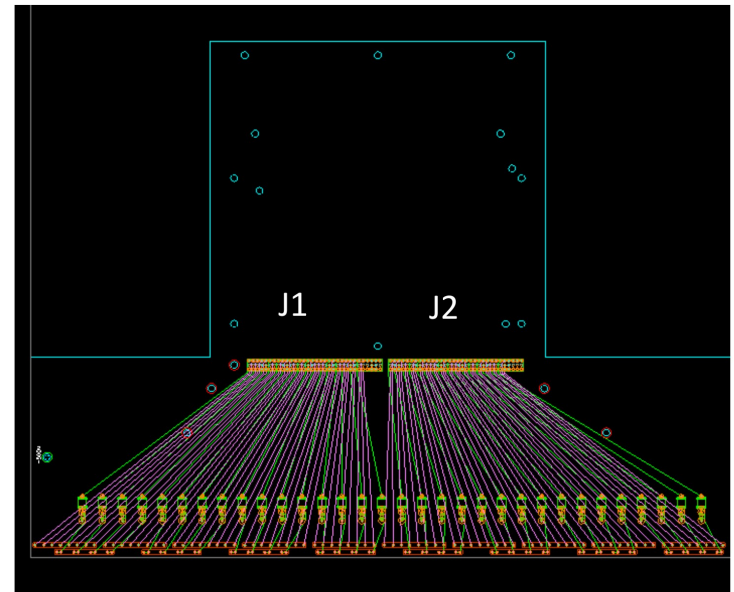
Cable strain relief

M3 screws

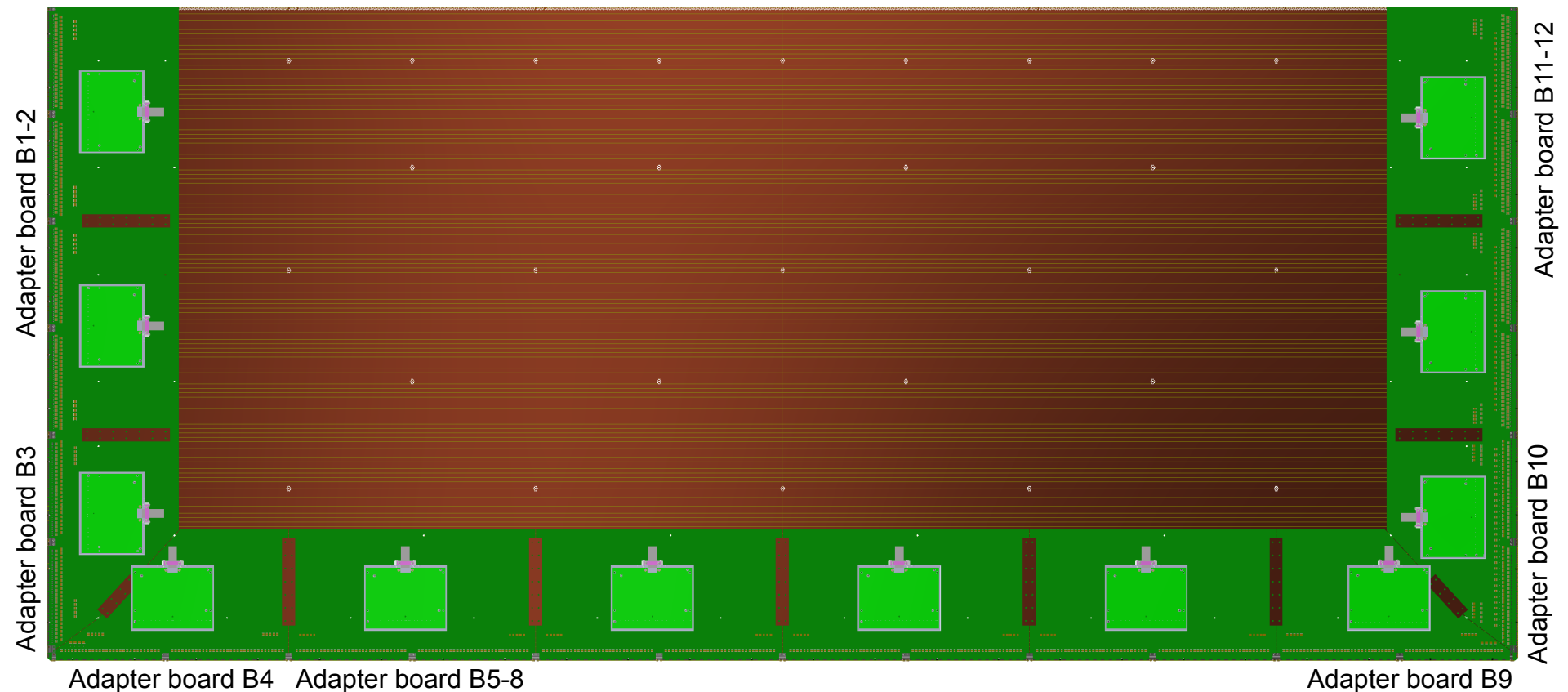


Two 96-pin
sockets

- Each FEMB is enclosed in a metallic CE box for electromagnetic shielding and mechanical protection
- CE Boxes are mounted to Adapter Boards using M3 screws
- Each FEMB is electrically connected to Adapter Board via two 96-pin three-row connectors
- Strip mapping scheme: [DocDB:23684](#)



Adapter Boards

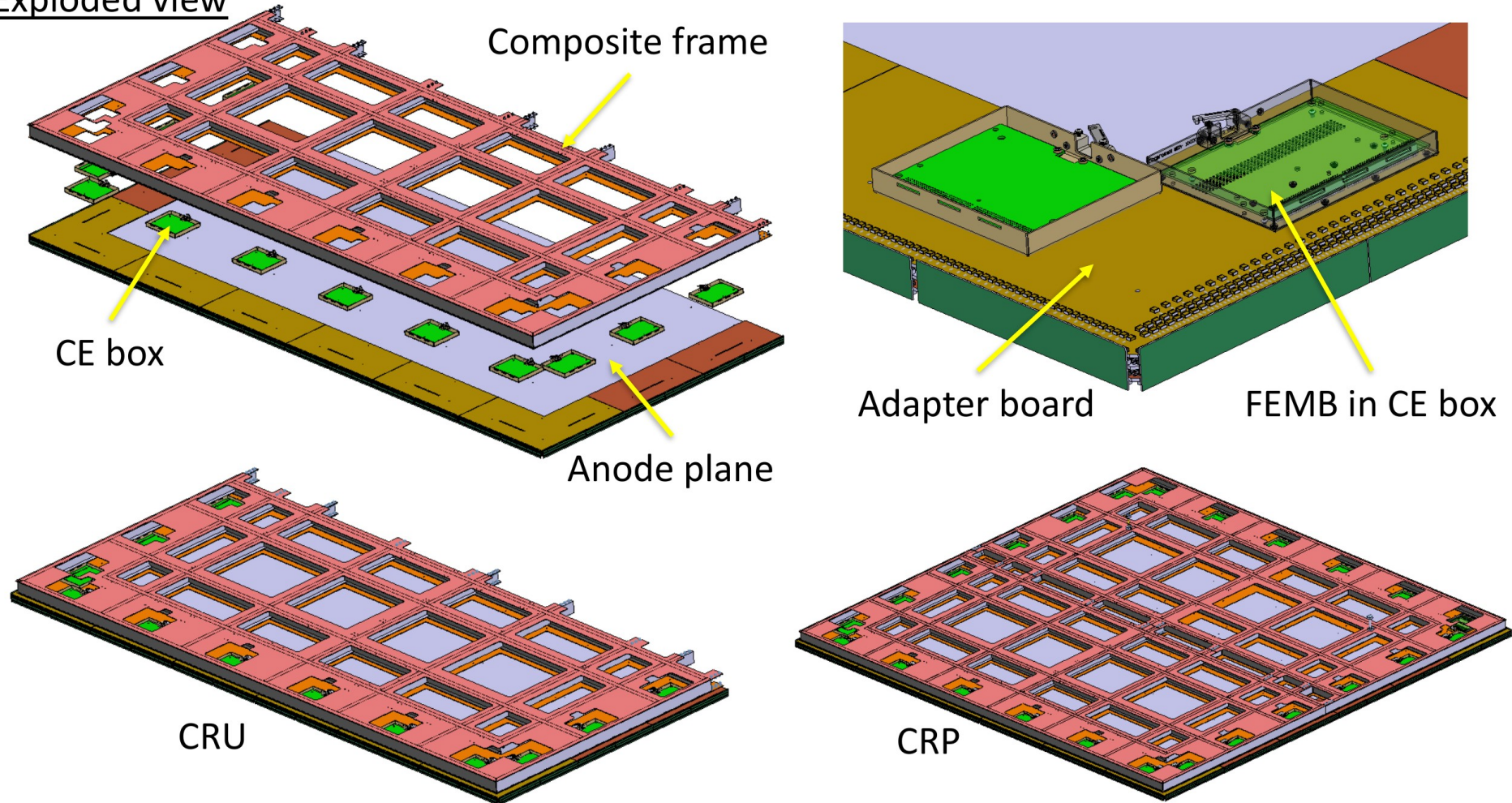


There are 12 adapter boards (shown in green) with 7 unique designs.

CE Box installation

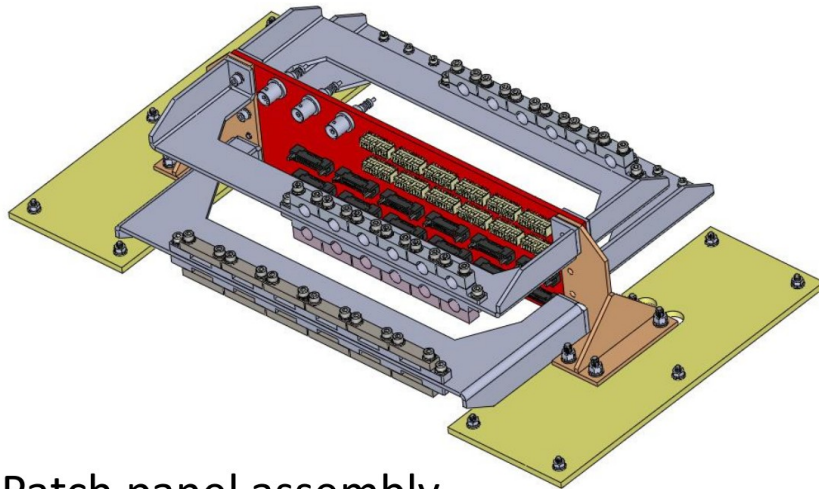
A CRP consists of two CRUs. Each CRU is readout by 12 CE boxes. In total, 24 CE boxes per CRP. The FEMBs are plugged into the CRP adapter boards via two 96-pin sockets.

Exploded view



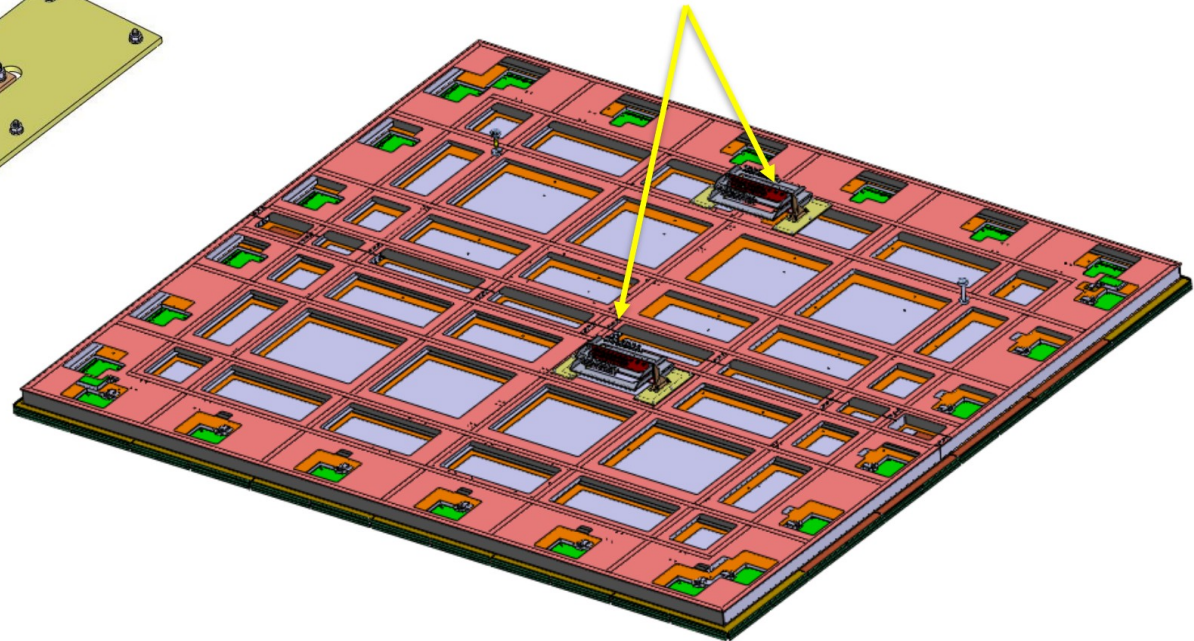
Patch Panels

Patch panels are mounted on the CRP composite frame. A patch panel provides an interface between the CRP cabling and the cryostat cabling. One side of the patch panel accepts Mini-SAS cable connectors from the CE boxes. The other side of the patch panel accepts Samtec cables and connectors from cryostat cabling.



Patch panel assembly

Patch panels installed
on composite frame

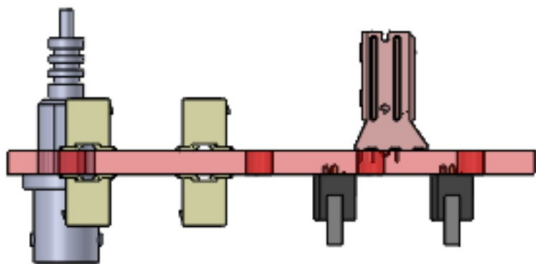
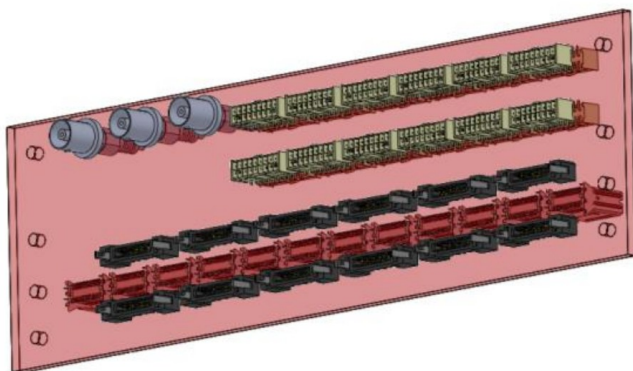


Patch Panels design options

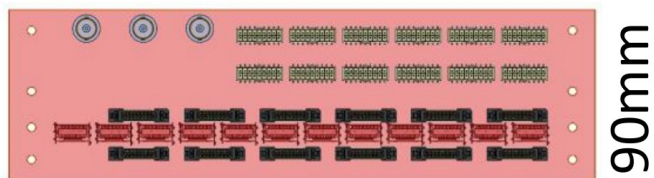
Two patch panel designs are being investigated.

Design A

One patch panel per CRU



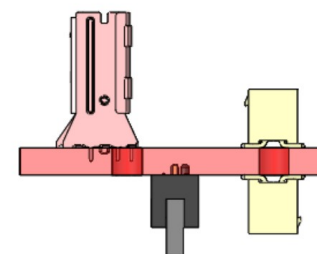
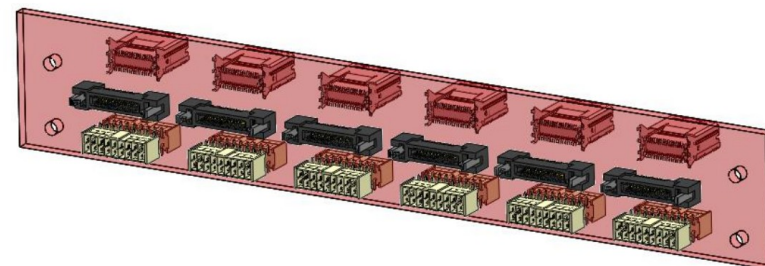
310mm



90mm

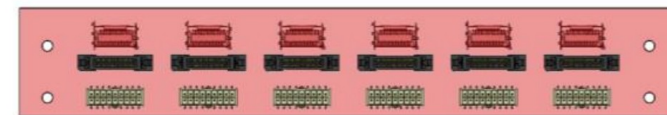
Design B

Two patch panels per CRU



282mm

46mm

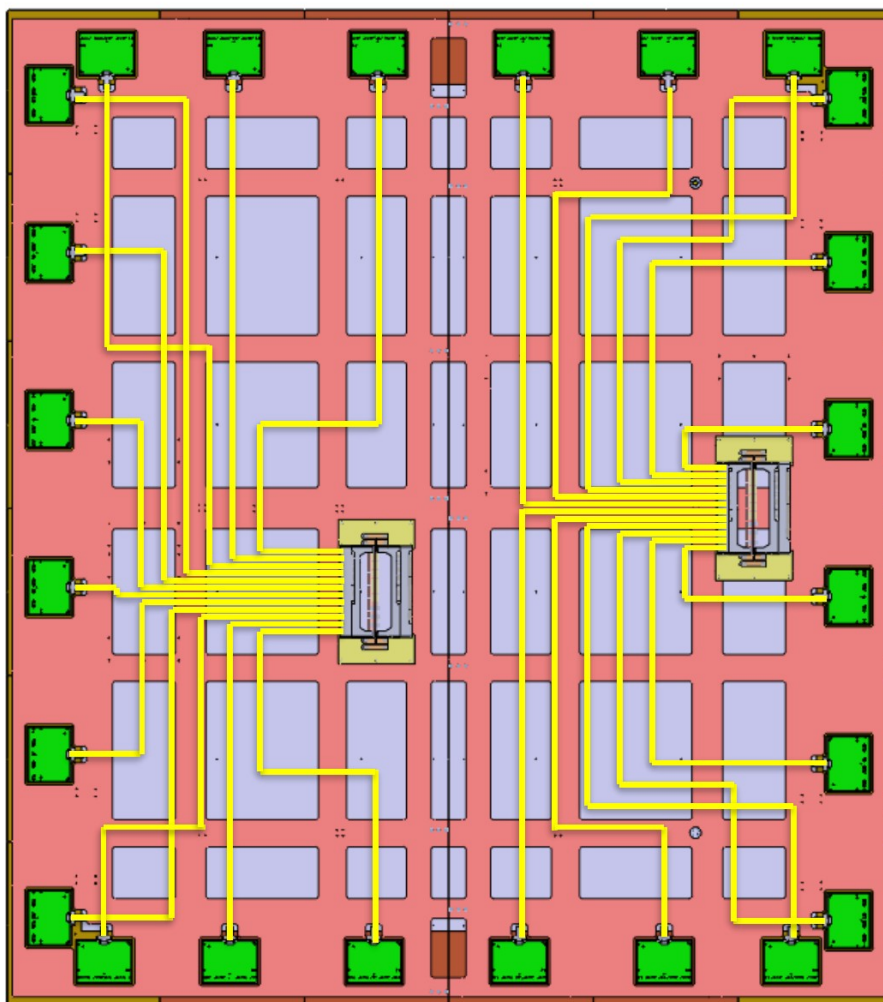
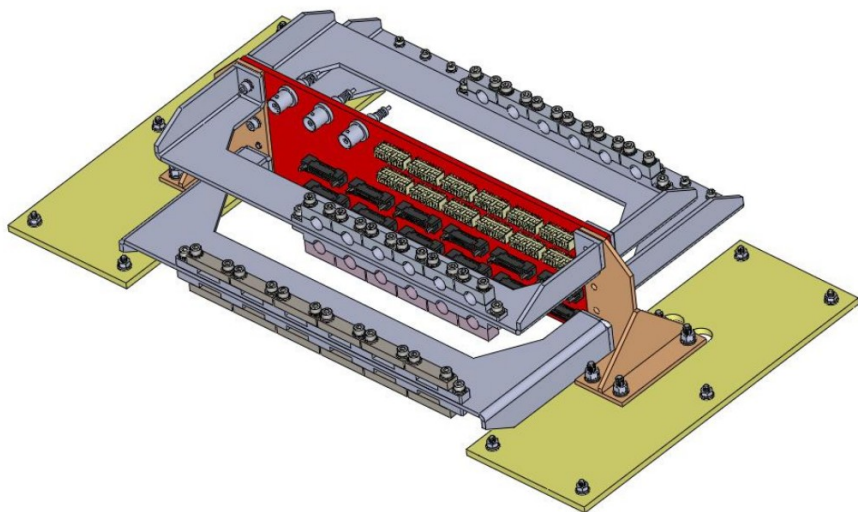


Cable routing on CRP

Patch panel and cable layout*

Design option A

One patch panel per CRU



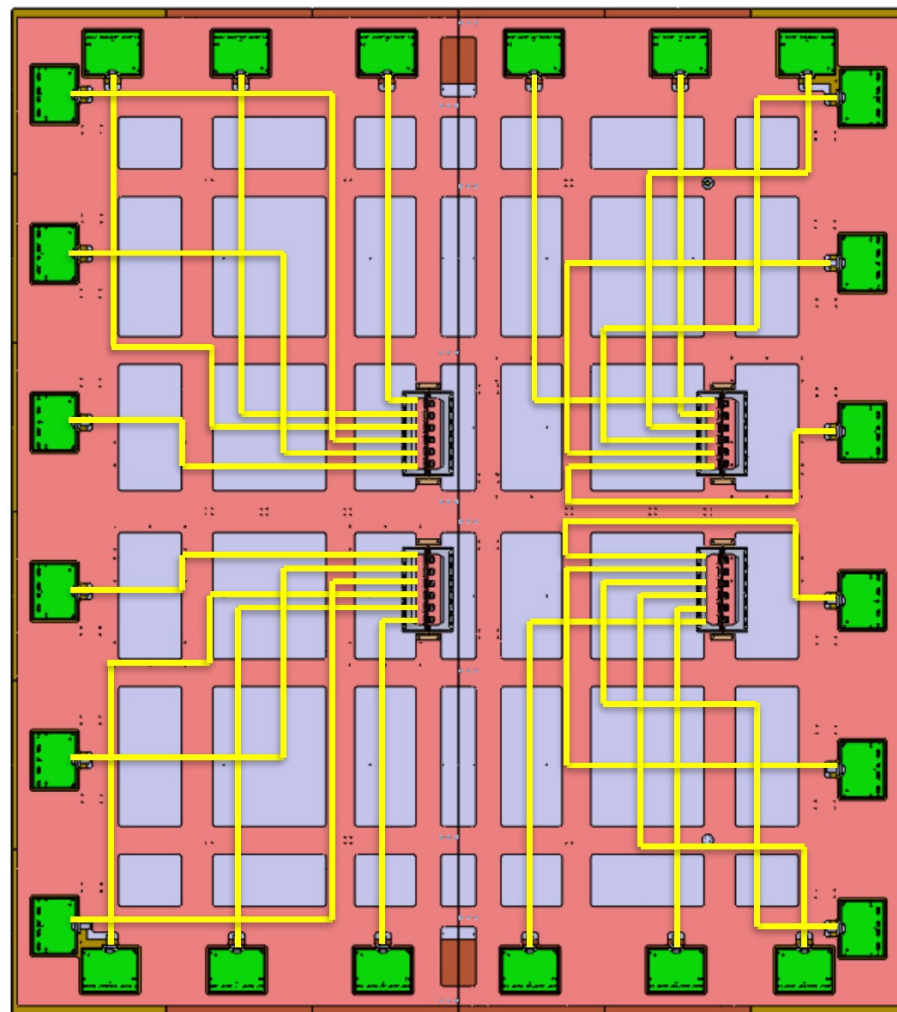
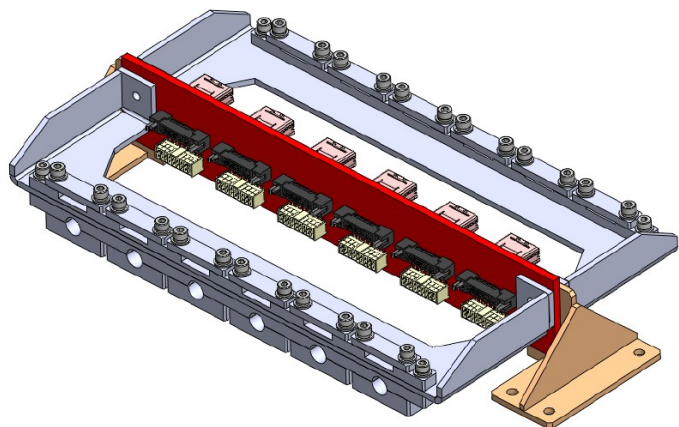
*It doesn't show the actual cable length or exact location. It only schematically shows the connections between CE boxes and patch panels.

Cable routing on CRP

Patch panel and cable layout*

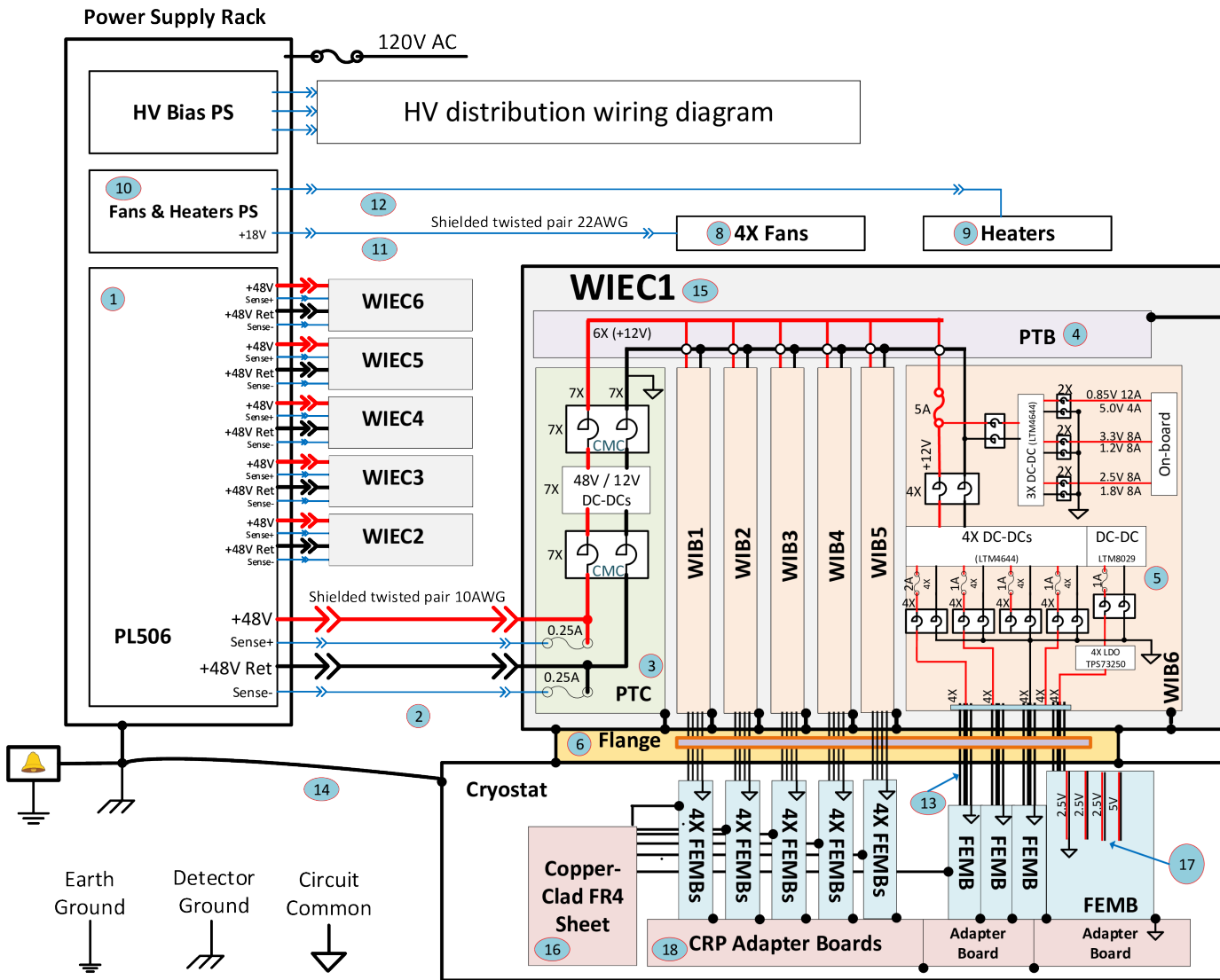
Design option B

Two patch panels per CRU



*It doesn't show the actual cable length or exact location. It only schematically shows the connections between CE boxes and patch panels.

CE grounding scheme



- 1: Weiner PL506 Power Supply
- 2: 48V power cable
- 3: PTC (Power and Timing Card)
0.25A Fuse P/N: 3404.0006.11
Choke P/N: PLT10HH501100PNL
4. PTB (Power and Timing Backplane)
- 5: WIB (Warm Interface Board Version 3.0)
5A Fuse P/N: 3404.0017.11
2A Fuse P/N: 0468002.NR
1A Fuse P/N: 0468001.NR
Choke P/N: PLT5BPH5013R1SNL
- 6: Flange Board
- 7: FEMB (Monolithic Front End Motherboard)
- 8: Fans box
Fans are electrical isolated from WIEC
- 9: Heater
Heater is electrical isolated from WIEC
- 10: Fans & Heater power supply
- 11: Fans power cable (shielded)
- 12: Heater power cable
- 13: 7m cold power cable
- 14: Grounding cable
- 15: Warm Interface Electronics Crate (WIEC)
- 16: Copper sheet underneath the CRP composite frame
- 17: Voltage measured at the FEMB
- 18: Adapter boards for the FEMBs to plug into
Note: Each adapter board takes 1 or 2 FEMBs, but adjacent boards are electrically and mechanically interconnected

Notes

- (1) Fans and heaters are isolated from WIEC
- (2) PTB is mounted with the brass standoffs as a grounding connection
- (3) The grounding connection between WIBs and WIEC is through front panels and side bars
- (4) The grounding connection between PTB and WIEC is through front panels and side bars
- (5) Flange (and flange board) is the place that the FEMB circuit common is referenced to the cryostat (detector ground)

Interface with CRP: responsibilities

- **CRP responsibilities**

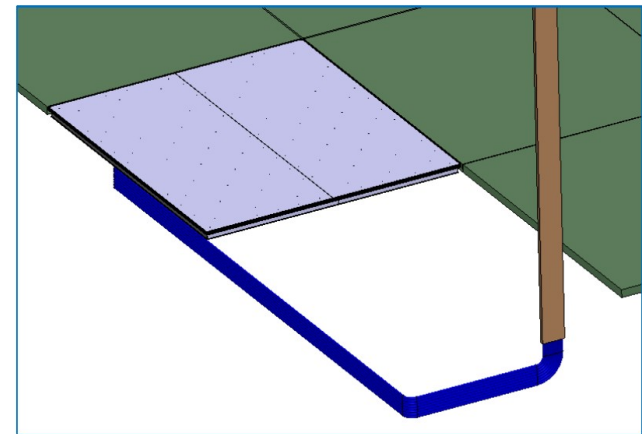
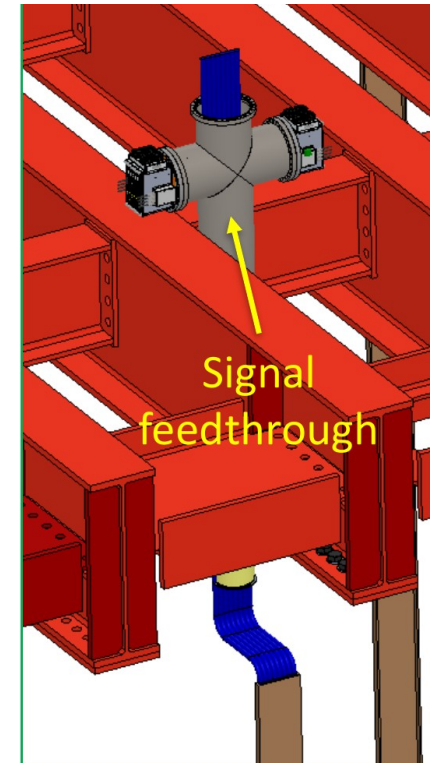
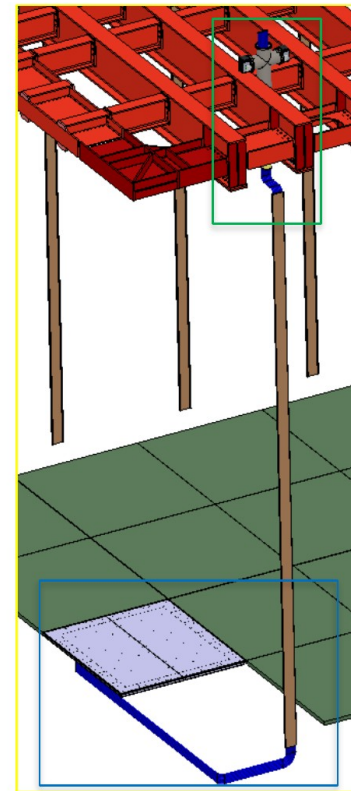
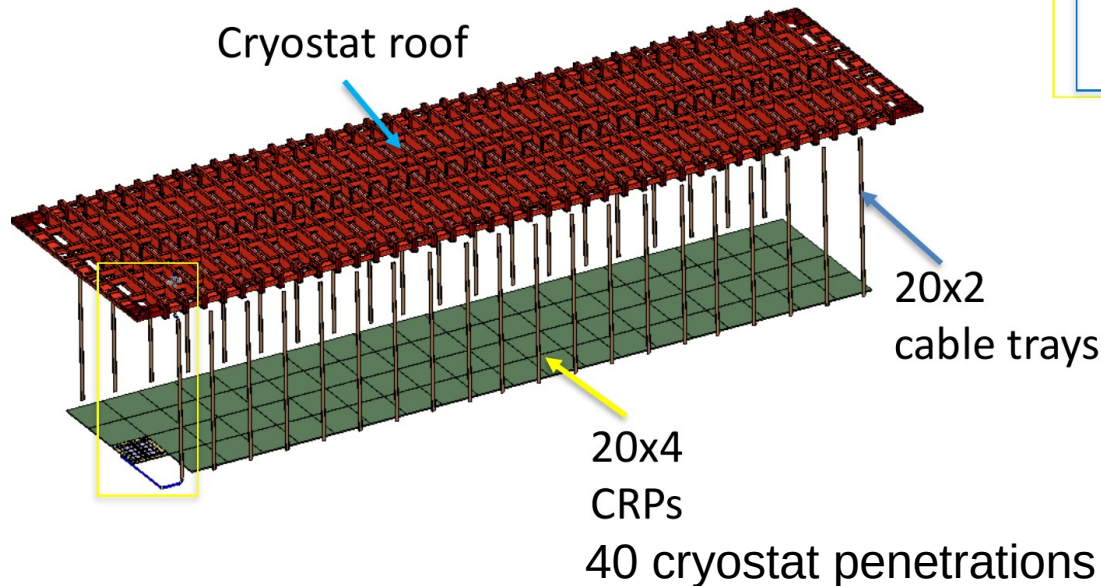
- Design and production of adapter boards
- Design and production of composite frame taking into account the cold-box openings and BDE requirements
- Installing and testing all FEMBs, routing the cables to patch panels at the CRP factories
- Integration of the patch panel into the CRP design

- **BDE responsibilities**

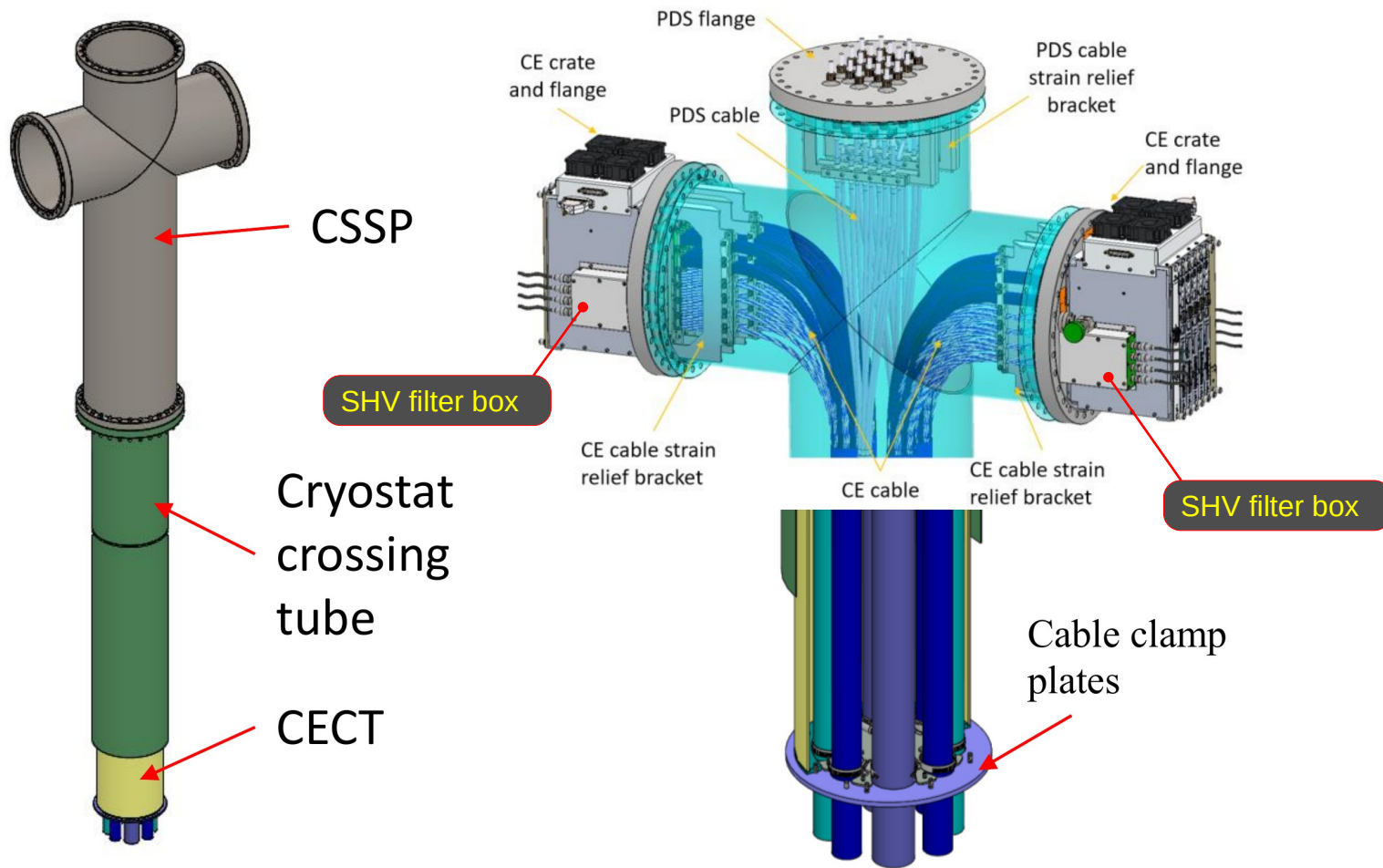
- Provides design details and specifications of the CE boxes as an input to CRP design
- Provides the signal, power cables
- Provides design and production of the patch panel
- Provides test stand for the CRP factories

Cryostat Cabling

SAMTEC CE cables connect CE flanges and CRP patch panels. CE flanges are installed on cryostat signal feedthrough. Inside the cryostat, the cables are tied to the cable trays on the wall and laid down on the cryostat floor prior to the installation of the false floor. The cables are later connected to CRP patch panels after the bottom CRPs are installed.




Signal Feedthrough



Interface with PDS

<https://edms.cern.ch/document/2618994>

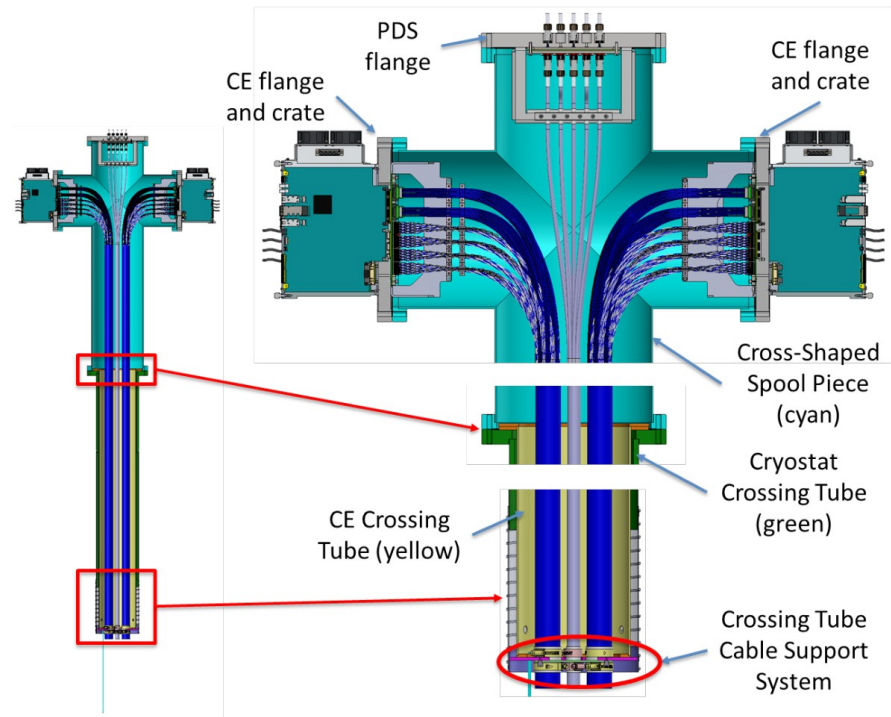
 <p>DUNE Interface Document: Far Detector 2 Bottom Drift Electronics / Photon Detector System</p>			
Document identifier: EDMS id 2618994	Created: 26 October 2021	Page: 1 of 9	
	Modified: 26 October 2021	Rev. No.: 1	

<p>DUNE Interface Document: Far Detector 2 (Vertical Drift) Bottom Drift Electronics and Photon Detector System</p> <p>This document formalizes the interface between the DUNE Vertical Drift Detector Bottom Drift Electronics (BDE) and Photon Detector System (VD-PDS) consortia. It defines the interfaces for both BDE and VD-PDS to complete the design, fabrication and installation of their subsystems. This document describes the elements and the scope of each subsystem at the interface between them.</p> <p style="text-align: center;">https://edms.cern.ch/document/2618994</p>		
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mechanical interface

Share CE crossing tube, cryostat crossing tube, cross-shape spool piece, crossing tube cable support system, cable trays.

electrical interface

There should be no electrical contact between VD-PDS and BDE elements with the exception of sharing the same reference voltage on the cryostat penetration. Both the BDE and the membrane detector are using the same reference voltage, which is the cryostat. Some of the components required to power, control, and read out the two detector systems may be housed in the same racks on top of the cryostat.

Responsibilities

- **BDE**

- cryostat penetrations, except for the VD-PDS flange
- CE flanges, gaskets, hardware(bolts), cable strain relief systems, cable clamps
- mock-up tests at BNL;


- **VD-PDS**

- VD-PDS flange (design, procurement, initial testing)
- Power supplies
- Arrangement of fibers and cables
- Samples for mock-up test at BNL

- **Facility**

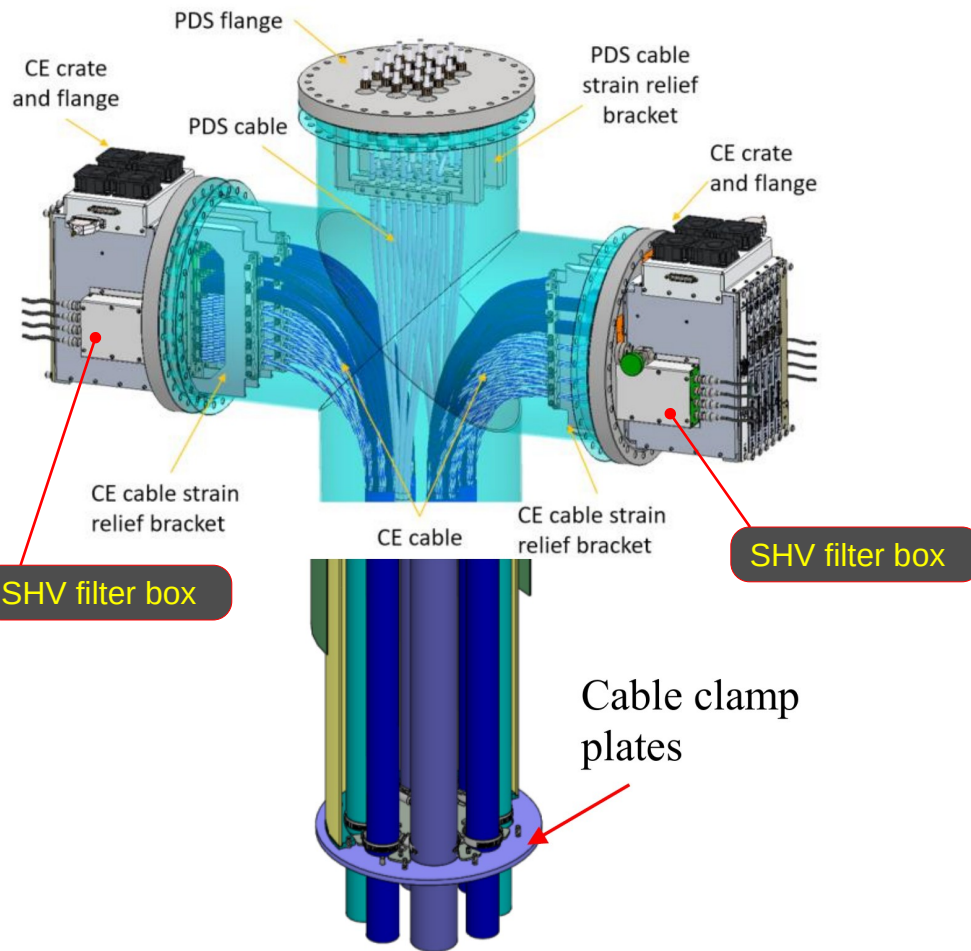
- Design of cable trays on the wall of the cryostat
- installation of fibres and cables in the cable trays

<https://edms.cern.ch/document/2726647/>

	<i>DUNE Interface Document: VD Bottom Drift Electronics / High Voltage System</i>	
	Document identifier: EDMS id 2726647	Created: April 8, 2022
		Rev.

<i>DUNE Interface Document: FD2 Bottom Drift Electronics / High Voltage System</i>		
<p>This document formalizes the interface between the DUNE FD2 Bottom Drift Electronics (BDE) and High Voltage System (HVS) consortia. It defines the interfaces for both BDE and HVS to complete the design, fabrication and installation of their subsystems. This document describes the elements and the scope of each subsystem at the interface between them.</p>		
https://edms.cern.ch/document/2088706		
Prepared by: B. Yu (BNL)	Checked by: CJ. S. Lin (LBNL)	To be approved by: F. Pietropaolo (CERN) T. Shaw (FNAL) B. Yu (BNL) S. Kettell (BNL)
Distribution List		

Interface with HVS



SHV Filter Boxes for bias voltages are installed on CE flanges. Three HV channels with 5 kV SHV connectors to pass up to +/- 1.5 kV voltages and up to 1 mA current to bottom CRPs.

Responsibilities

BDE

Cold SHV cables (procurement, installation)
Filter Boards and their enclosures (design, fabrication, installation).

HVS


Warm SHV cables with 5 kV plugs (procurement).

I&I

Installation and connection of warm SHV cables with assistance from HVS.

Interface with DAQ/SC

<https://edms.cern.ch/document/2088713/>

		<i>DUNE Interface Document: Data Acquisition /FD1 TPC Electronics – FD2 Bottom Drift Electronics</i>	
Document identifier: EDMS id 2088713		Created: May 19th, 2019	Page: 1 of 6
		Modified: March 9th, 2020	Rev. No.: 5

The readout of each FD2-VD Charge Readout Plane (CRU) requires 1 Warm Interface Electronics Crate (WIEC) housing 6 Warm Interface Boards (WIBs).

A total of 80 WIECs will be employed in FD2-VD for the bottom drift electronics.

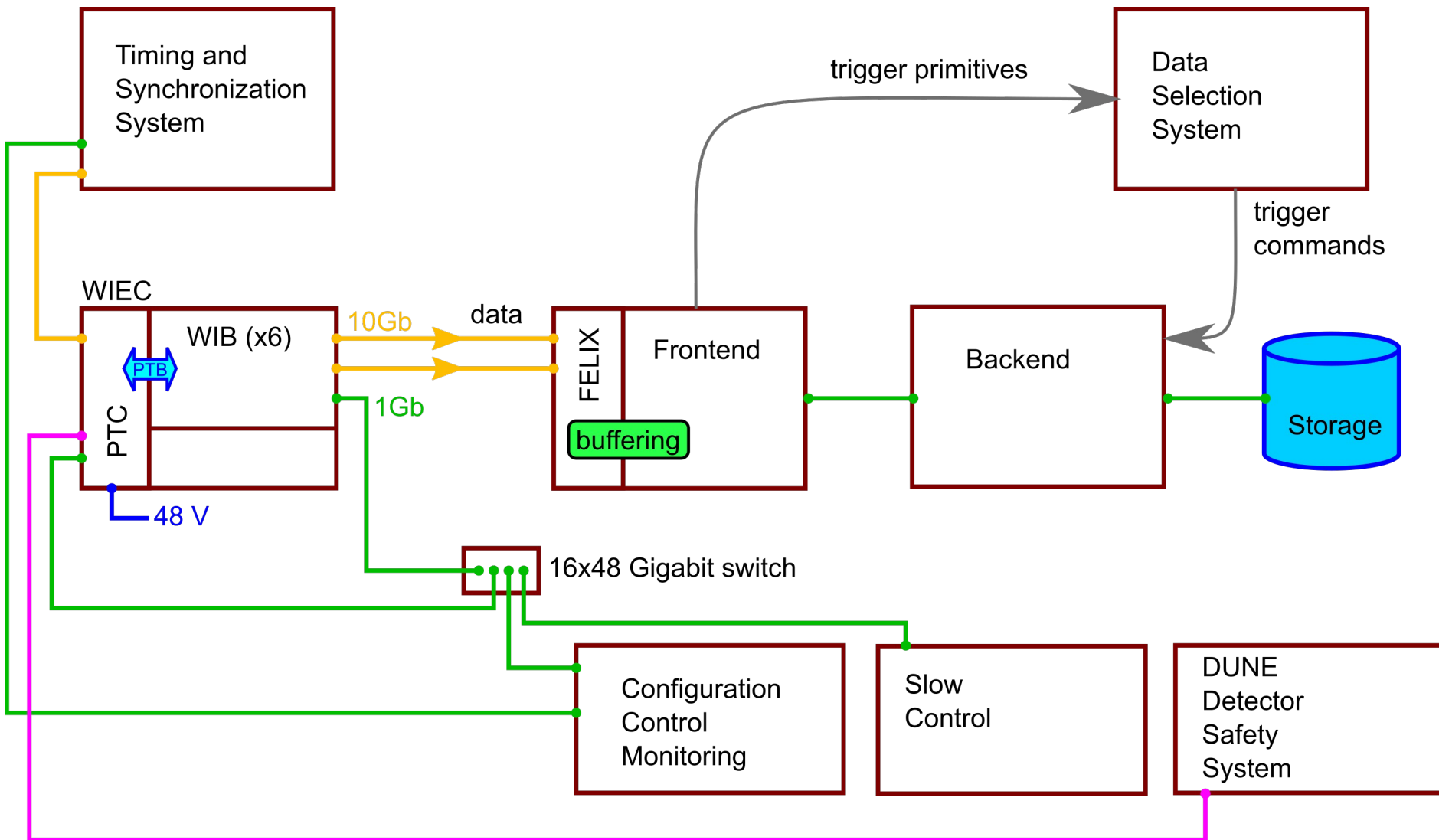
Interfaces:

- Timing
- Data
- Run control, configuration and monitoring
- Power supplies control, configuration, and monitoring
- Physical interfaces; software interfaces; data formats and protocols

Interfaces are same as in Cold Electronics for FD1-HD, which completed the preliminary design review. FD2-VD BDE has no new interfaces with DAQ/SC.

<i>DUNE Interface Document: Data Acquisition - FD1-HD TPC Electronics / FD2-VD TPC Bottom Electronics</i>		
<p>This document formalizes the interface between the DUNE Data Acquisition (DAQ) and FD1-HD TPC Electronics (TPC)/FD2-VD Bottom Drift Electronics (BDE) consortium. It defines the interfaces for both DAQ and TPC/BDE to complete the design, fabrication, and installation of their subsystems. This document describes the elements and the scope of each subsystem at the interface between them.</p> <p style="text-align: center;">https://edms.cern.ch/document/2088713/1</p>		
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CE power and communication interfaces



Responsibilities

BDE



- design, prototyping, construction, and installation of the electronics that is used for the readout of the waveforms on the strips of the CRPs.

DAQ

- Collecting the data from all the CRPs, selecting the interesting events, and assembling them for transmission to permanent storage on disk or tape.
- Distribution of the timing signals to all the DUNE detector components, as well as for the control, configuration, and monitoring of all the active readout components (through the CCM sub-system).

<https://edms.cern.ch/document/2694691>

We are actively working with I&I to define the interfaces and the installation plan.

 		https://edms.cern.ch/document/2694691	
Long Baseline Neutrino Facility, DUNE & CERN			
DocumentEDMS identifier:	Fermilab LBNF DocDB:	Created: March 24, 2022	Page 1 of 14
EDMS ID: 2694691 ▶		Last Modified: April 18 2022	Rev. No.: 1
<p>Interface Control Document Installation / TPC Electronics Consortium (FD2 Bottom Drift Electronics)</p> <p>Abstract</p> <p><i>This document defines the interfaces between installation and integration (I&I) and the TPC_Electronics Consortium for work related to FD2 Bottom Drift Electronics installation. It defines the interfaces for both TPC and I&I to complete the design, fabrication and installation of their subsystems. This document describes the elements and the scope of each subsystem at the interface between them.</i></p>			
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Distribution List			
D. Christian (FNAL), M. Verzocchi (FNAL), B. Miller, J. Fowler, J. Freitag, J. Mader, T. Shaw			

Risks of design changes

System	Risk	Risk level	Impact level	Mitigation
PDS	Increase in cable/fiber number or change in size (diameter) or routing scheme.	high	medium	Design the cable clamp plate, penetration port, and cable trays with sufficient space to accommodate additional cables and PDS strain relief system based on the most conservative estimate of PDS cable and fiber needs .
HVS	Increase in the number of cables	low	low	Reserve sufficient space to accommodate extra HV feedthroughs on the CE flange.
CRP	Increase in the number of strips	low	high	Modular and extendable design concept of CE.
DAQ	Change in DAQ front end link hardware (e.g. switching from FELIX-bases to commercial off-the-shelf data receiver).	high	medium	Use FPGA-based design of WIBs for flexibility. Changes in downstream protocol requirements can be easily accommodated with minor firmware modifications.
DAQ/SC	Change in communication or data exchange protocols with SC, CCM, etc.	high	medium	Use Xilinx Zynq Ultrascale+ FPGA in WIB for flexibility. Move SC functionality from firmware to software stack in the WIB.