ProtoDUNE Lessons Learned

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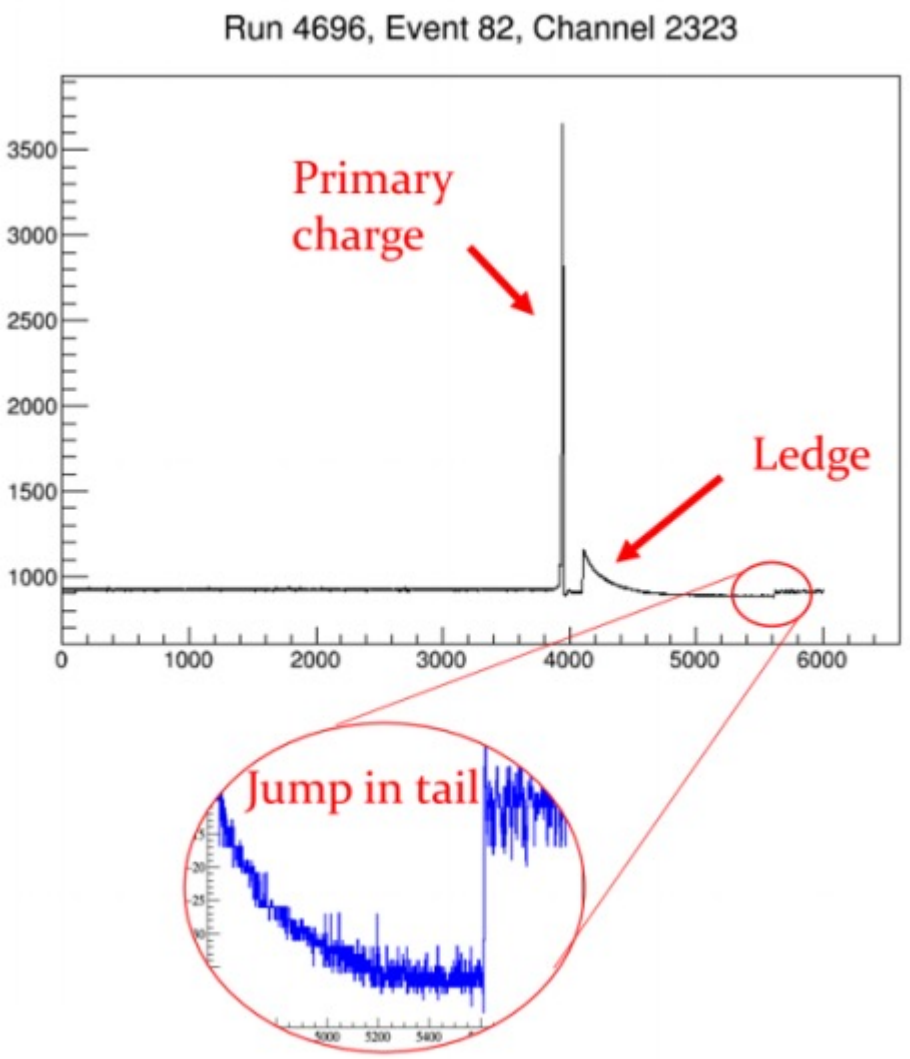
I will cover lessons learned relevant to BDE

- Many of the lessons learned from ProtoDUNE-SP are related to working at height on the APAs or in the cryostat and to mechanical connections to the APA and are not relevant for the bottom drift electronics for FD2.
- I will cover:
  1. “Ledge effect”
  2. LArASIC internal DAC for test charge injection
  3. ASIC problems not apparent at room temperature
  4. Sockets used in ASIC testing
  5. Cryogenic test stand development
  6. WIB firmware

1 of 6: Ledge Effect

- **Problem**: Analysis of ProtoDUNE-SP data revealed a problem with the FE amplifier (LArASIC). The problem occurs when a large amount of change (>50 fC) is collected over a period of 10-50 µs. In this case, the feedback mechanism of the FE amplifier stops working for several hundred µs. In this time period, the amplifier does not function and signals following the large charge deposition are lost. A ledge is observed in the output of the FE amplifier, followed by a slow decay and a sudden turn-on of the amplifier.

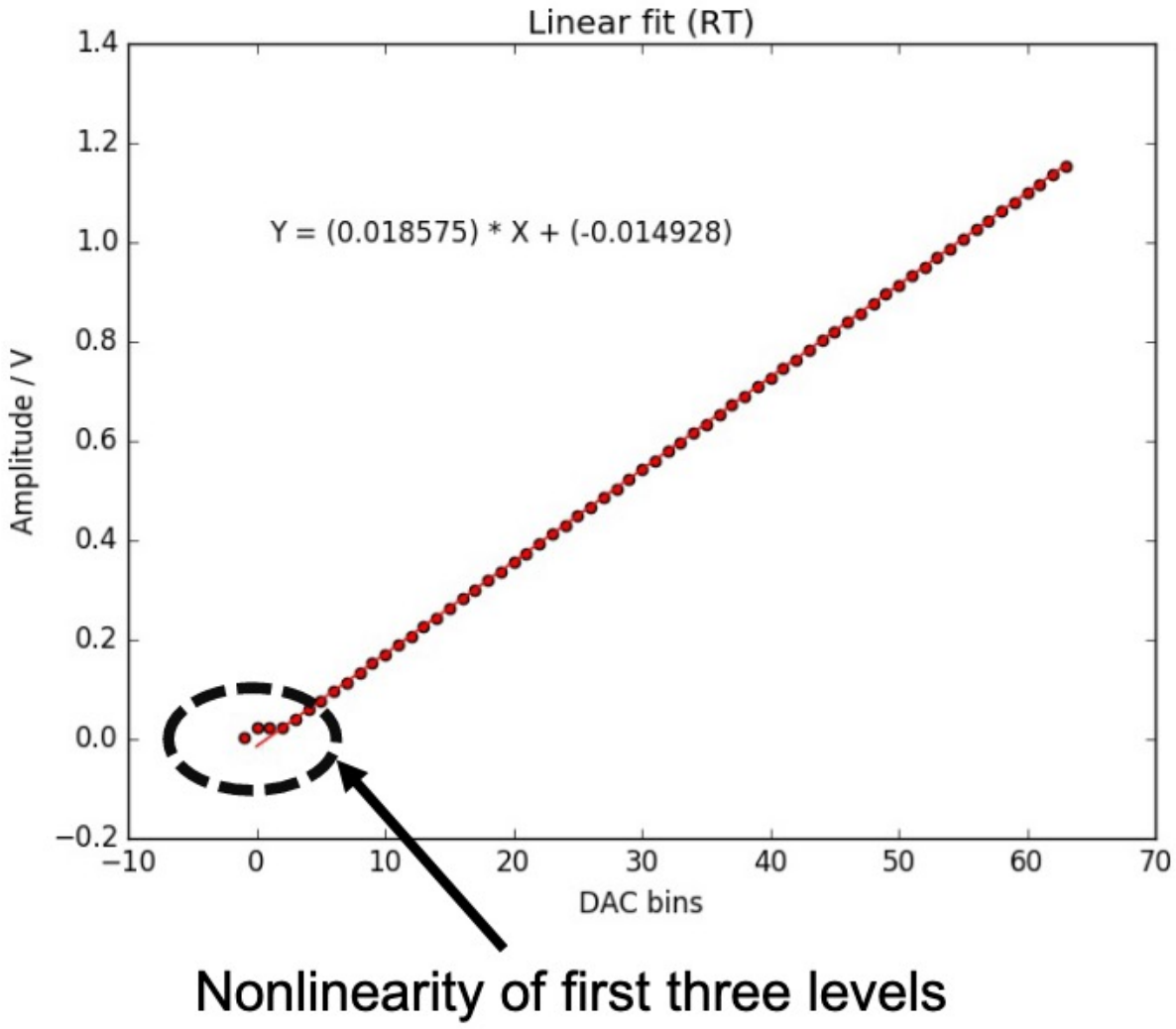


Resolution

- The problem was reproduced in the laboratory both at LN2 temperature and at room temperature. It was traced to a network designed to improve the return-to-baseline performance of LArASIC relative to the version used for MicroBooNE. The parasitic gate capacitance of large transistors used in that “adaptive continuous reset” network reduced the loop stability of LArASIC and resulted in the ledge effect. This problem was eliminated for LArASIC_P4.

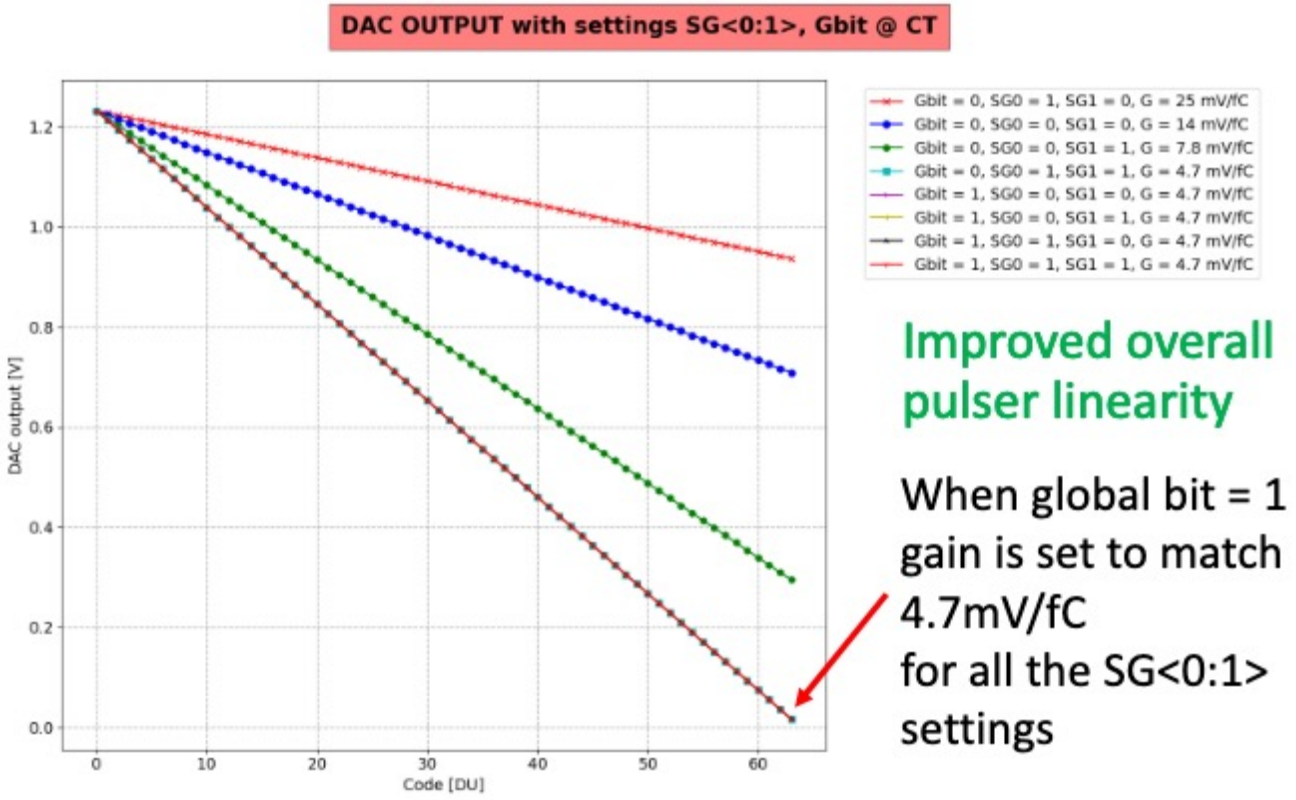
2 of 6: LArASIC DAC

- The ProtoDUNE version of LArASIC included an internal DAC to facilitate gain calibration. Unfortunately, the linearity of this DAC for small values was poor. This limited the usefulness of the DAC.



Resolution

- The original LArASIC DAC was non-linear near zero because it was referred to ground and was improperly biased. A new DAC has been designed that is referred to the positive voltage rail (1.8V). The new DAC also has 4 gain ranges (matched to the dynamic range of the 4 LArASIC channel gain settings). The latest FEMB also has a 2-bit DAC controlled by COLDATA that can be used to check the individual LArASIC internal DACs, and the latest WIB includes a high precision 16-bit DAC that can be used to pulse LArASIC test inputs. One of our goals for ProtoDUNE-II is to explore which of these options is most useful.



3 of 6: ASIC problems not apparent at room temperature

- **Problem:** During the cold testing of the ProtoDUNE front-end motherboards (FEMBs) it was found that approximately 4% of the FE ASIC were not functioning. This required reworking the FEMBs. The losses for the ADC ASICs, that were all tested in cold prior to the installation on the FEMBs, were negligible. The non-functioning FE ASICs on these boards were replaced and the boards were retested.

Resolution:

- Each FEMB includes 8 LArASICs, 8 ColdADCs, and 2 COLDATA chips.
- If the chip failure rate were 4%, more than ½ of the FEMBs would require rework ($.96^{18} = .48$).
- A rework target of 1% of FEMB implies that we need to test all chips cold as well as warm unless we can establish that the failure rate for chips that pass warm QC is lower than 0.05% ($.9995^{18} = .99$).
- Our plan is to test all ASICs in LN2 as well as at room temperature prior to FEMB assembly.
- We are developing a robotic cryogenic testing station which will be used for both warm and cold tests.
  - The cause of the LArASIC problem was that the bandgap reference circuit failed to start up when cold in ~4% of chips. The design shortcoming was understood and fixed. To date, 0 of 280 LArASIC5B chips failed LN2 tests after passing room temperature tests.

4 of 6: Sockets Used in ASIC Testing

- **Problem:** The sockets housing the chips being tested (either LArASIC or the ADC) for ProtoDUNE had to be changed rather frequently when immersing the test boards in LAr. In many cases the failures in the chip testing have been found to be caused by the sockets being used rather than the chips being tested. In part the problem was related to the type of socket being used (the clamping “clamshell” type had more problems compared to the sockets that push down on the pins of the chips using a spring system). The problem was probably exacerbated by the condensation that would form when extracting the test boards from the LN_2 while open dewars were being used. The number and frequency of failures of sockets was reduced when using the Cryogenic Test Stand to avoid condensation during the extraction from LN_2.

Resolution

- All sockets will be spring-type. All sockets will be mounted on daughter cards so that no board re-work is required to replace a socket. Boards and supports will be designed to control flexing during chip insertion and removal. Most of these features have been included in the test boards being used now.
- A “Cryogenic Test Stand” will be used to eliminate the condensation that occurs when an open LN2 dewar is used.

5 of 6: Cryogenic Test Stand Development

- Problem: The Cryogenic Test System (CTS) developed at Michigan State University failed to pass the initial safety inspections performed at BNL when the first CTS was delivered, and so was not used in most of the ASIC QC testing before ProtoDUNE-SP. Significant modifications to the CTS were required before it could pass the BNL safety inspections. The same thing happened when the CTS was delivered to Fermilab, despite the fact that the unit delivered at Fermilab already included the design changes requested by BNL. Units delivered to SLAC and LBNL that included all design changes required by BNL and FNAL passed the safety inspections without further problems.

Resolution

- External safety reviews will be included in all future cryogenic test system design.
- CTS units are in use now at BNL, LSU, UC Irvine, LBL, and FNAL and will be used in FEMB testing for DUNE.
- The design of the new robotic CTS for ASIC testing is nearly mature. We included external reviews with Fermilab experts early in the design of this system (two sessions so far). We will have another external review before construction begins.
- The design incorporates lessons learned about sockets.

6 of 6: WIB Firmware

- **Problem:** The WIB firmware developed at Boston University for use in ProtoDUNE required the use of the full ProtoDUNE data acquisition system and thus was not easy to use to verify the performance of single FEMBs. It also did not include easy provision for debugging. As a result, a stand-alone firmware developed at BNL was used for all FEMB check-out and all debugging. Consortium members trained to use one version of the firmware had difficulties with the other.

Resolution

- Since ProtoDUNE-SP the WIB has been redesigned to use a less expensive SoC FPGA (a Xilinx Zync, running Petalinux). The firmware and software for the new WIB have been developed by a team led by Alex Madorsky (U. Florida) in close consultation with the WIB designer (Jack Fried, BNL). The new firmware supports the full DUNE DAQ, but also supports simple test stands using Gbit Ethernet.