LArASIC and ColdADC Lifetime Studies

Jianming Bian
University of California, Irvine

FD2 BDE Preliminary Design Review
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UCIrvine

DUNE

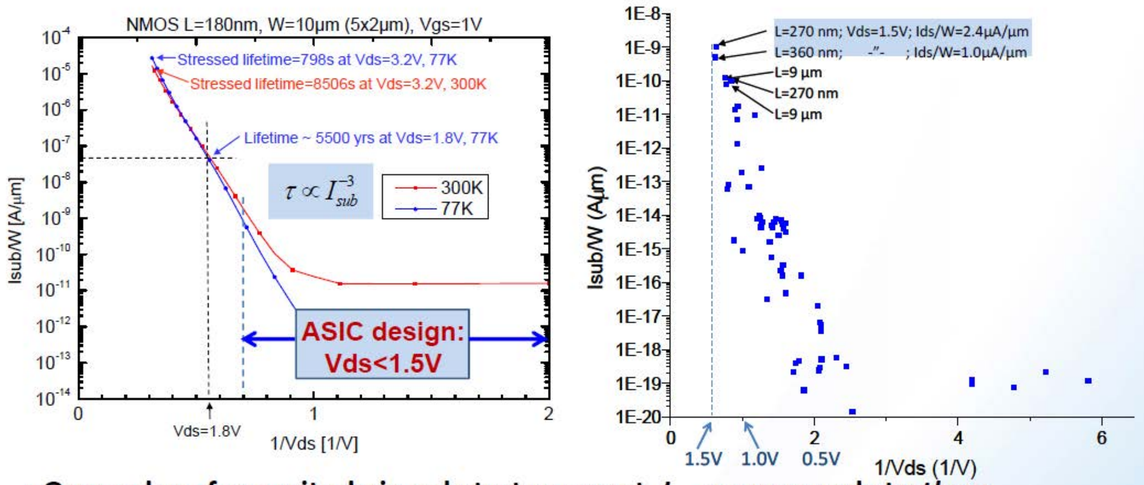
Content

- LArASIC lifetime study
- ColdADC lifetime study

LArASIC Lifetime study

- The remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to channel hot carrier effects (HCE)
- **LArASIC is designed for long lifetime at cryogenic temperatures**
  - Low voltage and current in each transistor

Measurement Type II: Substrate Current Density I_{sub}/W vs $1/V_{ds}$



- One order of magnitude in substrate current I_{sub} corresponds to *three orders* of magnitude in lifetime. At 77 K, V_{ds} = 1.8 V projects a lifetime of ~5500 years.
- I_{sub}/W and $1/V_{ds}$ distribution for all transistors in the analog front-end ASIC for LAr TPC (TSMC 180nm, 1.8V node) shows that all transistors are well below nominal voltage of 1.8V and at low I_{sub}; *Reduced* V_{ds} < 1.5 V results in essentially making HCE negligible and a very long extrapolated life time.

Brookhaven Science Associates

BROOKHAVEN NATIONAL LABORATORY

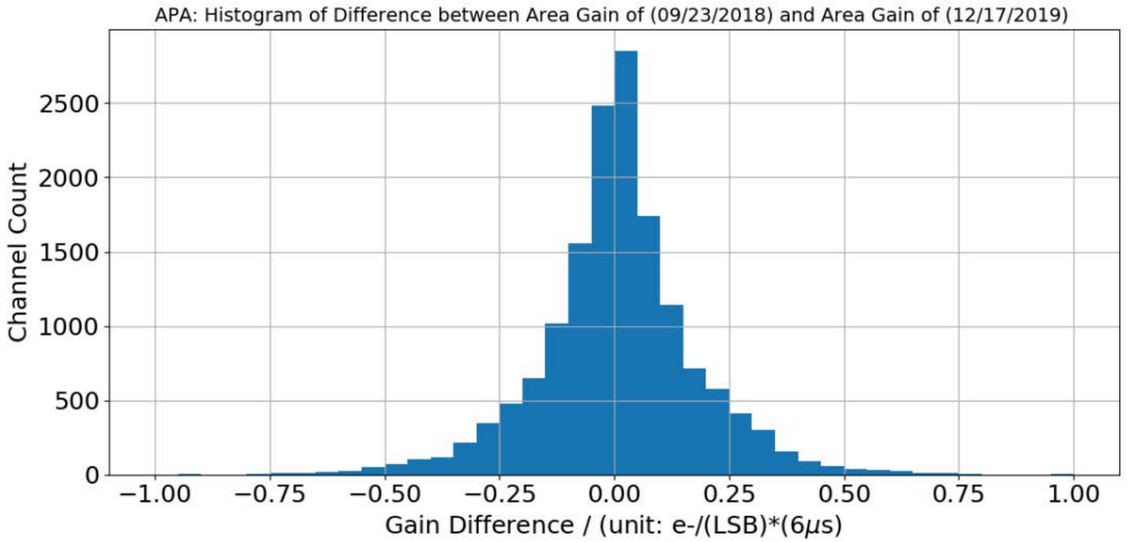
To alleviate the lifetime risk, **custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years**

Any transistor falling in the region V_{ds} <1.5 V and I_{sub}/W < 10^{-9} A/m should have a very long lifetime

S. Li, et al, "LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling," IEEE Transactions on Nuclear Science, Volume: 60, Issue: 6, Part: 2, Pages: 4737-4743 (2013)

LArASIC Lifetime study

- LArASIC in MicroBooNE: **No observable change after seven years**
- ProtoDUNE-I (SP): No measurement degradation is observed over a year
  - The measured gain shift is around 0.13% and 0.4%RMS, with an excellent agreement between 2018 and 2019 (around 0.01% shift with 0.3% RMS)
- The lifetime study of LArASIC will take place in two different phases, the exploratory phase and the validation phase. Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is the preparation phase. The most time and effort will focus on the exploratory phase, we will gain (or lose) confidence based on the test results in this phase. Validation phase will be useful to validate what we would learn in the exploratory phase, and collect more information to prepare for future review(s)
  - **A P5 LArASIC was stressed at 3.0V over 300 hours in liquid nitrogen, no significant change in current drawn is observed.**
  - The recommended voltage for CM018/G is 1.8 V + 10%, which limits the stress voltage
    - commercial chips designed in TSMC 180 nm, e.g., AD9265 and AD9650, the absolute maximum rating is 2.0 V which is consistent with 1.8V + 10%
  - Test setup will be optimized with the dual-dut test board to observe more performance parameters
  - More tests will be carried out after the busy ProtoDUNE-II production

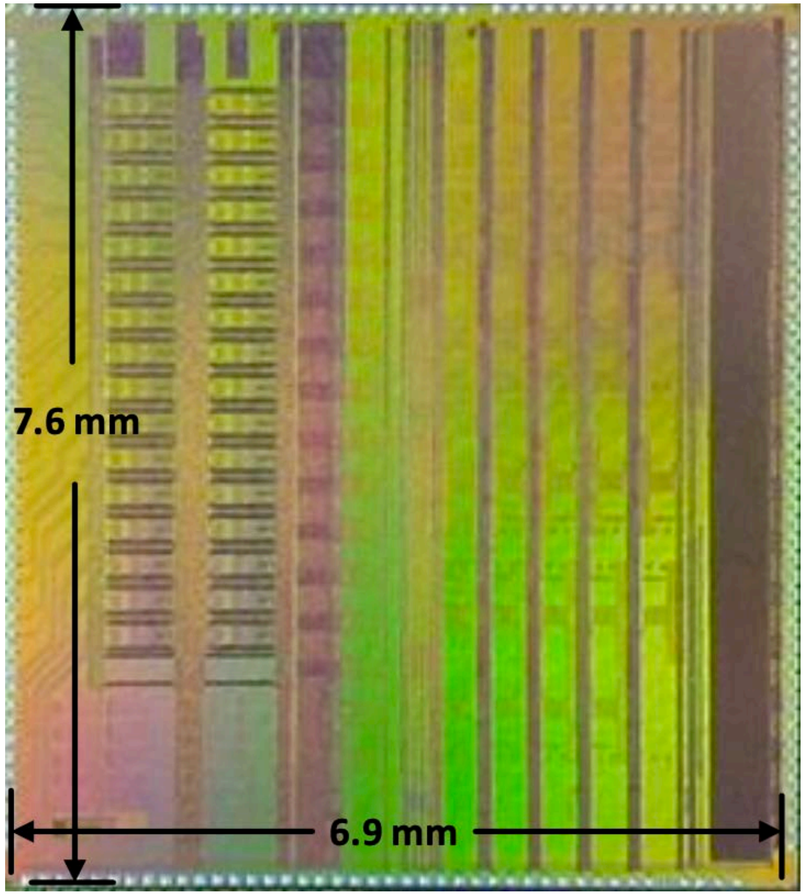


ProtoDUNE-SP: Good reliability over a year operation

Introduction to ColdADC

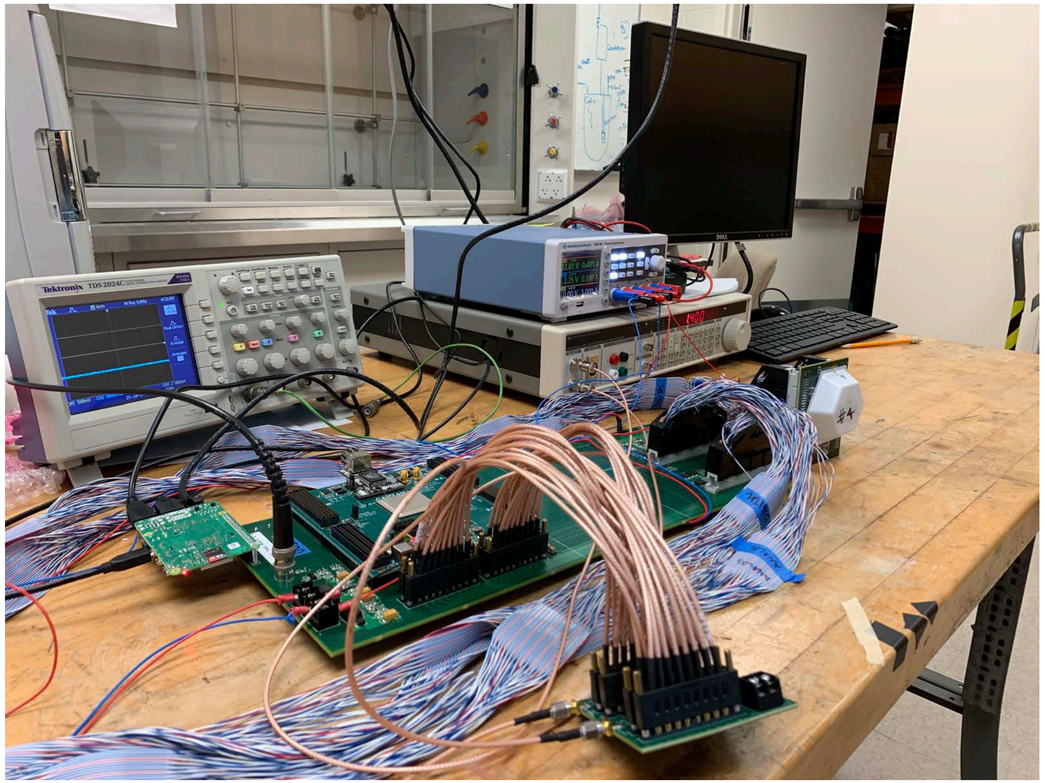
- ColdADC_P2 is a 16-channel, 12-bit, 2 MS/s digitizer
  - It's redesigned to correct several design errors, to improve performance and to add new features based on the first prototype of the ASIC (CodeADC_P1)
- It will be used inside the DUNE Far Detector, and intended for operation without replacement
  - Required to have long-term reliability in cryogenic environments
  - Also required to have low noise, good linearity and low crosstalk

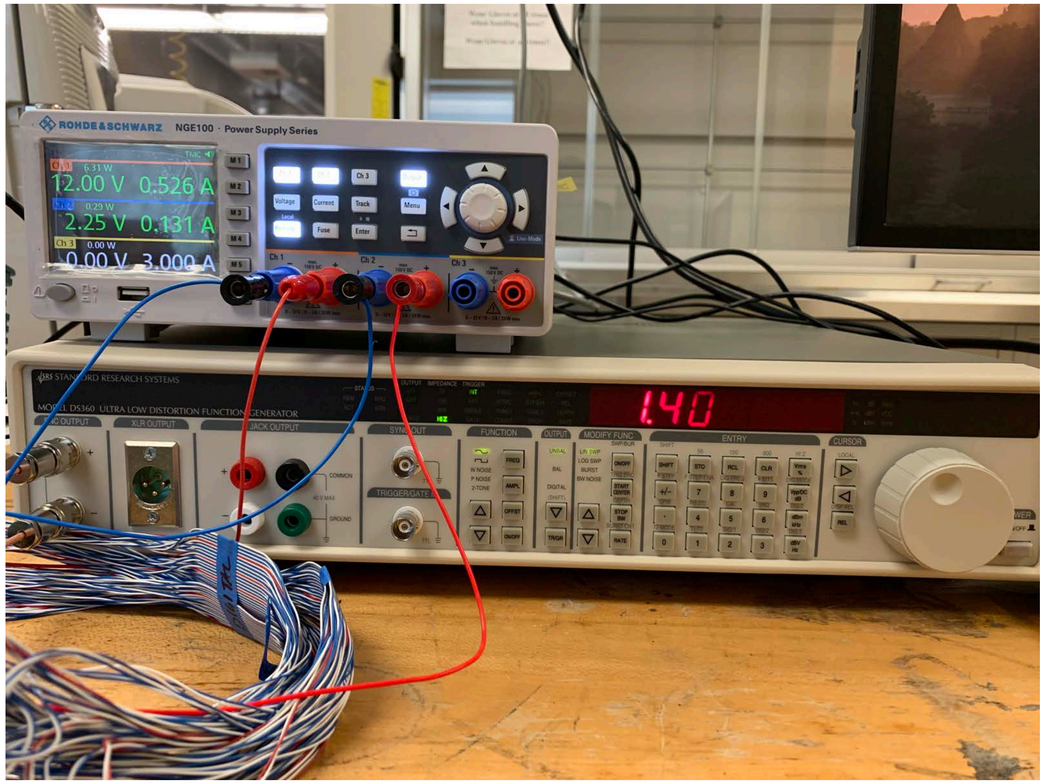
A bare die photograph



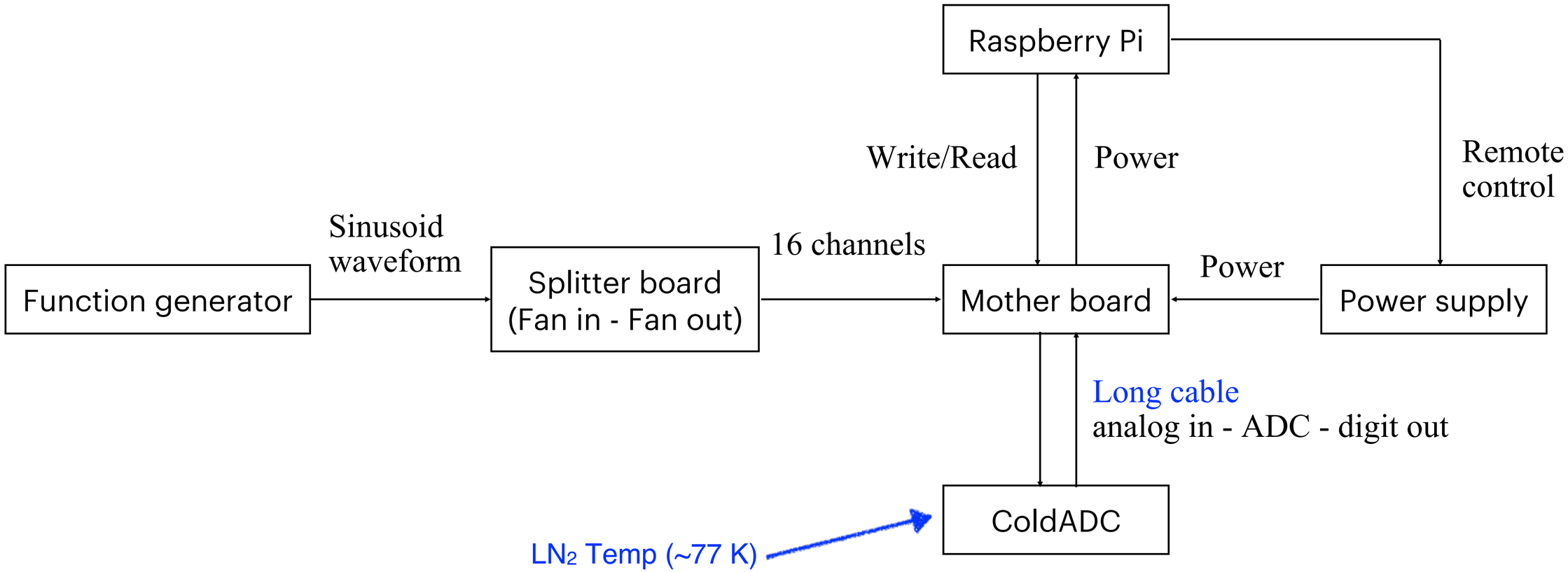
Preparation for the lifetime study

- Setup the ColdADC test stand
  - Power supply (Rohde&Schwarz NGE 100), SRS DS360 Ultra-Low Distortion Function Generator
  - With USB interface, the setup can be remotely operated



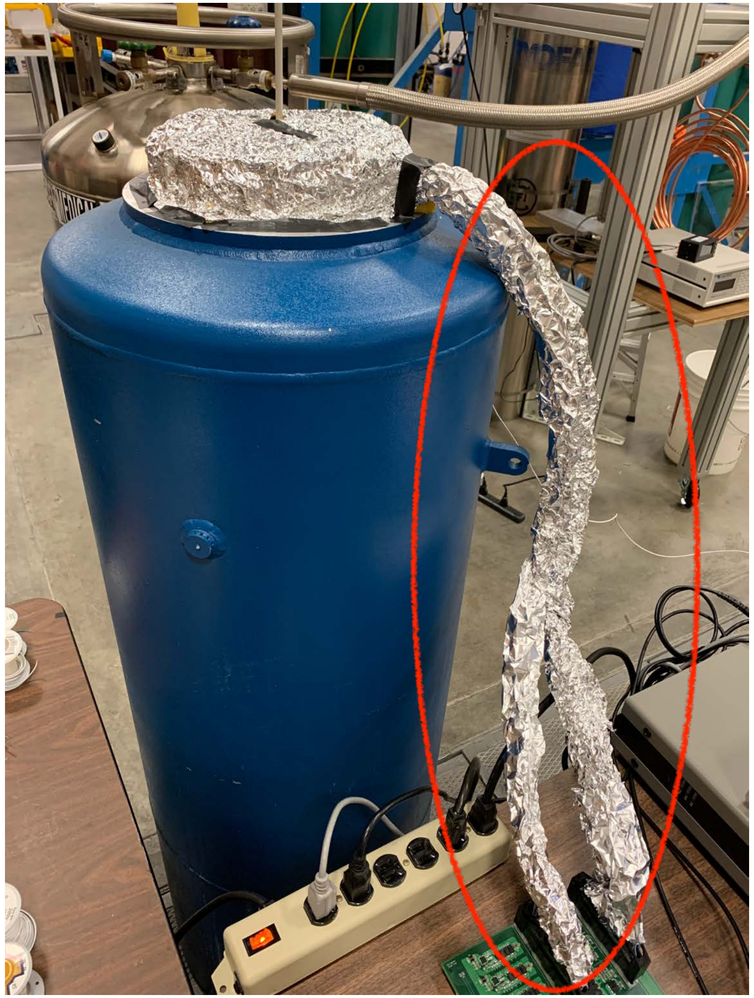


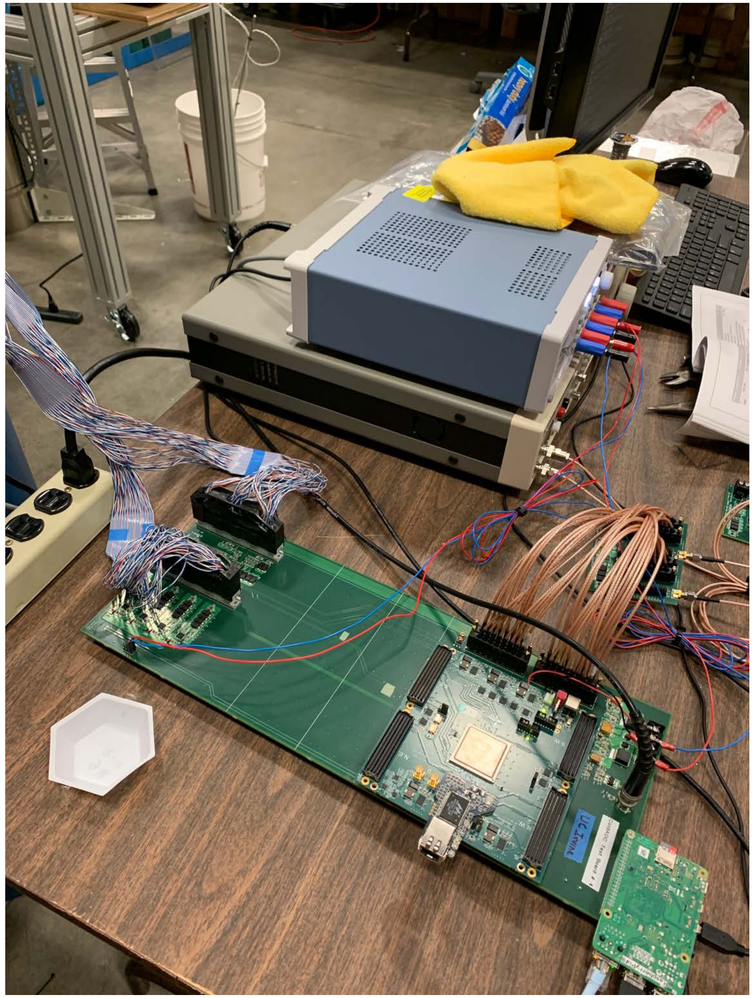
Testing setup



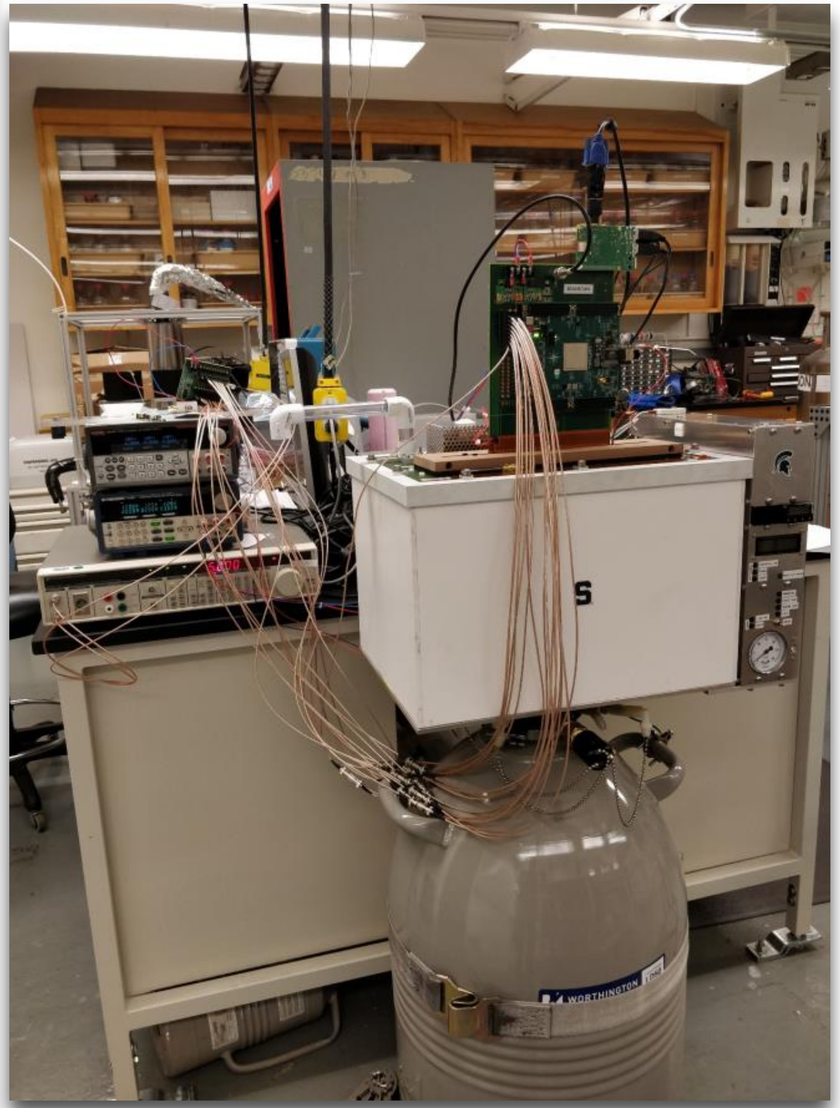
Test stand

Test stand at Irvine: we have the long cable in order to deploy the ColdADC into LN_2



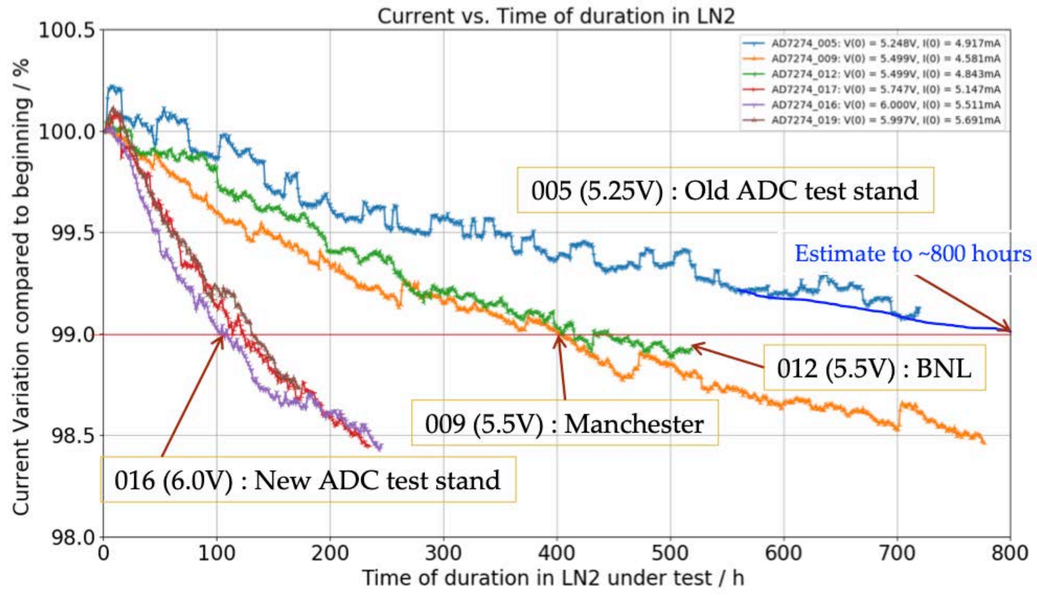


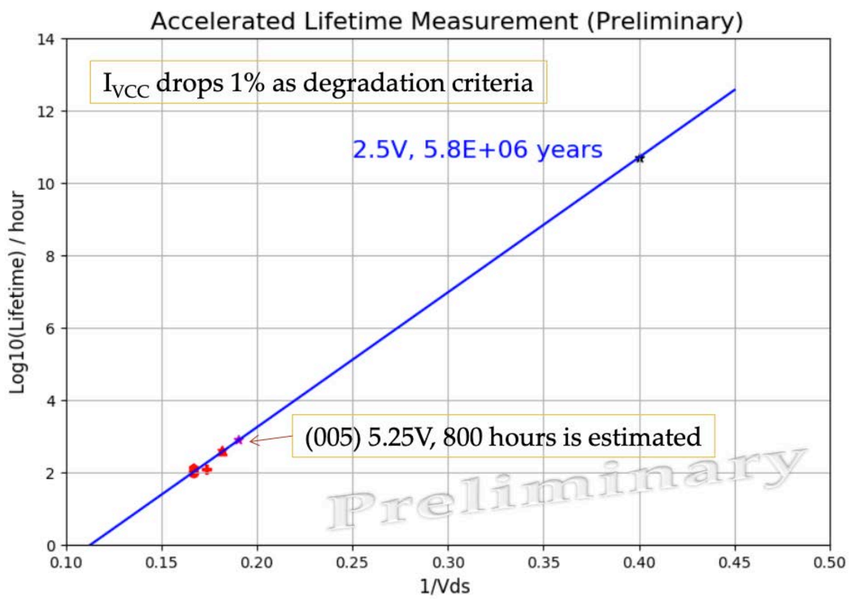
CTS:
half of the mother board with the ColdADC is immersed in LN_2



Lifetime study: Methodology

- Accelerated lifetime measurement
  - ColdADC normally work at 2.25 V for long-term reliability. The lifetime at 2.25 V is at the level of decades.
  - In order to perform the lifetime study, we purposely increase the working voltage, such as 4.2 V and study the lifetime of ColdADC under the high voltage, then extrapolate the results to low voltage.



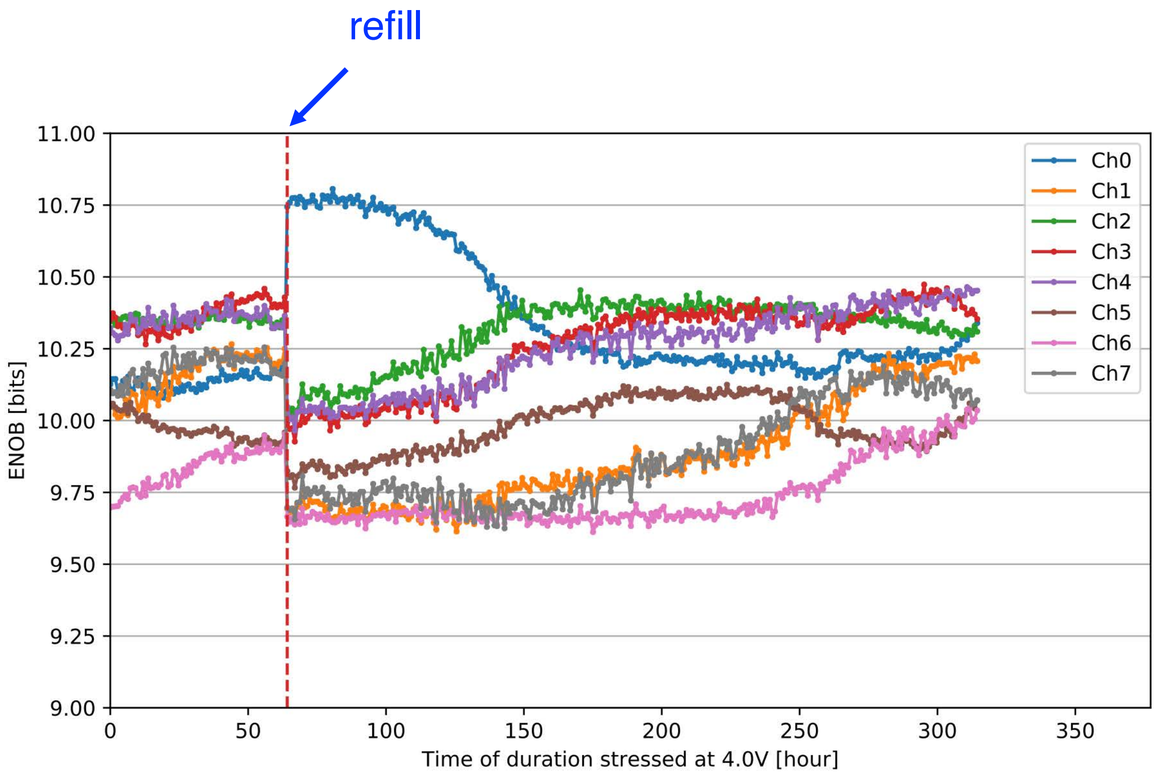


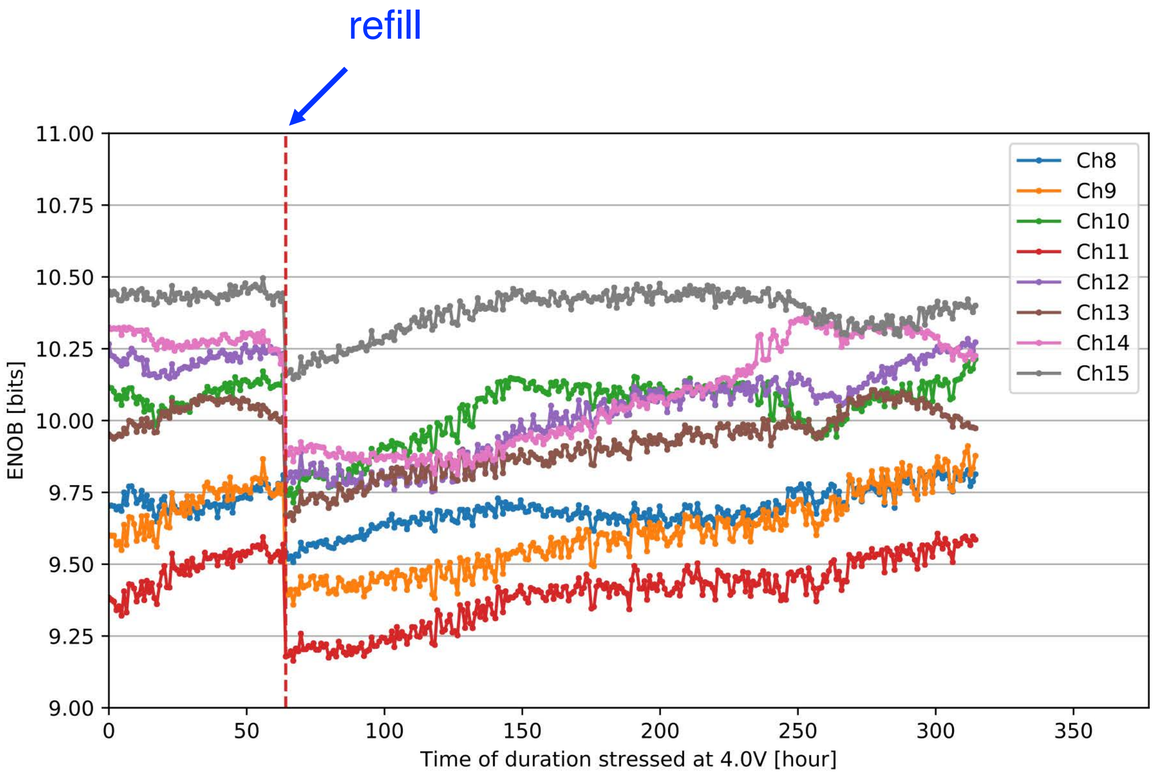
Measurements of the Cold COTS ADC for SBND TPC Readout from H. Chen

Lifetime study

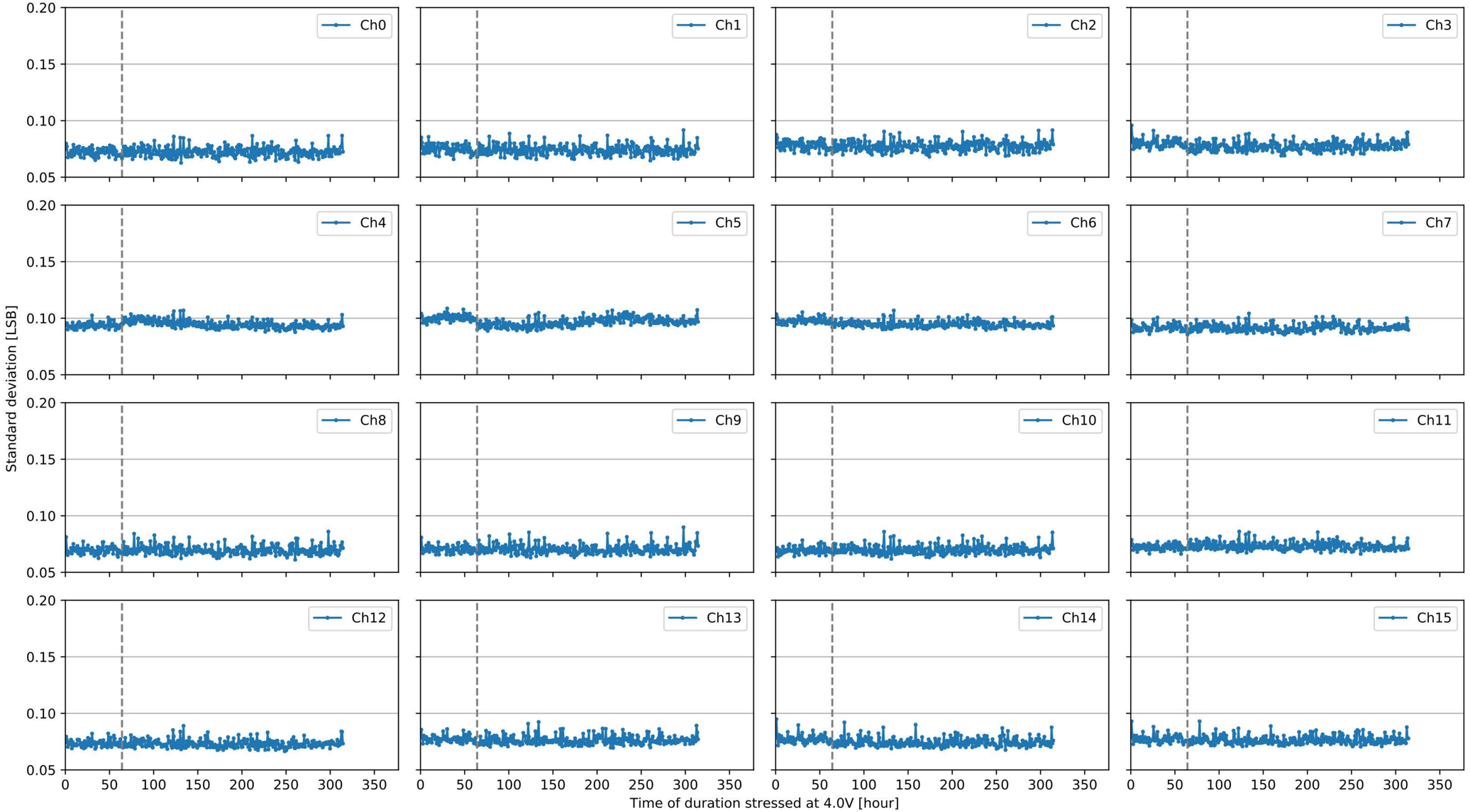
- We improved the test stand and stabilized the data acquisition as the preparation for the lifetime study
  - Tuned the parameter to truncate ADC code in order to exclude outliers of DNL
  - Using averaged FFT results to alleviate the fluctuation of ENOB
  - Shielded the long cable and the dewar with aluminum foil
  - Adjusted the hanging position of the ADC
- Monitoring parameters
  - Dynamic linearity: effective number of bits (ENOB)
  - Static linearity: differential nonlinearity (DNL) and integral nonlinearity (INL)
- Status
  - The method to test lifetime is to increase the stress voltage (4.2V, 4.0V, 3.8V, 3.6 V) and study the degradation of performance
  - Two chips were stressed at 4.2 V, another three were stressed at 4.0 V, 3.8 V and 3.6 V respectively for the last several months

ENOB

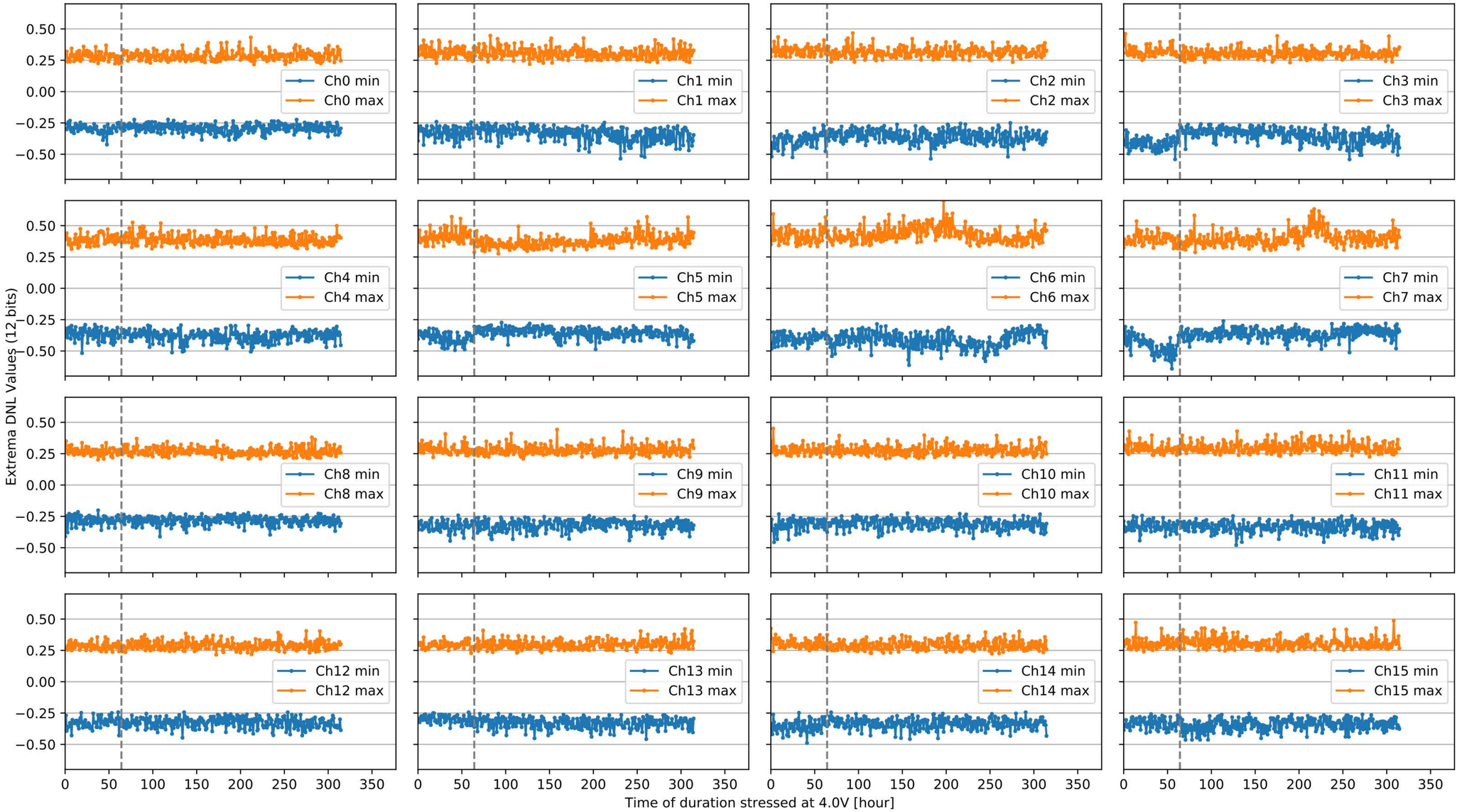

refill
11.00
10.75
10.50
10.25
10.00
9.75
9.50
9.25
9.00
ENOB [bits]
0
50
100
150
200
250
300
350
Time of duration stressed at 4.0V [hour]
Ch0
Ch1
Ch2
Ch3
Ch4
Ch5
Ch6
Ch7


refill
11.00
10.75
10.50
10.25
10.00
9.75
9.50
9.25
9.00
ENOB [bits]
0
50
100
150
200
250
300
350
Time of duration stressed at 4.0V [hour]
Ch8
Ch9
Ch10
Ch11
Ch12
Ch13
Ch14
Ch15

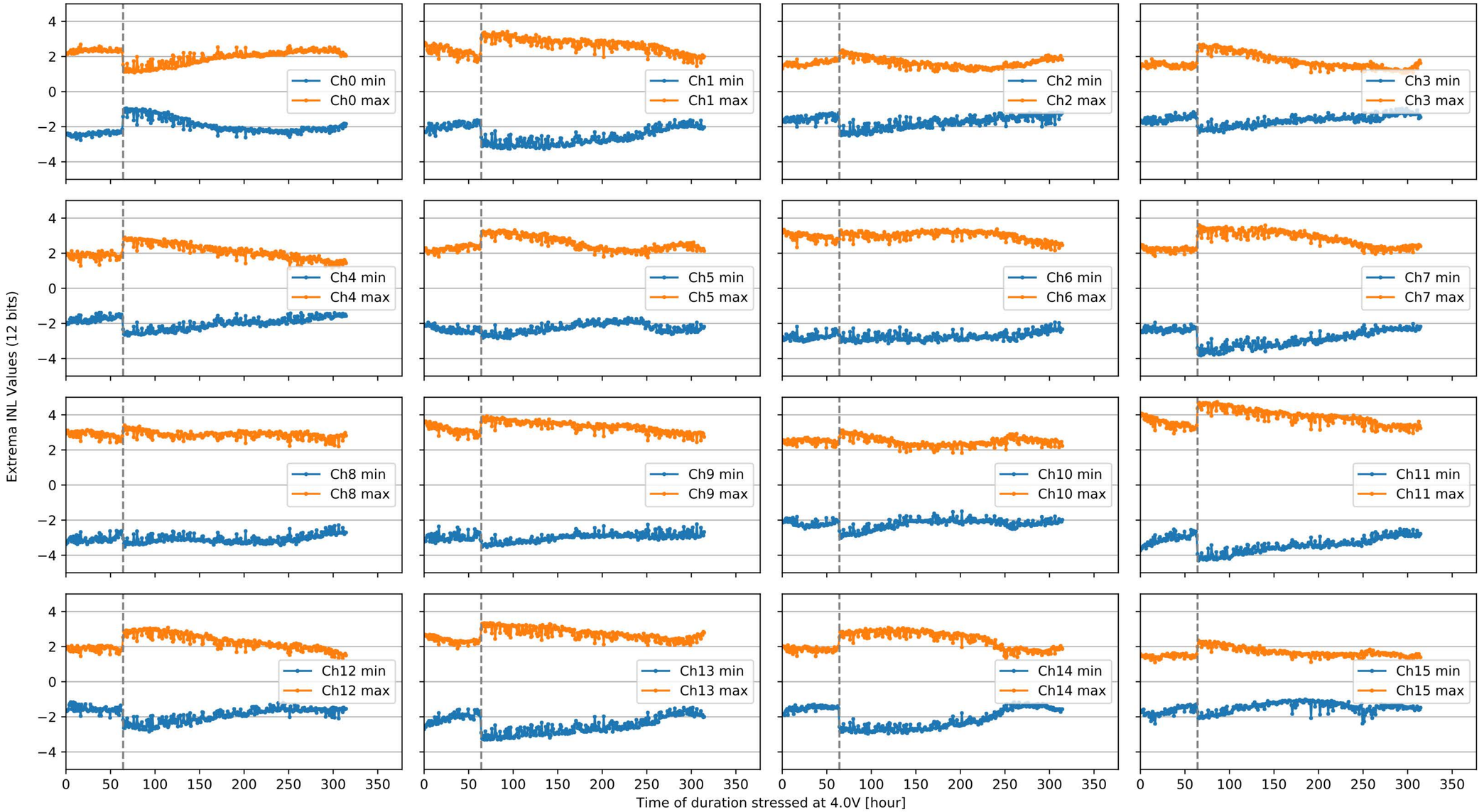
DNL: standard deviation



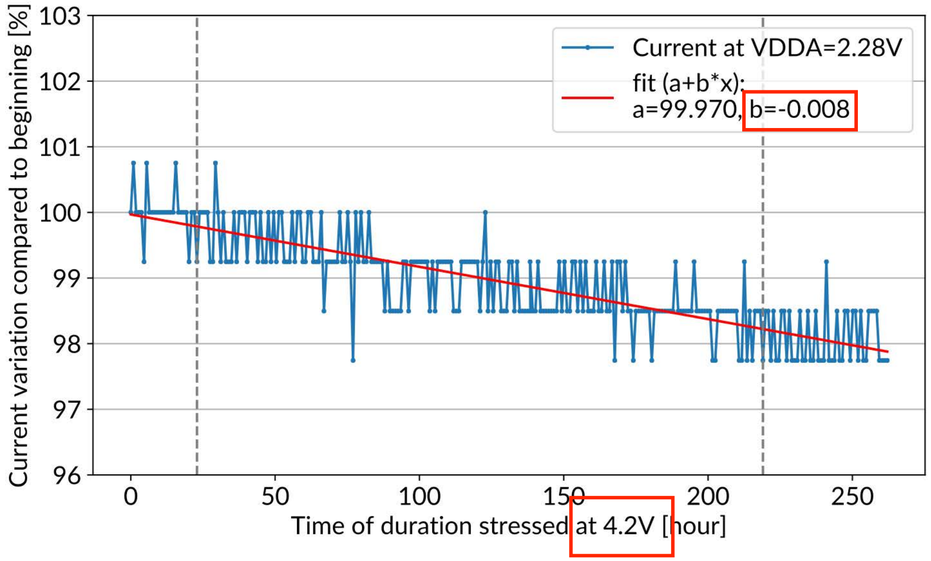
DNL: Extrema

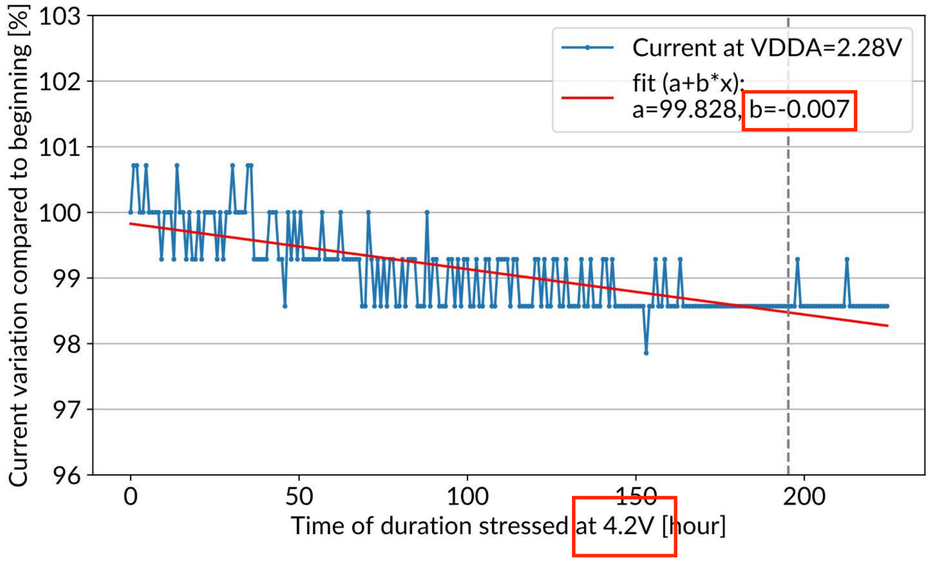

Ch0 min
Ch0 max
Ch1 min
Ch1 max
Ch2 min
Ch2 max
Ch3 min
Ch3 max
Ch4 min
Ch4 max
Ch5 min
Ch5 max
Ch6 min
Ch6 max
Ch7 min
Ch7 max
Ch8 min
Ch8 max
Ch9 min
Ch9 max
Ch10 min
Ch10 max
Ch11 min
Ch11 max
Ch12 min
Ch12 max
Ch13 min
Ch13 max
Ch14 min
Ch14 max
Ch15 min
Ch15 max
Extrema DNL Values (12 bits)
Time of duration stressed at 4.0V [hour]

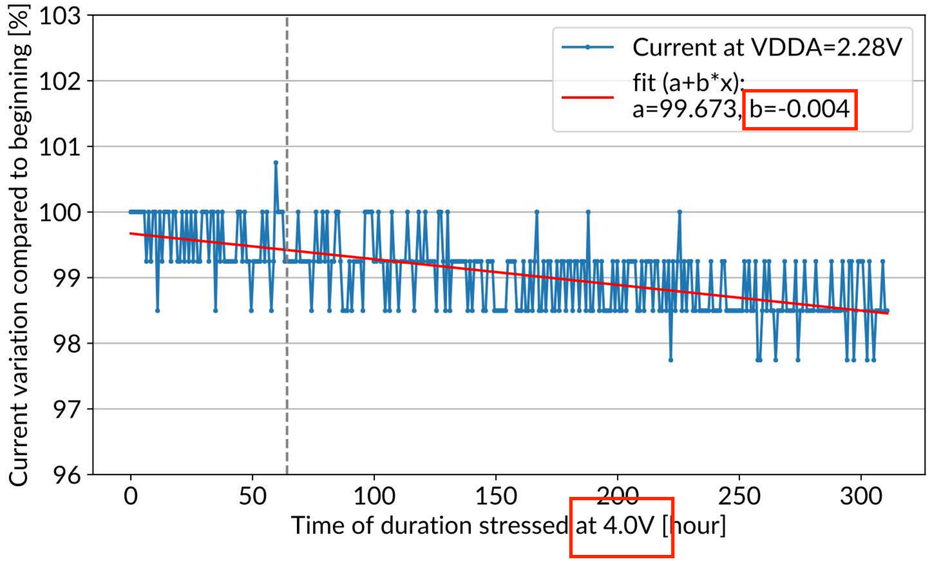
INL: Extrema

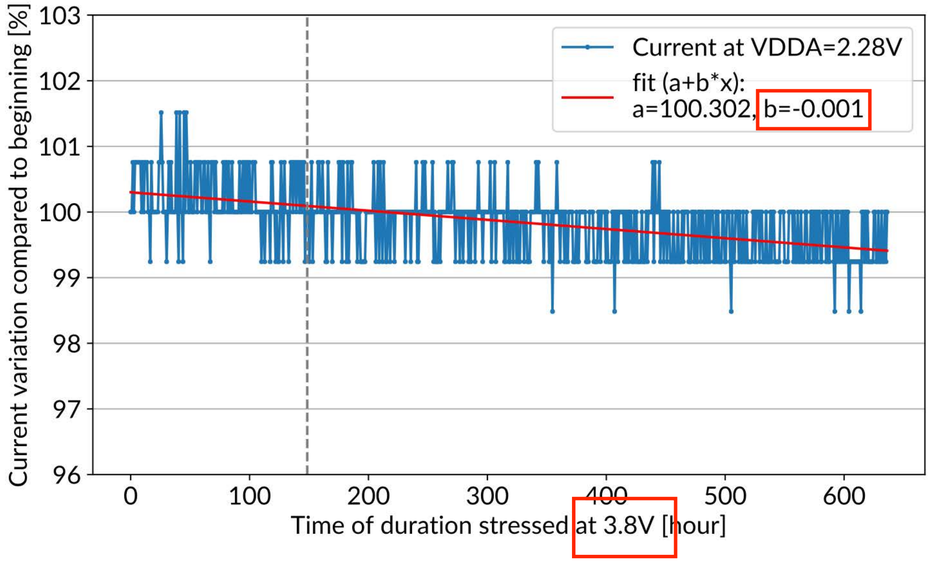

Ch0 min
Ch0 max
Ch1 min
Ch1 max
Ch2 min
Ch2 max
Ch3 min
Ch3 max
Ch4 min
Ch4 max
Ch5 min
Ch5 max
Ch6 min
Ch6 max
Ch7 min
Ch7 max
Ch8 min
Ch8 max
Ch9 min
Ch9 max
Ch10 min
Ch10 max
Ch11 min
Ch11 max
Ch12 min
Ch12 max
Ch13 min
Ch13 max
Ch14 min
Ch14 max
Ch15 min
Ch15 max
Extrema INL Values (12 bits)
Time of duration stressed at 4.0V [hour]

Current at 2.28V VDDA

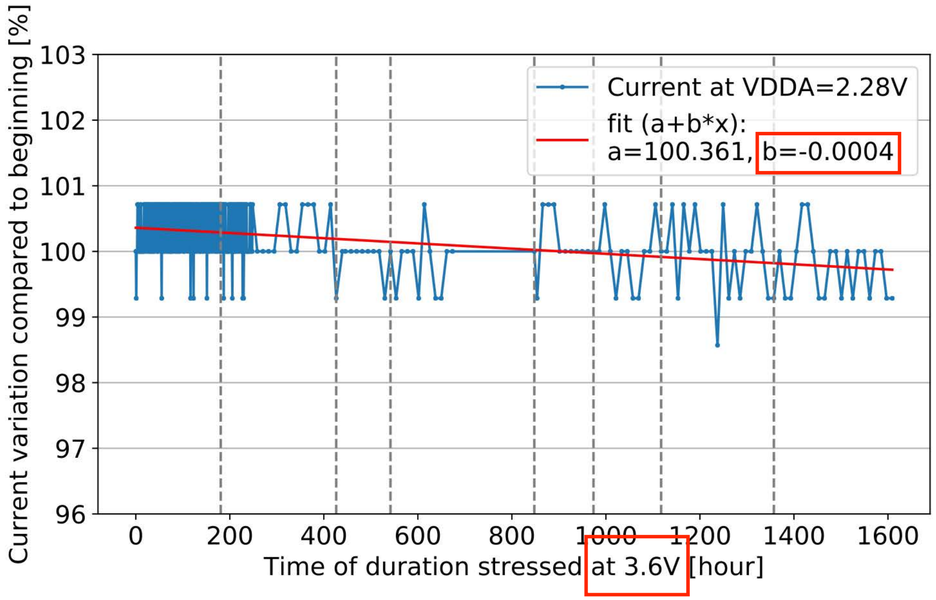






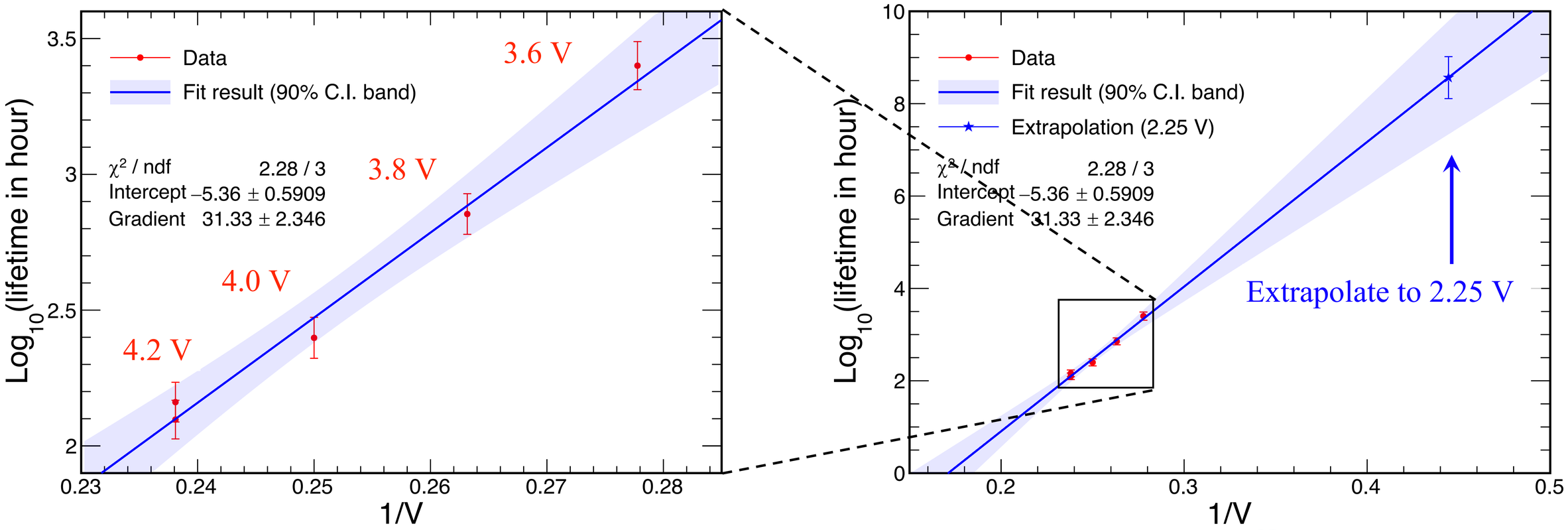


Current at 2.28V VDDA



Lifetime

- **No obvious degradation of the performance (ENOB, DNL, INL) after hundreds of hours testing**
- Given no ADC failed the stress test at the moment, a conservative lower bound on lifetime is extracted by using "current drop of 1%" as the failure threshold (note: ADC performs fine at 1% current drop)
- Use the difference between two measurements stressed at 4.2 V as the uncertainty from chip-to-chip. Use the error output from the fitting as the uncertainty of the measurements. Treat them as uncorrelated
- **It gives a lifetime of 4.2×10^4 years at 2.25 V**



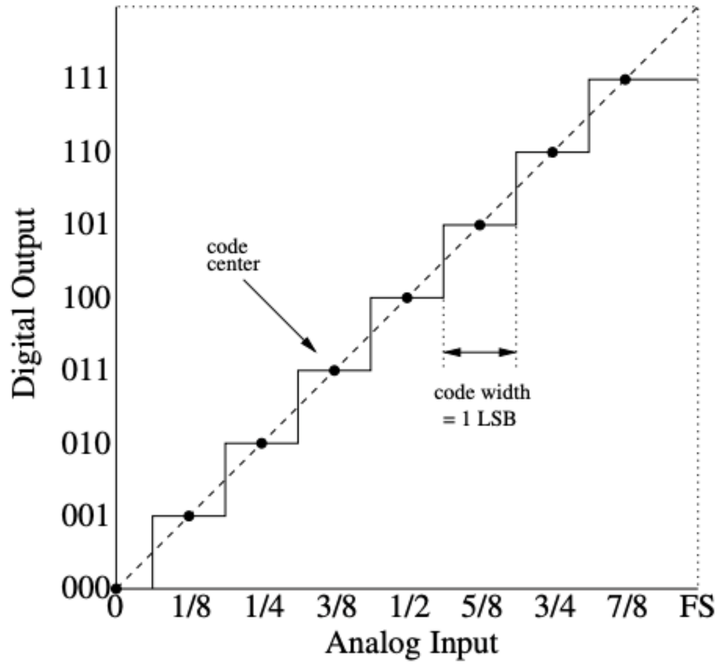
Summary for the lifetime study

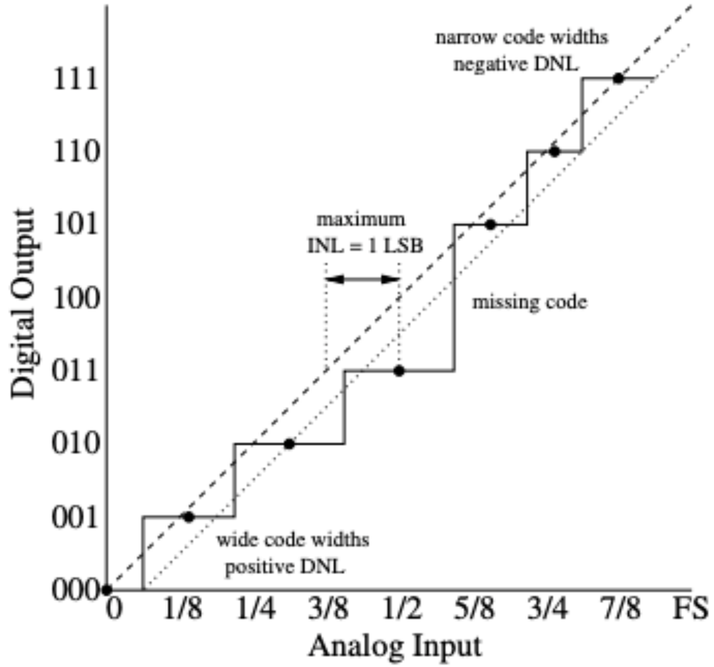
- Accelerated lifetime test at any temperature were performed for both LArASIC and ColdADC (well-established by foundries)
  - transistor is placed under a severe electric field stress (large V), to reduce the lifetime due to hot-electron degradation to a practically observable range
  - It is widely used in industry
- The positive lifetime results on LArASIC suggest for its use in LAr, the lifetime shouldn't represent a concern
- A conservative lower bound on lifetime for ColdADC was measured to be 4.2×10^4 years
  - There is a large uncertainty on the extrapolated lifetime due to lack of data points

Backup

Monitoring parameters

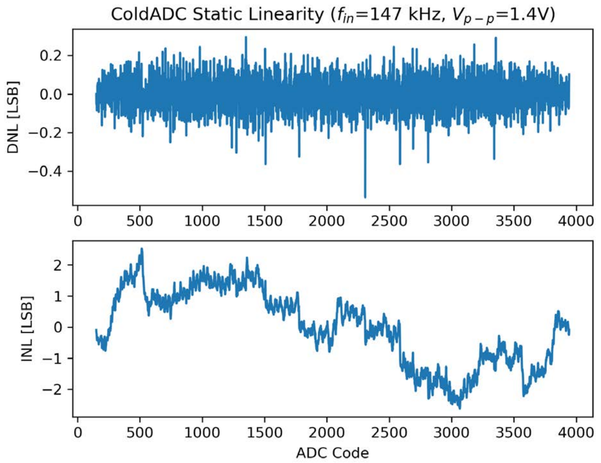
- Static linearity: differential nonlinearity (DNL) and integral nonlinearity (INL)
  - DNL is the deviation of the code transition width from the ideal width of 1 LSB. All code widths in the ideal ADC are 1 LSB wide, so the DNL would be zero.
  - INL is the distance of the code centers from the ideal line. If all code centers land on the ideal line, the INL would also be zero



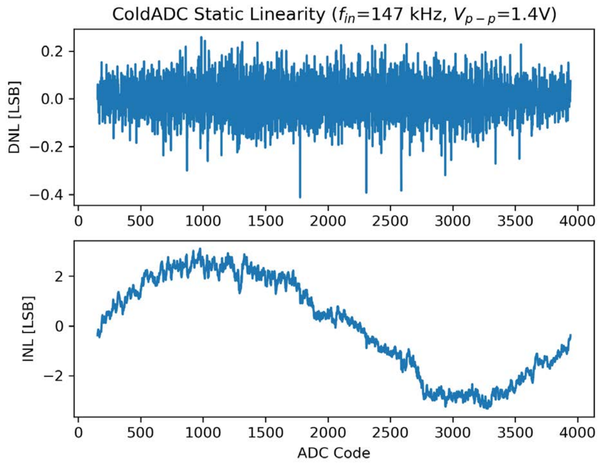


Monitoring parameters

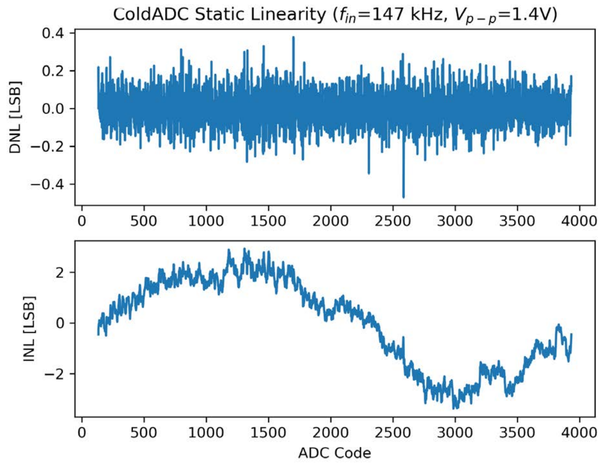
Ch0



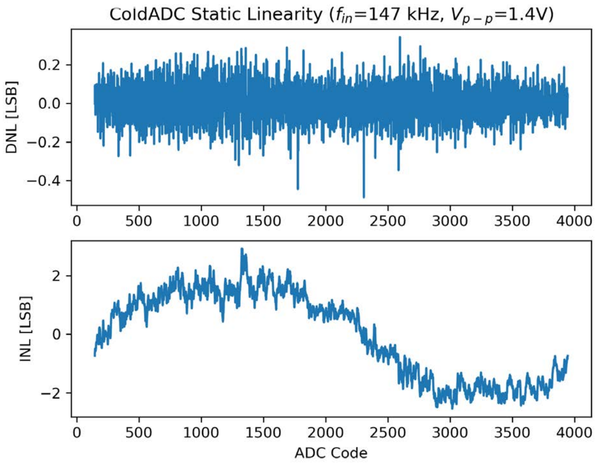
Ch2



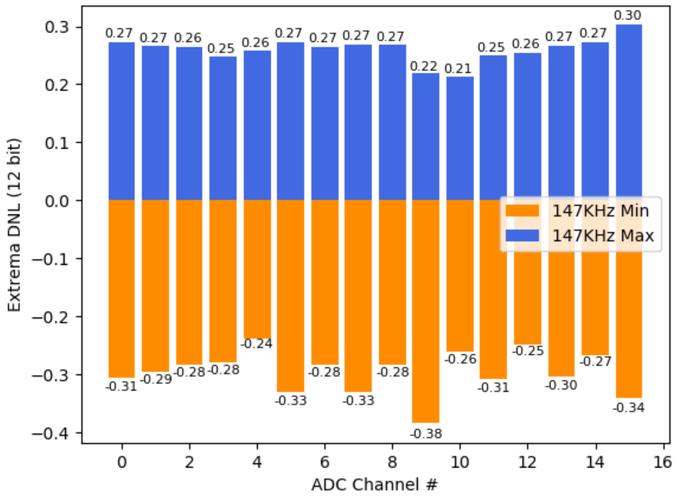
Ch4



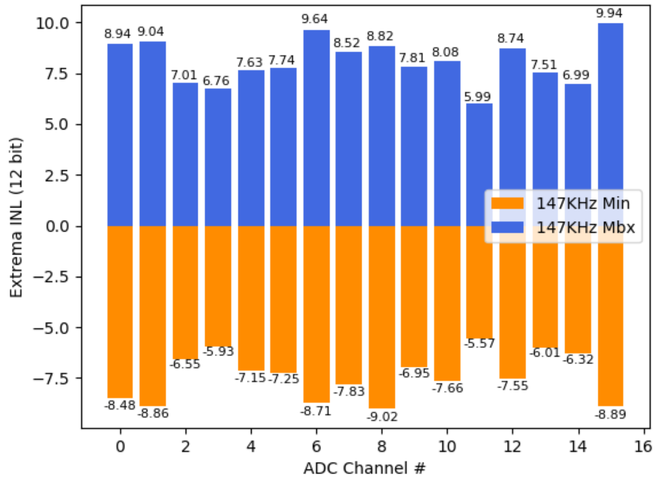
Ch6



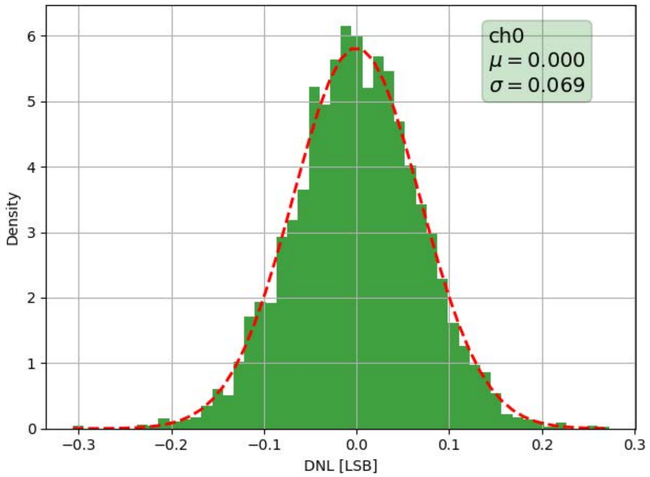
Extrema DNL for each ADC channel



Extrema INL for each ADC channel



Standard deviation of DNL for each ADC channel



Monitoring parameters

- Dynamic linearity: effective number of bits (ENOB)
  - It's the ratio of the input signal amplitude to the rms sum of all other spectral components
  - It's a measure of the combination of nonlinearity and noise