DUNE FD2 BDE PDR
QA/QC Plan

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Quality Assurance (1)

- The QA plan developed here is consistent with the principles discussed in chapter 9 of DUNE far detector technical design report Volume III, DUNE far detector technical coordination
  - The goal of the QA plan is to maximize the number of functioning readout channels in the detector that achieve the performance specifications, particularly on noise.
  - Apart from the number of channels, the most important difference between ProtoDUNE-I and DUNE is the projected lifetime of the detector.
- Cold Electronics
  - 128-CH Front-End Mother Boards (FEMB) installed on the bottom CRPs
  - Cold Cables (Samtec 25m data cable, short miniSAS cable, 25m and short power cable)
  - CRP cable patch panel
  - Feed-through assembly
    - Flange assembly
    - Warm Interface Electronics Crate
      - Warm Interface Board (WIB)
      - Power and Timing Card (PTC)
      - Power and Timing Backplane (PTB)
  - Others (mechanical support structure, and etc)

Quality Assurance (2)

- Design files assurance
  - All FEMB design files, including schematics, layout, BOM, and other relevant files, must be finalized and uploaded to CERN EDMS before the production phase begins.
  - An initial design validation should be performed to confirm the correctness.
  - After that, the design files should be locked, and any modification should be reviewed and approved by the CE consortium.
  - The main design files include:
    - ASIC design documentations (design specifications, production records, datasheets, user manuals)
    - Original schematics files and schematics in pdf format
    - Original layout files
    - PCB fabrication package, including but not limited to gerber and drill files
    - Assembly package, including but not limited to gerber, BOM and position files
    - Mechanical drawings, including cold cables, flange, crate, and etc.
    - BOM and assembly note (requirement)
    - Other relevant files like a list of substitutes, assembly quote or PCB fabrication quotes

Quality Assurance (3)

- Procurement of parts
  - The production of FEMBs requires many large procurements that must be carefully planned to avoid delays. The procurement of ASICs (LArASIC, ColdADC and COLDATA) is included in the ASIC QA/QC plan (https://edms.cern.ch/document/2604783/1). For all other components, several vendors will bid on the same package. Depending on the requirements of the funding agency and of the responsible institution, this may require a lengthy selection process. Vendors must be certified to meet a certain quality standards required by the responsible institution.
    - For example, a BNL-QA-101 form is applied to all vendors if the purchase order is made by BNL Procurement & Property Management Division (PPM).
  - PCB fabrication and assembly will be performed by external companies that meet the quality standard required by DUNE and the responsible institution. A trial run of a small amount should be performed before the large purchase.

Quality Assurance (4)

- QC activities in all sites will be monitored and led by the TPC electronics consortium
  - Maintain central repo for the testing software
  - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup (both DAT and RTS) and the same QC procedure
  - All ASICs to have a unique identifier on the package, COLDATA chips will also have E-fuses burnt during the QC process
  - Plan on testing all ASICs both at room temperature and in LN2 prior to installing them on the FEMBs
    - All ASICs to be place into sockets by pick and place robotic system
  - Test board design is inspired by FEMB design and by test boards used for ProtoDUNE and for initial testing of ASICs during their development

QA/QC Documentation

- DUNE TPC Electronics FEMB/ASIC FDR
  - https://edms.cern.ch/document/2604170/1

Summary of requirements on ASICs	2397298	ASIC_Requirements_v3.docx	Summary list of the requirements affecting the DUNE ASICs
Preliminary Manufacturing and Procurement Plan and Preliminary QC Plan	2604783	**2604783_ASIC_Production_QC**	Document describing the production plans and the preliminary quality control procedures for the ASICs. This includes a detailed description of the measurements to be performed as well as a conceptual design of the test equipment.

LArASIC	2314428	**LArASIC_P5B_Datasheet_V1.pdf**	Datasheet for version P5B of LArASIC. Version P5B is identical to version P5 except that it includes minor modifications (improved input ESD, S16 global bit toggle, as discussed on page 3
		P5LArASICDesignSimulation.pdf	Design and simulation of the single ended to differential buffer.
ColdADC	2314429	ColdADC_Summary_of_Design_Modifications_-_v2.docx	Summary of the design changes introduced between version P1 and version P2 of ColdADC
		ColdADC_Expected_Performance_from_Simulation_v2.docx	Expected performance of version P2 of ColdADC based on simulation
		COLDADC_P2_Datasheet.pdf	Datasheet for version P2 of ColdADC.
		COLADC_P2_Testing_v3.docx	Measurements of ColdADC P2 performance
COLDATA	2314430	**COLDATA_P3_Datasheet.pdf**	Datasheet for versions P3 of COLDATA
		COLDATA_Design_Changes_v3.docx	Design changes from the P2 version of COLDATA to the P3 version (and proposed design chanes for the P4 version).
		COLDATA_P3_Testing.docx	Measurements of the COLDATA P3 performance
FEMBs	2588344	**FEMBDevelopmentPower.20210712.docx**	Document describing the current status of the FEMBs for DUNE and future development. Also included are results from system tests of the FEMBs.
		DUNE_Monolithic_FEMB_Schematics.pdf	Schematics of the current monolithic FEMB prototype
		DUNE_Monolithic_FEMB_Layout.pdf	Layout of the current monolithic FEMB prototype
		DUNE_Monolithic_FEMB_Bill_of_Materials.xlsx	Bill of materials for the current monolithic FEMB prototype

ASIC for DUNE FD2 BDE

- Designed to operate in liquid Argon (87K)
  - Appropriate design rules for operation in cryogenic liquids are used to ensure ASIC will operate with minimal losses of channels throughout the expected lifetime of the DUNE experiment (~30 years)
  - FEMBs in cryostat (liquid Argon) is not accessible for repair or replacement
- Total ~38,000 good packaged chips in need
  - 15,360 LArASIC (P5B) for DUNE-FD2-VD BDE
  - 15,360 ColdADC (P2) for DUNE-FD2-VD BDE
  - 3,840 COLDATA (P4) for DUNE-FD2-VD BDE
  - 10% spares
- Assuming 90% yield of the packaged chip
  - This yield includes warm screening, screening in LN2, installation on FEMBs, FEMB quality control at room temperature, FEMB quality control in LN2
  - **Total ~42,200 packaged chips to be tested**
    - The TPC electronics consortium plan involves having multiple sites using the same QC procedure.
    - The plan assumes each chip passing warm test will be tested at LN2 to assure the cold yield

Strategy for the ASIC cold screening

- Warm QC Screening is necessary
  - QC test at room temperature removes chips with manufacture defects
  - Hardware test setup is easy to extend, easy to operate, and reliable
    - Much less ASIC socket worn-out compared to “Cold” Test
    - Require less resources, such as manpower or cost
- The cold screening test is not reliable enough for high-yield ASIC chips
    - Chip socket is easy to worn-out at cold
    - Cooldown may cause misalignment between chip’s pins to socket’s pads
    - “False” cold test result is foreseeable high
- **Can we skip/minimize the ASIC cold QC screening?**
  - The ASIC QC plan keeps the assumption that there is a cold yield required to perform cold QC test for each ASIC.
  - Because the cold screening of FEMB boards is unavoidable, **if the cold yield is high enough**, a small portion (5~10%) of ASIC will be tested at cold instead of all chips.
    - The ASIC cold failure is a negligible contribution on the yield of FEMB boards
    - The current on-going LArASIC QC for ProtoDUNE-II will provide the statistics result to answer this question.
- All test sites should use the same hardware test setups calibrated by golden reference chips
  - Robotic chip handing system would be helpful to avoid manual handing uncertainty
- QC data storage
  - Test result will be uploaded to the central hardware database
  - Raw data and test result will be backed up locally.

LArASIC QC Items

Test Item	Description	Reference chips	Chips for QC	FEMB QC
Power Consumption	Measure the power consumption on the three rails of LArASIC (VDDP, VDDA, VDDO), for each of six configurations (two baseline references: 200 mV and 900 mV; three configurations of the output buffer: bypassed, single ended, differential)	Required	Required	No
Power Cycling	a number (>5) power on/off cycles, measure the pulse response with a certain configuration (e.g., 14mV/fC, gain, 2.0us peak time, 200mV baseline, 500pA leakage current)	Required	Required	Required
Register configuration	check through SPI interface for register configuration W/R	Required	Required	Required
Bandgap	Measure the bandgap reference voltage	Required	Required	Required
Temperature sensor	Measure the voltage of embedded temperature sensor	Required	Required	Required
Channel response monitoring	Check response of each channel through the monitor pin	Required	Required	Required
Internal DAC measurement	measure INL/DNL of 6-bit DAC (4 ranges for 4 gains)	Required	subset	subset
baseline measurement through monitoring pin	Measure baseline through the monitoring pin (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	subset
baseline measurement	Measure baseline with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents)	Required	subset	subset
Noise measurement	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents). A reference capacitive load of ~150 pF at the inputs.	Required	subset	subset
Calibration with internal-DAC	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	subset	subset
Calibration with external precise source	Measure with ColdADC (4 gains x 4 peak times x 2 baselines x 4 leakage currents) for gain, linearity, range	Required	No	No
Crosstalk	Measure with ColdADC (1 gains x 4 peak times)	Required	No	No
Internal calibration capacitor measurement	Measure the capacitance of the calibration capacitor	Required	subset	No

ColdADC QC Items

Tests 1-6 are performed first at room temperature, then in LN_2

1. Power on/off cycles (at least 5)
2. Measure power consumption in 4 rails (V_{DDA2P5}, V_{DDD2P5}, V_{DDD1P2}, V_{DDIO})
3. Test I2C communication with chip
4. Test chip starts up in appropriate state after reset
5. Perform autocalibration procedure
6. Use sine wave with frequency of 150 KHz and amplitude of 1.6-1.9V to verify all channels are functioning

Following tests are performed in LN_2 only

7. Measure reference voltages for BGR and CMOS reference block
8. Determine dynamic range / check overflow is working with 2V sine wave or slow ramp
9. Make ADC performance both with single ended / differential input (determine INL, DNL, ENOB, noise) using 150 kHz sine wave (amplitude 95% of dynamic range). Use 14 bits readout, no offline non-linearity corrections
10. Measure frequency of ring oscillator
11. Measure cross-talk on a subset of the ASICs

Determine acceptance criteria will be after ProtoDUNE-II HD&VD

> 1,000 chips tested from the engineering run

COLDATA QC Items

1. Power on/off cycles (at least 5)
2. Measure power consumption in 5 rails (V_{DDIO}, $V_{DD\_LArASIC}$, V_{DDCORE}, V_{DDD},V_{DDA})
3. Test I2C both on LVDS lines and CMOS lines
4. Test chip starts up in appropriate state after reset
5. Assign (and read back) unique identifier by burning eFuses
6. Check clocks sent to COLDATA (62.5 MHz, 1.953125 MHz, check 32:1 ratio, check jitter)
7. Checking tuning parameters for PLL
8. Verify Fast Commands (Reset, Edge, Sync, Act)
9. Check data transmission to the WIB (data formats, eye diagram)
10. General purpose I/O bits on the FEMB

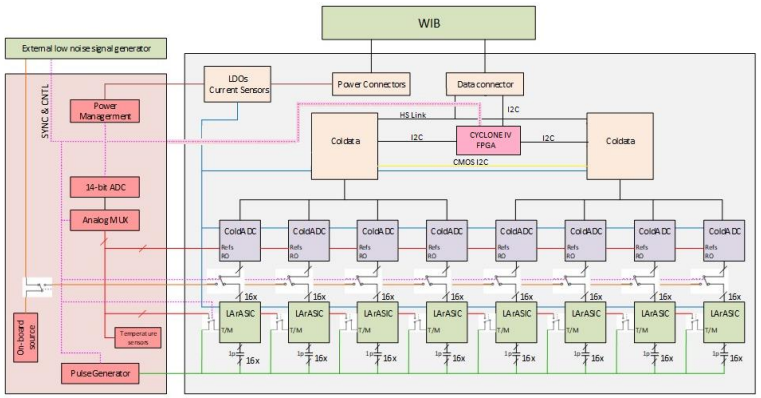
All measurements to be repeated in LN_2

Exact acceptance criteria will be defined after testing a sizeable number of ASICs from the engineering run

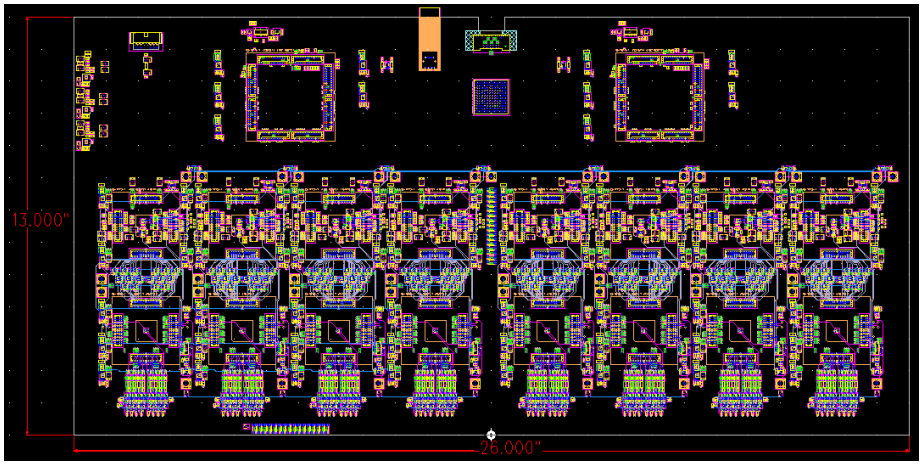
ProtoDUNE-II HD&VD: ~300 COLDATA chips

Hardware: DUNE ASIC Test Board (DAT)

- DUNE ASIC Test (DAT) Board
  - Unified ASIC test board for LArASIC, ColdADC, and COLDATA QC
    - Compatible power and data interface with WIB. It acts as exactly as a FEMB to WIB
    - Can perform QC testing for 8x LArASIC, 8x ColdADC and 2x COLDATA at both RT and LN2 with MSU new RTS
    - Aim for DUNE-FD1 & FD2 ASIC QC carried out in several test sites
  - A single big board solution with ASIC socket mezzanines
    - ASIC socket suffers mechanical degradation through thermal cycling
    - More commercial semiconductor devices have been identified for cryogenic operation
      - Such as Analog MUX: SN74LV4051, Power Monitoring Chip: INA226, I2C Bridge device: PCA9306, DAC: AD5675ARUZ
  - Unified ASICs and FEMB QC with the same SW set
    - Can benefit directly from the WIB, back-end DAQ, **analysis software developments**
    - Some extra software effort for ASIC QC can be implemented as a widget to the available software



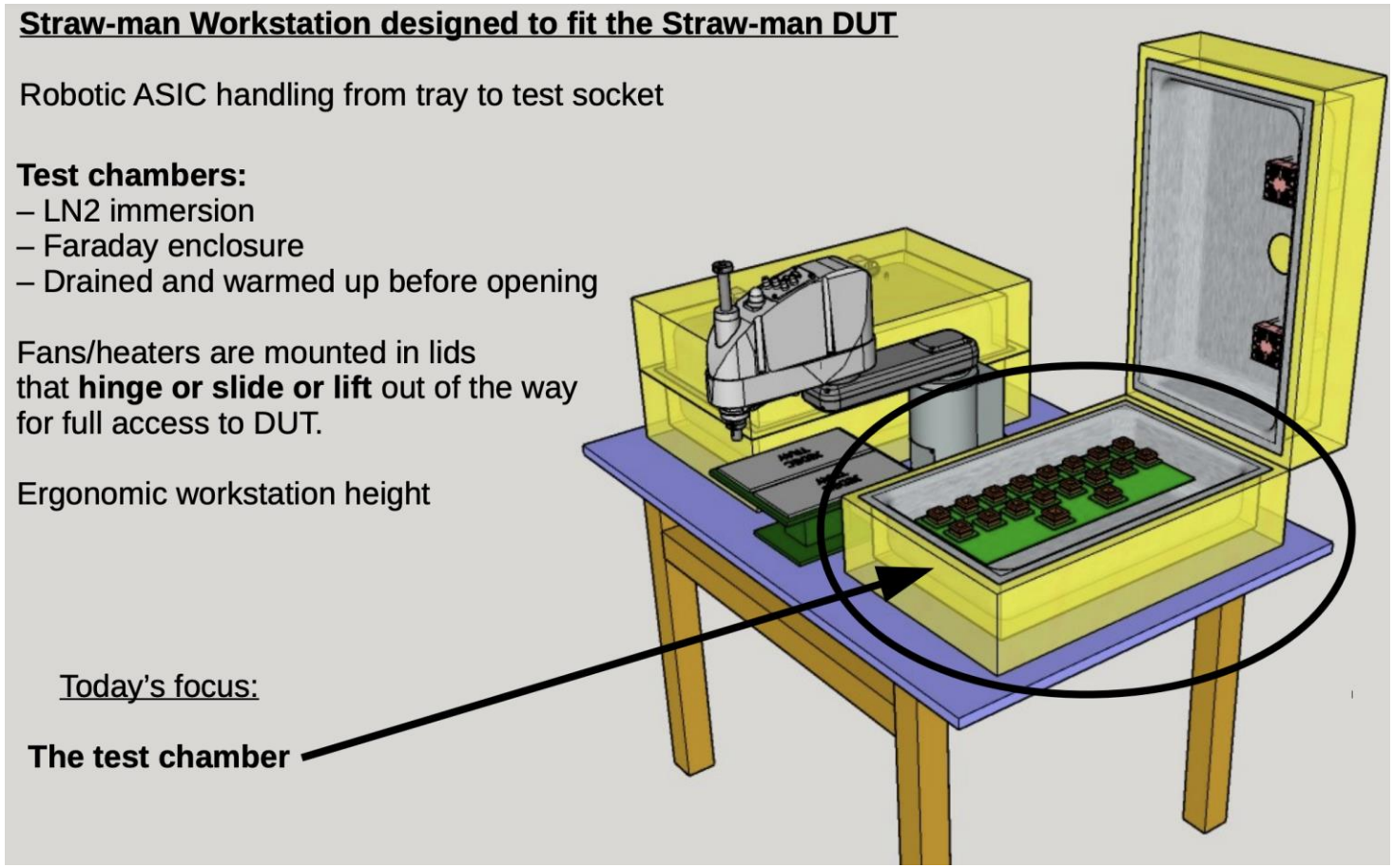
Schematics is done, layout is ongoing



Board size is 13”x26”

Hardware: DUNE RTS

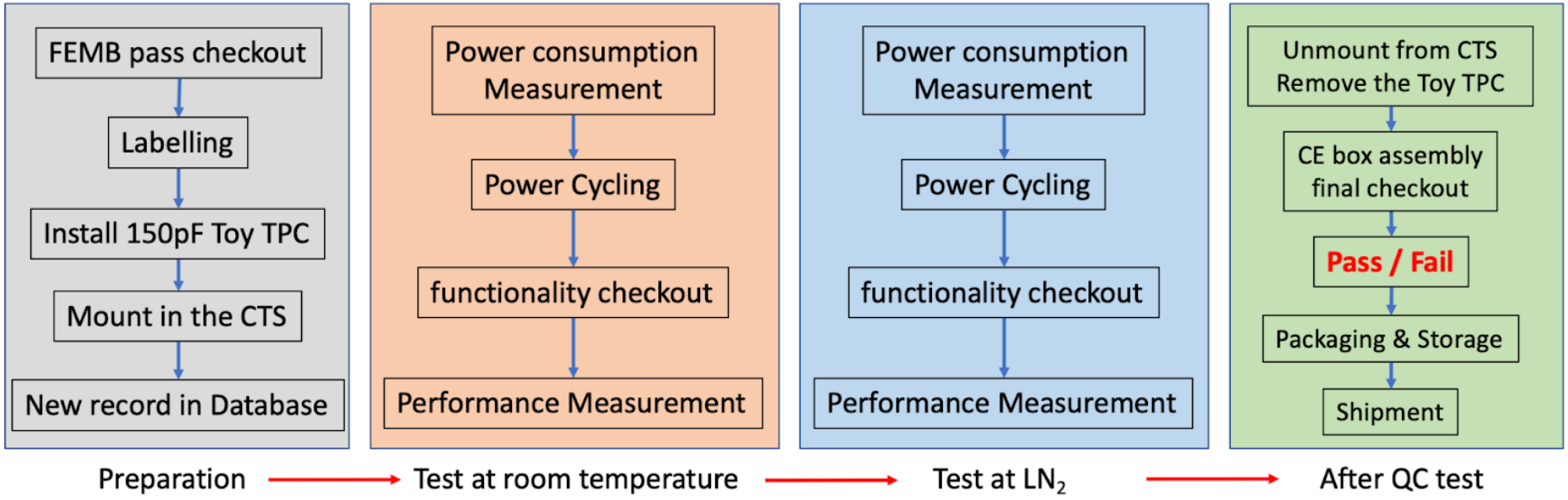
- Robotic Testing Station



RTS is designed by Dean Shooltz, Kendall Mahn, Carl Bromberg from Michigan State University

FEMB QC Procedure

- All data from the QC process will be stored in a common database, and the yields of the production will be centrally monitored and compared among different sites.



FEMB QC

- FEMB PCB fabrication confirmation
  - The PCB fabrication house provides a test report of electrical continuity and shorts test
  - Visual inspection for a few bare boards of each production batch
- Post-assembly FEMB checkout
  - A visual inspection should be performed before power on
    - Missing soldering, Extra soldering paste on board, Extra components on board, Insufficient cleaning. …
  - A FEMB checkout test
    - Power consumption is normal
    - All communication links are good (high-speed links, I2C, fast command, and monitoring)
    - Consistent calibration pulse response of each channel on board
    - Reasonable baseline of each channel
    - Reasonable noise distribution when the input is floating
  - Only a FEMB passes the checkout can be accepted as a qualified unit for the QC testing. A routing QC procedure for a CE box assembly starts from here.
  - The similar checkout procedure will also be necessary later during the reception test of CE box assemblies and cold cables when they arrive at the destination (South Dakota).

Checkout Test Report (example)

Identifier

Temperature

Note

Tester

Configuration

Power consumption

Monitoring

Noise Distribution

Pulse response

1-cycle Waveform overlap (128CH)

Averaging Waveform overlap (128CH) for noise environment

FEMB#0009 Checkout Test Report

FEMB ID = 0009
Date&Time: 2022-04-24 15:20:15
WIB_TCP_Version: 0x100
Temperature: RT
Note: setup#1 ToyTPC_1_2, 22m samtect data cable, 9m power cable

Tester: SG
WIB_UDP_Version: 0x1a5
Input Capacitor(Cd): 150pF

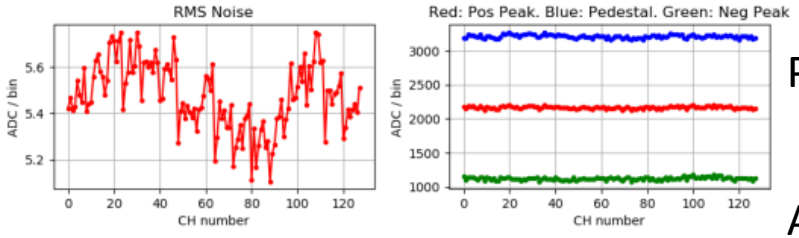
FEMB Configuration
FE_CFG: 14mV/fC, 900mV BL, 2.0us, SE_OFF, 500pA, ASIC_CAL, ASICDAC=0x10
ADC_CFG: CMOS reference set to default, Auto Calibration,
ADC_CFG: SE, SDC off, offset_binary_format, Auto Calibration,
CD_FE_pulse: 500 samples/pulse, CD Addr0x06:0x30,0x07:0x00, 0x08:0x38, 0x09:0x80

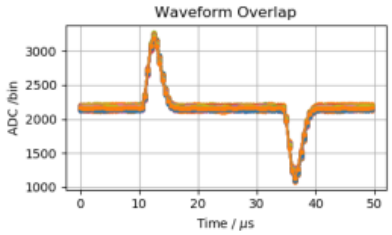
Power Consumption (including cable dissipation) = 6.397W

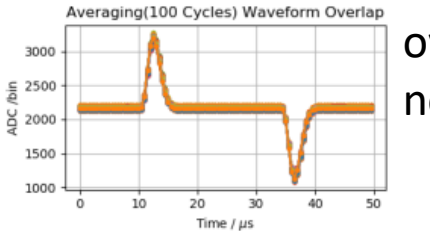
Power rail	V_set /V	V_meas /V	I_meas /A	P_meas /W
LArASIC	3.000	2.962	0.431	1.277
ColdADC	3.500	3.408	1.291	4.402
COLDATA	2.800	2.768	0.217	0.600
BIAS	5.000	5.000	0.024	0.118

Monitoring path for FE-ADC#0 (unit: mV)

ASIC#	FE Vref	FE T	ADC VCMI	ADC VCMO	ADC VREFP	ADC VREFN
0	1245.000	940.000	959.000	1241.000	1948.000	530.000







FEMB QC Items

- Preparation Phase
  - Install two 64-channel 150 pF Toy TPC boards on each FEMB
  - Place FEMB into the CTS/RTS
    - Up to 4 boards may be tested simultaneously to improve efficiency
    - A new item will be created in the database for each CE box assembly with the initiation information, such as date and time, test setup number, CE box serial number, location, name of who performs the test, and so on
  - **Phases of tests at room temperature (RT) / liquid nitrogen (LN2)**
    - Power consumption measurement
    - Power cycling test (optional at RT, mandatory at LN2)
    - Functionality checkout
    - Performance measurement
  - Phase of post-QC test
    - FEMBs passed the cryogenic test will be installed in the CE box
    - A similar fast checkout test should be performed to finalize the QC test
    - A judge of **pass**/**fail** CE box assembly thus will be made before packaging

FEMB QC Items (Functionality checkout)

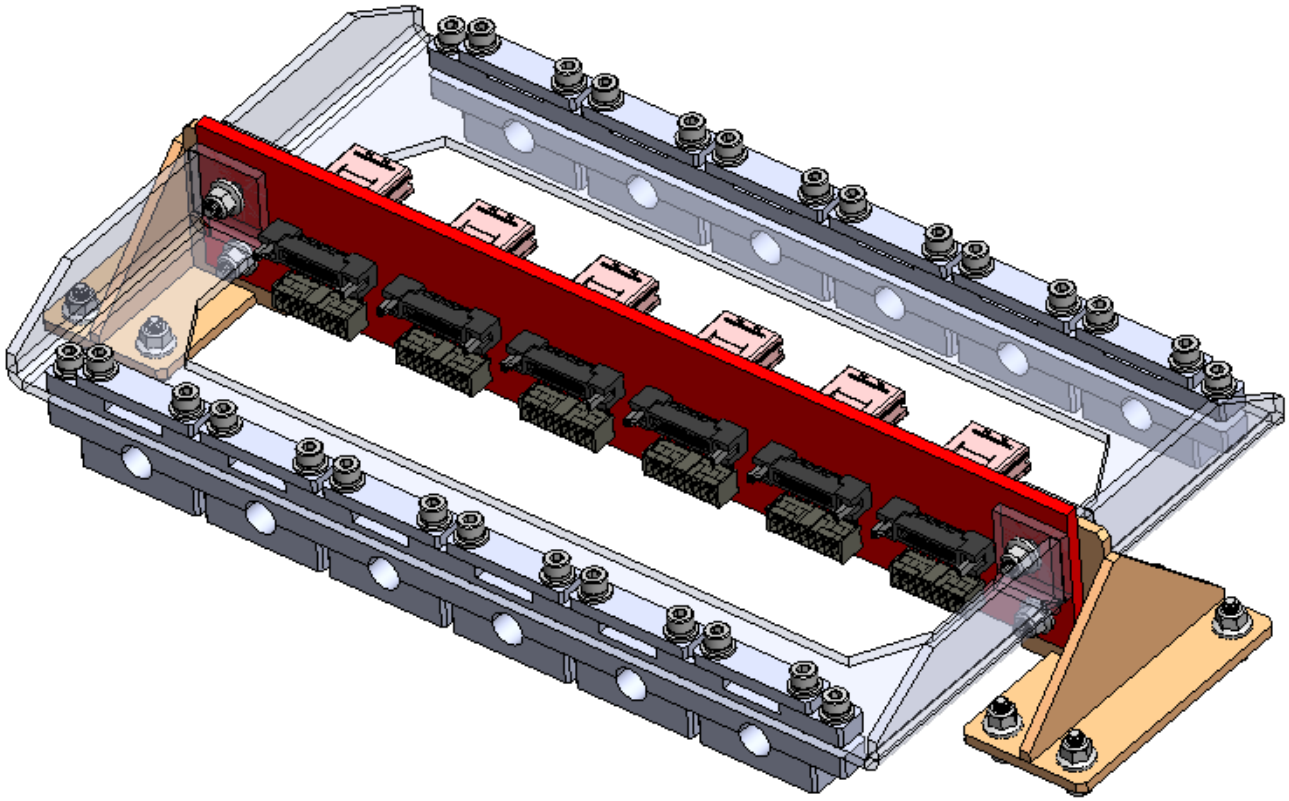
Item	Description	Expected output
Communication links	I2C and FAST command communication between Coldata and WIB I2C communication between ColdADC and Coldata SPI communication between LArASIC and Coldata Data pattern from ColdADC all the way to the WIB	No communication failure or error
Reset	COLDATA can be reset into the default state LArASIC and ColdADC can be reset by COLDATA. After the reset the chips come up in the default state	Pass/Fail
ColdADC reference voltage measurement & scan	Measure the four reference voltages for both the bandgap reference block and the CMOS reference block (the four voltages to be measured are: VREFP, VREFN, VCMI, and VCMO). A few scan points to assure the reference voltages are adjustable	Voltages of references should be in required range and adjustable
LArASIC bandgap & temperature measurement	Measure the bandgap reference voltage Measure the embedded temperature sensor voltage	The values are in the acceptable range
LArASIC DAC measurement	Measure the 6-bit DAC voltages with 64 settings	DNL/INL are in the acceptable range
Pulse response	The FEMB accepts the external calibration pulse from WIB. All channels should have a consistent response. Two combinations will be measured (single-ended or differential interface between LArASIC and ColdADC)	Pass/Fail

FEMB QC Items (Performance measurement)

Item	Description	Expected output
Noise & pedestal measurement	Noise performance will be evaluated with a 150 pF capacitive load. LArASIC will be set to 14 mV/fC gain and 500 pA leakage current with 8 combinations (900mV/200mV baseline, 4 peaking times) The single-ended interface between LArASIC and ColdADC will be in use	Noise & pedestal in the acceptable range
Gain measurement (coarse)	The single-ended interface between LArASIC and ColdADC will be in use Gain measurement is done by the ASIC embedded calibration pulser 32 combinations, a coarse measurement is preferred (4 gains x 4 peaking times x 2 baselines)	Gain under each configuration should be in the acceptable range
Linearity and range measurement	The single-ended interface between LArASIC and ColdADC will be in use Linearity measurement is done by the ASIC embedded calibration pulser. LArASIC is configured with 14mV/fC gain, 2 us peaking time, 200 mV baselined and thus calibrated by 64 charge points generated by ASIC internal DAC.	<1% non-linearity at required linearity range (100 pC)

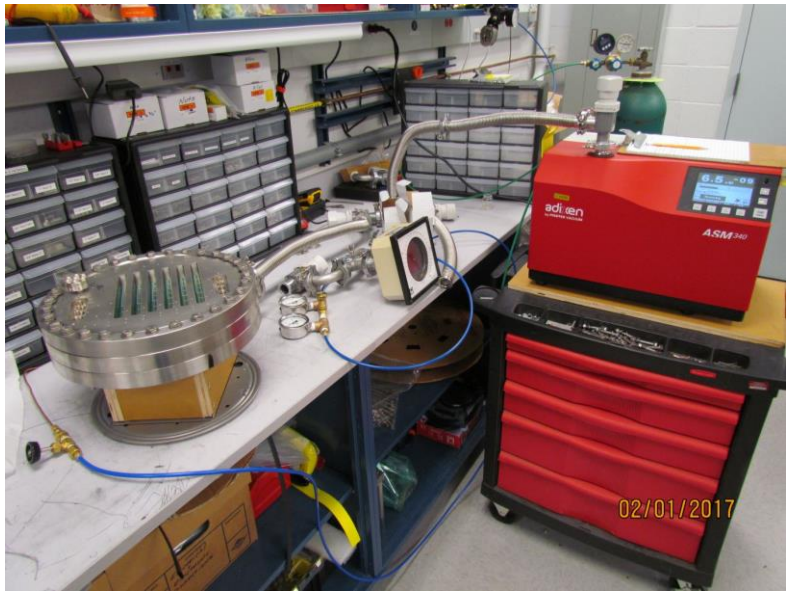
CRP Cable Patch Panel QC Items

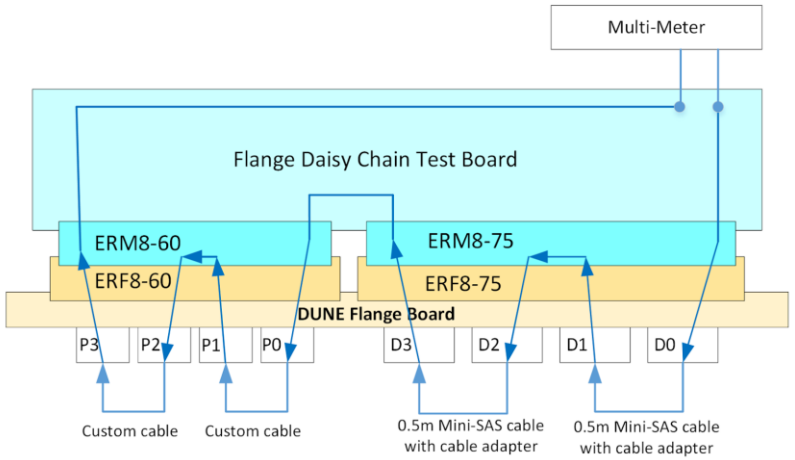
- The design of the CRP Cable Patch Panel is being finalized
  - The patch panel only consists of connectors, the QC procedure should include the continuity test, and warm-cold cycle test.



Flange QC Items

- Leak test
  - Every signal feed-through assembly will go through a standard leak test before it is used to mount the WIEC.
- Cold cable continuity test
  - The risk of cable continuity is very low because cables are manufactured by qualified manufacturers which meet the required industry standard with QA/QC.
  - Materials used for cold cable production must be under control. Only the permitted materials (e.g. wire, connector) are allowed to use during cable production.
- Flange board continuity test
  - The continuity test is the QC procedure for the flange board.





WIB QC Items

Test item	Description	Expected output
WIB Power management (hardware dongle)	Validate all WIB power rails are operational and are in expected range through LTC2977 power management IC	Use “LT powerplay” software and DC1613A dongle for verification
FPGA initialization testing	SD Card & JTAG programming of the FPGA	Front panel LED & UART status
TCP/IP communication	The TCP/IP connection is built between the WIB and the host PC	WIB pass “ping” test
On-board power measurement (Linux interface)	Voltage/current of each power rail through software monitoring (I2C) LTC2991 and LTC2990	In the expected range
On-board I2C devices detection	FPGA detects all on-board I2C devices	All I2C devices work
FEMB power management	Voltage/current of each power rail can be set/monitored	In the expected range
DDR check	Read/write, burst mode	Pass or fail software test
PTB interface	12V power from PTB Receive system clock from PTB Identify WIB address	Verify all connections to PTB

WIB QC Items

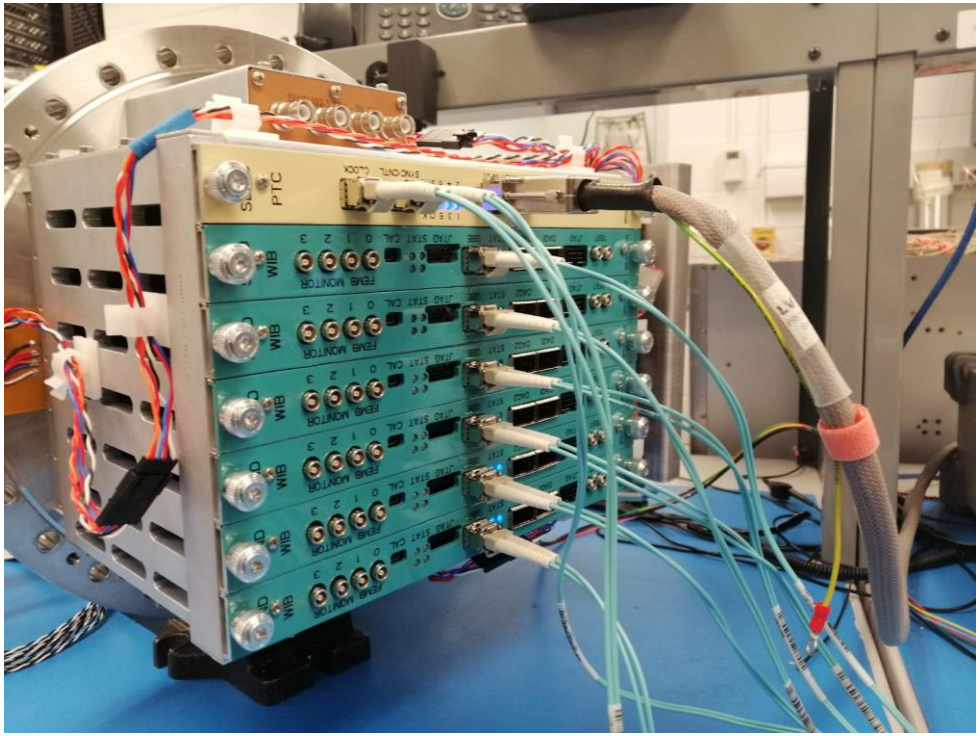
Test item	Description	Expected output
Communication between WIB & FEMB (FEMB interface)	WIB ⟷ WIB adapter board ⟷ 4 FEMBs I2C command Fast command Clock Data links External calibration path (FEMBs are configured to accept external calibration pulser control by WIB)	Receive correct data pattern from FEMBs
FEMB calibration/monitor verification	On board DAC8411, ADC and external calibration verification	An external calibration source should be used to calibrate the ADC which then can be used to verify the on board DAC for each FEMB
Timing interface	Verification of all timing paths front and back panel connections. Will also verify ADN2814 and SI5344 functions. Back panel connection will require PTB & PTC or a test dongle.	FPGA can generate a pass or fail for timing chain
IBERT test	Vivado IBERT tool TX ⟷ fiber ⟷ RX	Can't be done by self-checkout test. This can be done using test firmware but some development will be required.

PTC QC Items

- The design specification of DUNE PTC hasn’t been finalized

Final walk-through QC for WIEC

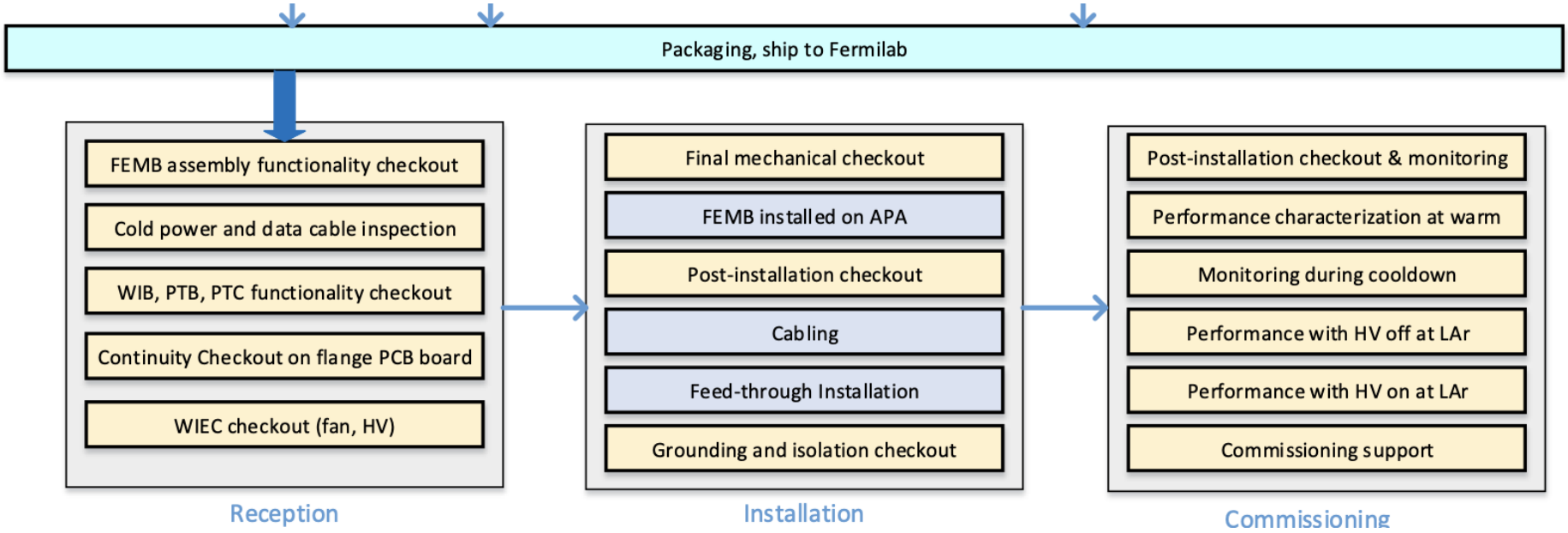
- A final walk-through test will be performed to confirm no defect caused by installation before the shipping
- Reception test should be performed in South Dakota before the assembly is installed on the cryostat.



A final walk-through test setup for SBND

QC for Cold Electronics Installation and Integration Test

- The installation procedure will be developed in ProtoDUNE VD



SBND cold electronics installation procedure

QC Management

- QC activities in all sites will be monitored and led by the TPC electronics consortium
  - Maintain central repo for the testing software
  - Each site admin updates the controlled system deployment in coordination with local operators
- All test sites share use the same hardware setup (both DAT and RTS) and the same QC procedure
- Identifier
  - EDMS-2505353 specifies a scheme for identifying all the detector components
- ASIC/FEMB handling
  - ASIC belongs to MSL level 3
  - Follow Standard IPC/JEDEC J-STD-033
    - Handling, Packing, Shipping and Use of Moisture, Reflow, and Process Sensitive Devices
- QC data storage
  - The hardware database is getting close to a useable state (Paul Laycock)
    - (to do) define what data needs achieved to form the component template for the hardware DB. The component template just defines what data is associated with each object.
    - A test summary in a data interchange format (e.g. HDF5, CSV, JSON) will be stored in the central hardware DB
  - All the raw data from testing is achieved locally

Summary

- The construction of ProtoDUNE-II HD&VD will gain our experience for DUNE FD2 BDE QA/QC
  - Especially, FD2 BDE will significantly benefit from FD1 CE
- Qualify assurance is well explored and understood
- 5-level qualify control is explored
  - Component: LArASIC, ColdADC, COLDATA, cold cables, connectors, commercial parts
  - Board: FEMB, WIB, PTC, PTB, Flange, Patch Panel
  - Assembly: CE box, WIEC
  - Reception
  - Infrastructure
- QC management and data storage is being detailed in the coming months
- QA/QC will be finalized with the experience gained in ProtoDUNE-II HD&VD.

backups

Performance Characterization vs. QC Testing

- Performance Characterization
  - has the ASIC met all the functionality requirement?
  - explore the optimal configuration for the ASIC
  - investigate potential design/manufacture defects
  - focus on a small batch of chips
    - functionality and performance are thoroughly studied
  - a golden reference for QC is determined during the performance characterization
- QC testing
  - **Develop a criteria to screen the ASIC chip after ASIC is completely characterized**
    - Normally, it is not necessary to get the optimal performance during QC. It is more important to gain the consistent performance for majority of chips.
  - Most failure modes have been identified during the performance characterization
    - There could be few failure modes later recognized during the early stage of the QC activity
    - Performance characterization and QC can't assure all potential failure modes are addressed
  - Result of QC testing
    - **PASS**: the chip passes the pre-defined tests, achieve the performance consistent with the golden reference
      - Possible criteria: cut ASICs with any of those values >3(?) sigma from channel expected response
    - **FAIL**:
      - A pre-defined failure mode is observed
      - Its performance is out of tolerance range compared to the reference chip
  - Reliable and easy-handle QC test stand, clear and routinely QC testing procedure
    - A non-expert with a couple of hours training should be able to perform the QC testing
    - QC test stand and the test procedure should be able to prevent an operator from making mistake
      - The test should be automatically performed once the chip is installed in the socket
    - Considering 60-minute thermal cycle, < 10-minute testing time per chip is acceptable, <90 minutes for FEMB board