HEP-CCE Status

SCD Projects Meeting - R&D
18 August 2022

Fine-Grained I/O and Storage (IOS)

- Work continues on trying to integrate HDF5's MPI based concurrent writing into test framework

- Began investigating how class layout affects storage time/size
  - Looking at most costly data products stored in CMS' AOD format

Portable Parallelization Strategies (PPS)

- Patatrack
  - A frozen, standalone version of CMS heterogeneous pixel track and vertex reconstruction
    - "End-to-end", with mock framework and build system
  - Current status

	Implementations							
	CPU Serial	**CUDA** (original)	**HIP**	**Kokkos**	**Alpaka** (by CERN team)	**std::par**	**SYCL** (also by CERN team)	**OpenMP**
NVIDIA								
AMD				Crashes randomly				
Intel				Does not compile (Eigen)				
CPU				Serial, POSIX threads	Serial, TBB			

Completed
In progress
Not started

Portable Parallelization Strategies (PPS)

- Patatrack: recent updates
  - New effort in `std::par` by a person from Berkeley
    - Good progress
    - Approach is to take full CUDA Unified Memory version, and work it towards standard C++ with NVHPC
  - SYCL
    - Summer students at CERN group working on it as well
- Plans
  - Get access to JLSE at Argonne to be able to test on AMD and Intel GPUs
  - Continue with direct SYCL, OpenMP-Target, and `std::par`

Portable Parallelization Strategies (PPS)

Completed
In progress
Not started

- Propagation-to-r (p2r)
  - Kernel for track propagation in radial direction extracted from mkFit
  - Current status

	Implementations								
	TBB	CUDA	HIP	Kokkos	Alpaka	std::par	SYCL	DPL	OpenACC
NVIDIA									
AMD									
Intel									
CPU									

Portable Parallelization Strategies (PPS)

- Propagation-to-r (p2r): recent updates
  - First SYCL implementation (by Alexei) uses a different memory layout than CUDA/Kokkos/Alpaka versions
  - Working on a 2nd SYCL implementation with AOSOA to be consistent with CUDA/Kokkos/Alpaka versions.
- Plans
  - Measure each backends of all the implementations on JLSE hardware