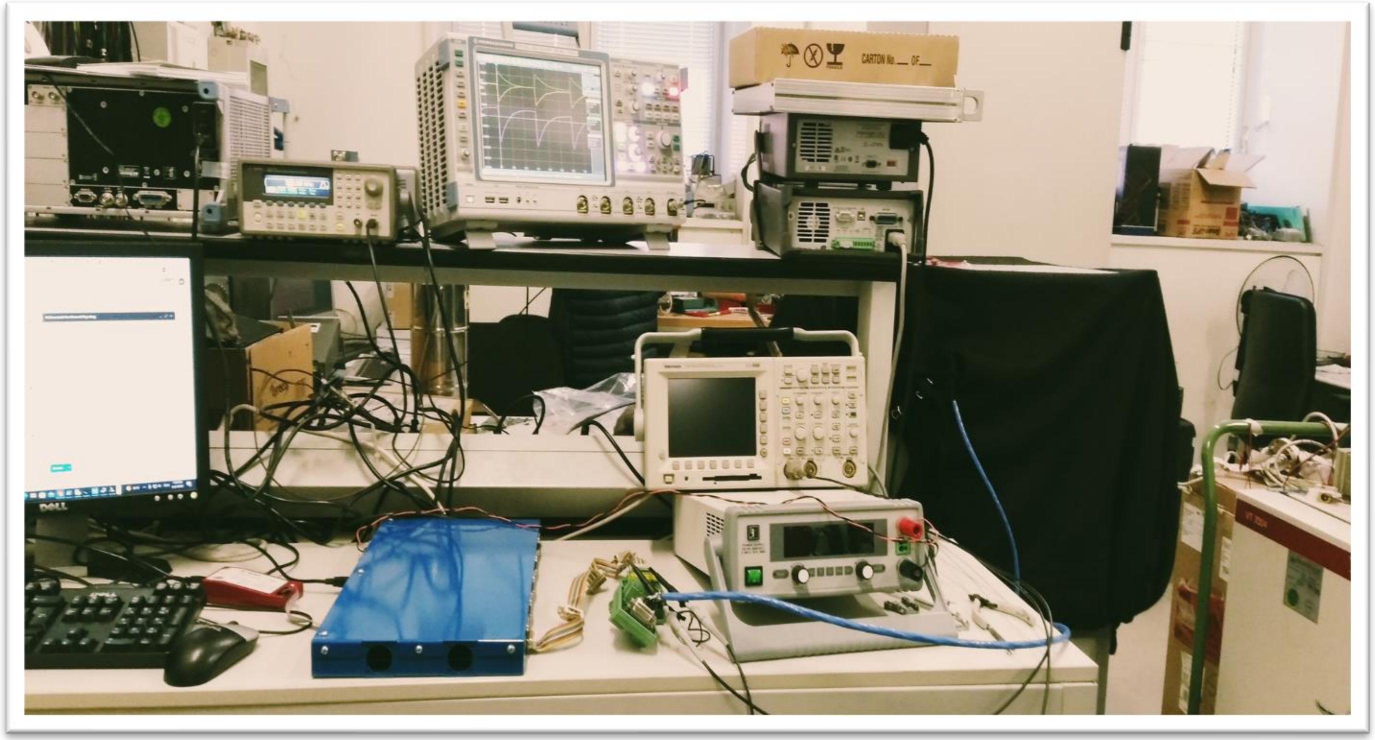
DAPHNE Tests

E. Cristaldo , M. Delgado , C. Gotti , F. Terranova

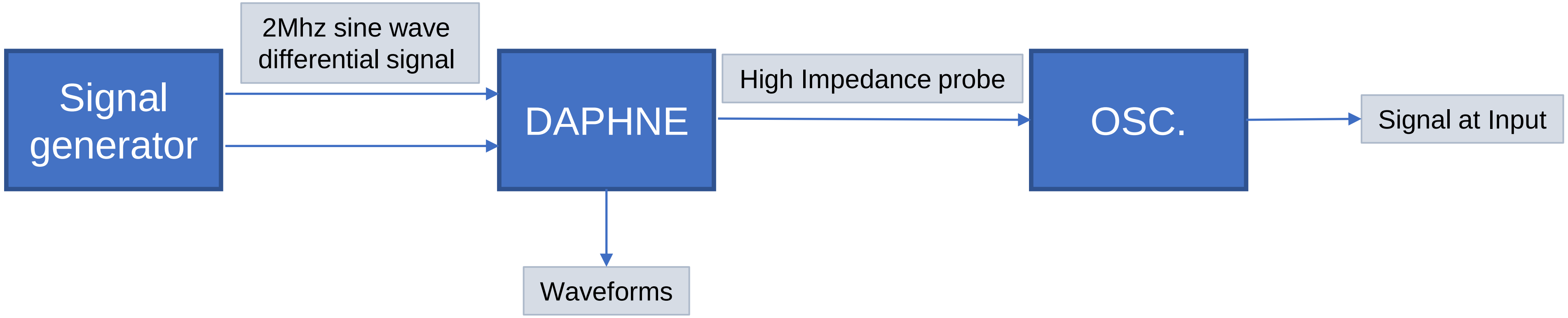
April 4th , 2022

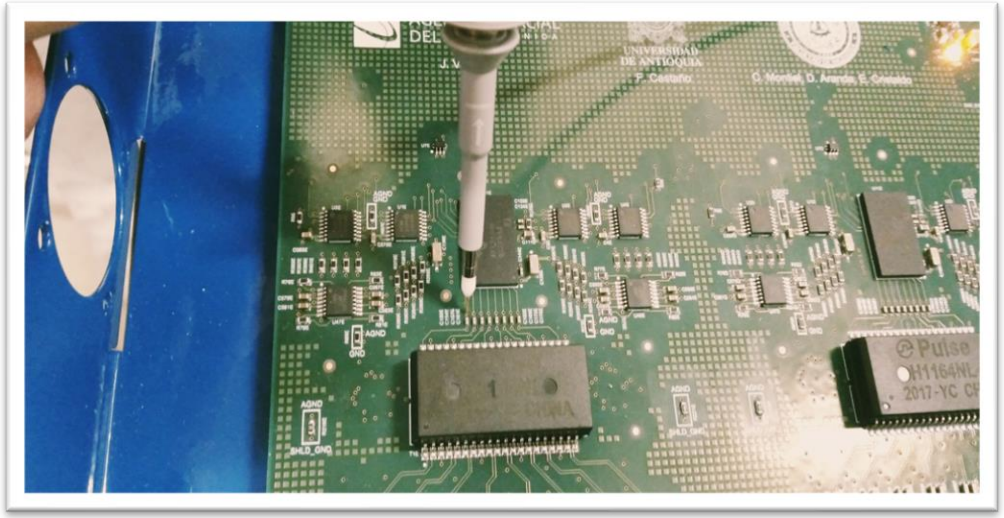
Tests Setup

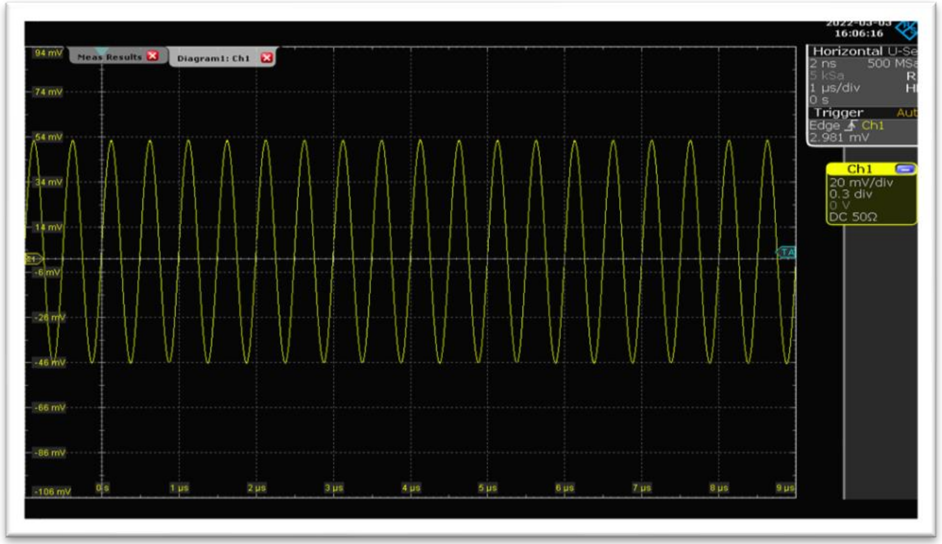
1. Preliminary Gain Tests.
2. Offset Tests.
3. Test at CERN.
4. Next Steps.



Measurement Setup

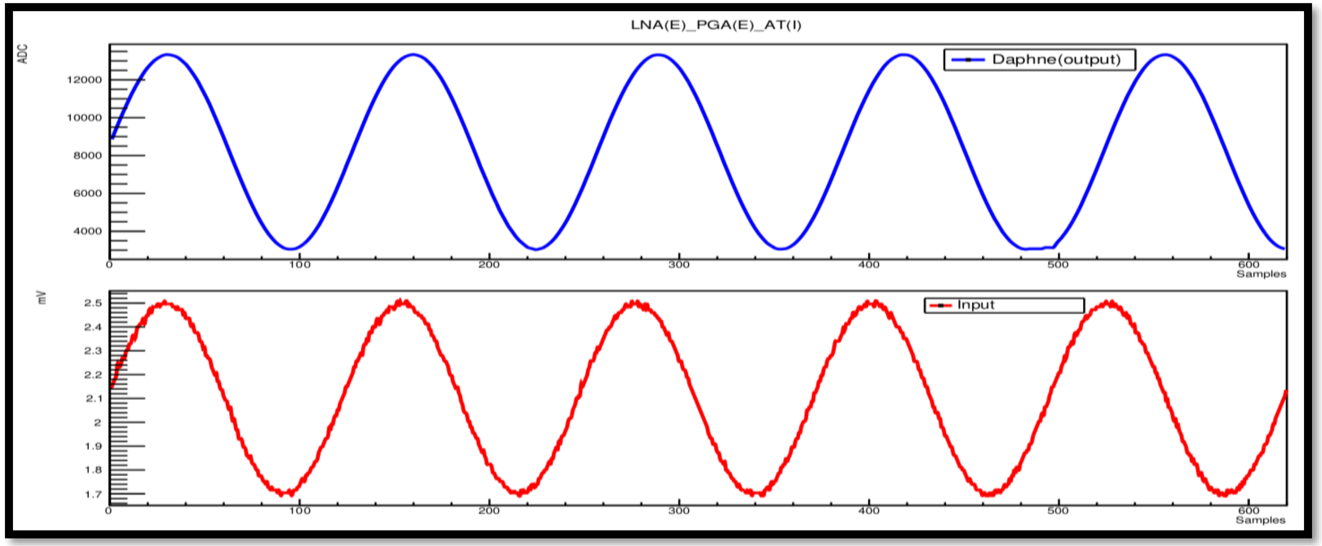


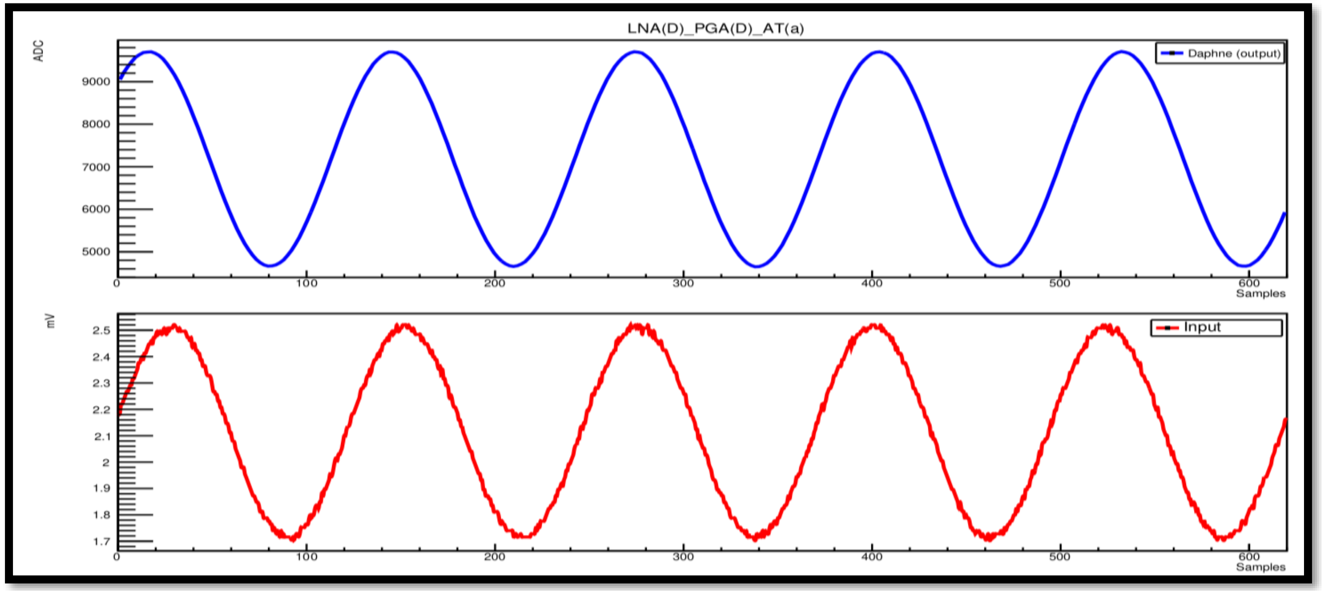




Preliminary Gain Measurements

LNA_I	PGA_I	AT	A(ADC)	Gain
E	E	E	5025	0,76
E	D	E	7704	1,2
D	E	E	5043	0,76
D	D	E	5059	0,77
E	E	D	10308	1,5
E	D	D	15605	2,3
D	E	D	10338	1,6
D	D	D	14990	2,2



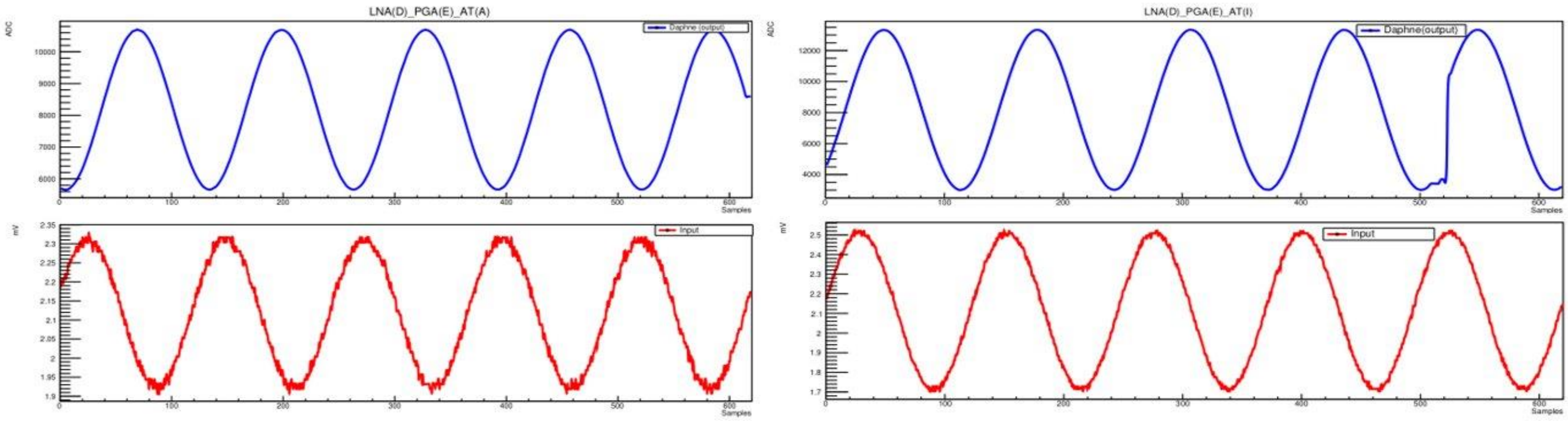


Setup

-VGAIN=1.3 V
-LNA Gain=12 dB
-PGA Gain=30 dB
-LNA Integrator Reg 52[12]
-PGA Integrator Reg 51[4]
-Active termination Reg 52[8]
-Active termination Reg 52[7:6]= 100 Ohm
-Amplitude:400 mVpp differential

UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA INFN Istituto Nazionale di Fisica Nucleare DUNE

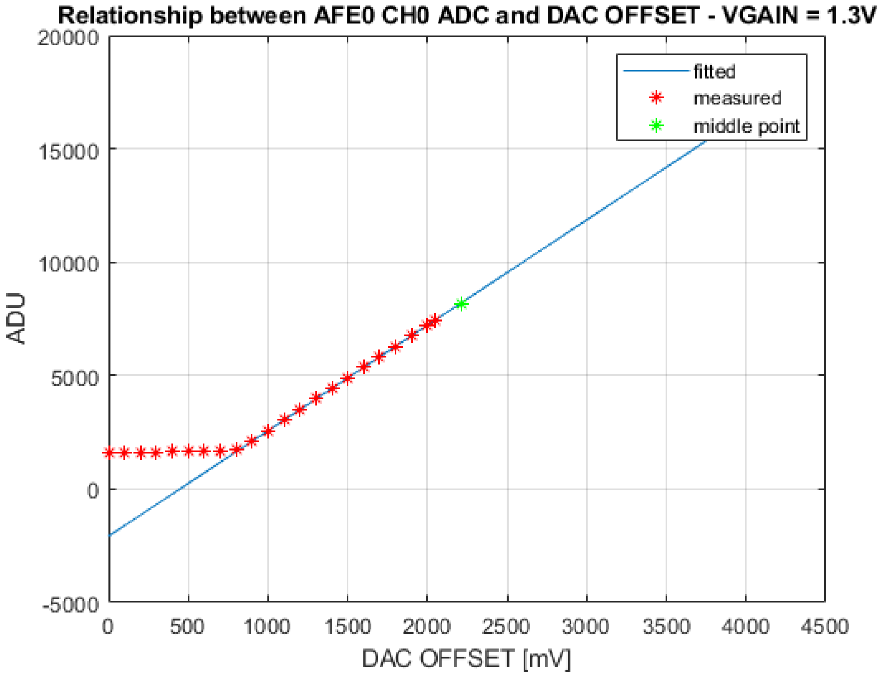
Preliminary Gain Measurements

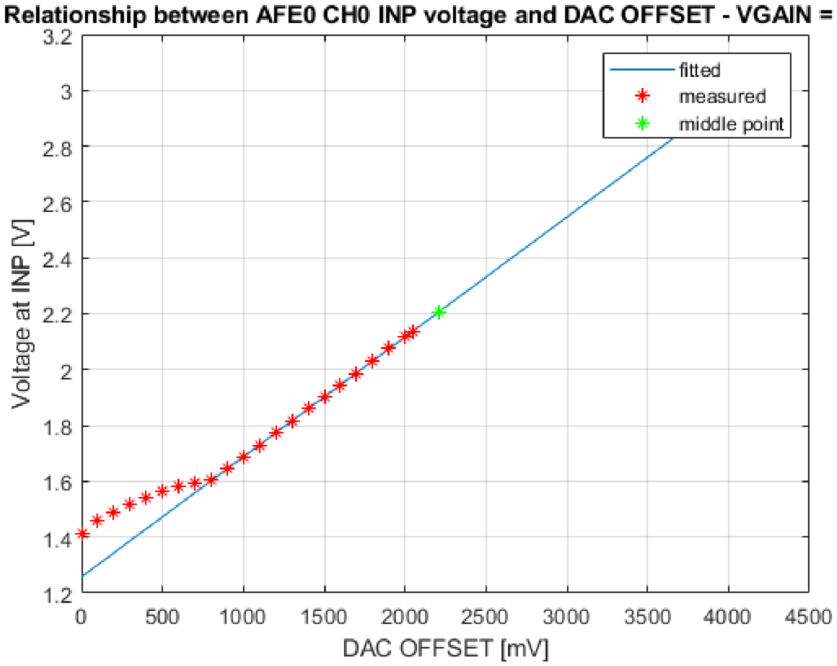


- With this configuration (LNA 12dB, PGA 30 dB) the signal is not clipped (Except when A>14000 or A<3500).
- LNA integrator does not affect the gain, this value is preserved when enabled or disabled.
- PGA integrator affects the amplitude when disabled with the active termination disabled, the amplitude is reduced by 35%.
- With both the integrators disabled there is no loss of gain at OFFSET = 2047.
- When the active termination is disabled, a doubling of the amplitude is obtained.
- With this preliminary test, it is clear that the active termination has to be enabled to obtain the required behaviour and properly match the cold amplifier interface.

OFFSET TESTS

- The offset tests were performed sweeping the DAC OFFSET value with the integrators disabled.
- The DAC OFFSET in mV is the value set by the USER from 0mV to 2047mV.
- The relationships of the sampled ADU and voltage measured at INP (voltage at the input of AFE0 – CH0) can be observed in the graphics below.
- A good linearity is obtained until a point where the value seems to be clipped.

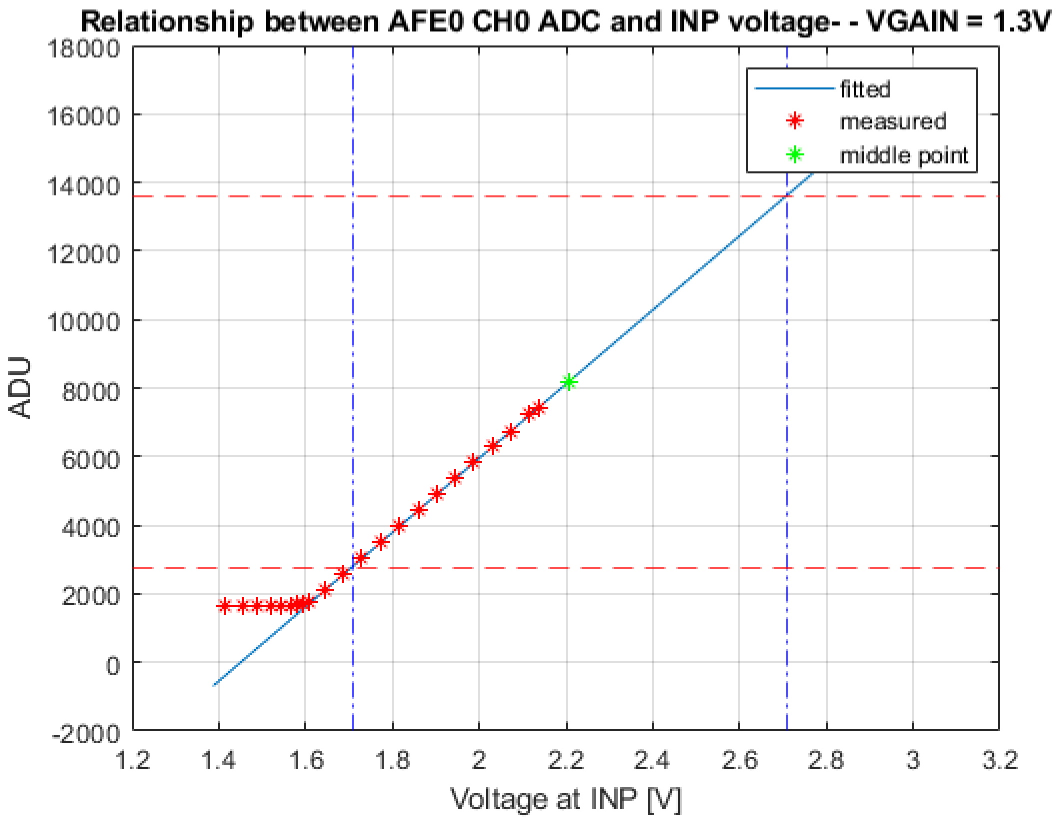




OFFSET TESTS – Linear limits

- Combining the two figures from the previous slide, we obtained the figure below that represents the relationship between the acquired value at a given input voltage.

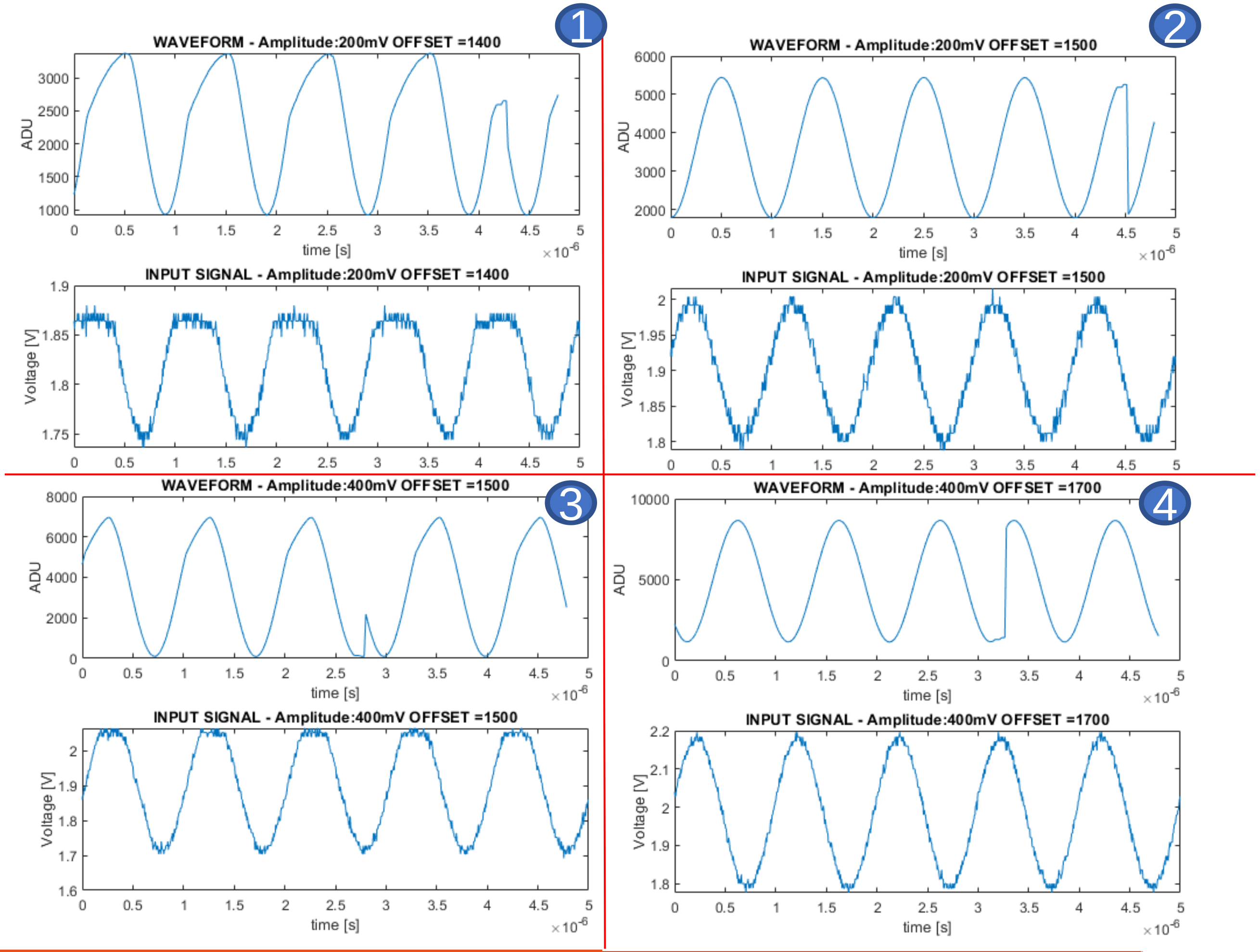
- The limits observed in vertical BLUE lines are the INP values corresponding to the middle point ±0,5V, which determine the expected maximum linear range in this configuration.
- The limits observed in horizontal RED lines are the ADU values corresponding to the intersection of the vertical BLUE lines with the fitted curve, which determine the ADU region where linear behavior is expected.



OFFSET TESTS – Signal response

- The previous figures proves that good linearity can be obtained by the offset circuit.

- We now consider a 2MHz sinusoidal input signal with relative low amplitude to the maximum allowed, to determine the acquired waveform with different OFFSET values.
- Starting from 1, applying 200mVpp with OFFSET 1400mV, we clearly see nonlinearities in the acquired waveform. The input signal is clipped at the positive semi cycle.
- In 2, we increase the OFFSET value to 1500mV, effectively moving the signal pedestal and eliminating the clipping effect in the input.
- In 3 and 4, we increased the amplitude to 400mVpp and observed the reappearing of the clipping effect and the input. This issue is the mitigated again by increasing the OFFSET value.
- From this set of measurements, the dynamic range is clearly limited on both semi cycles, by the clipping effect on top and by the saturation in 0 of the ADC on the bottom.



OFFSET TESTS – Disabling AFE Active Termination

- The clipping issue is related to the CLAMP at the active termination pin ACT.
- As the INP value decreases due to the OFFSET circuit, the inverting output DC value of the LNA increases moving the sinusoidal closer to the CLAMP activation value.
- We then proceeded to disable the Active Termination and place a physical 100Ω between INPUT and GND.

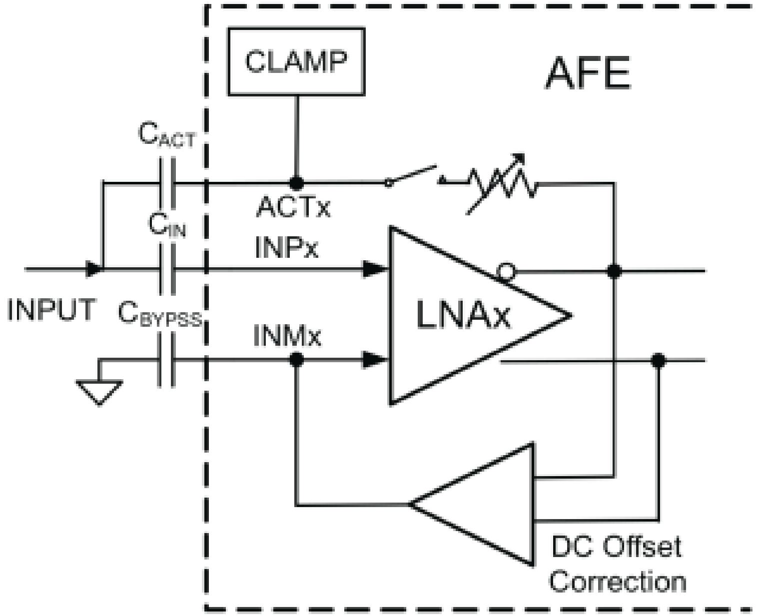


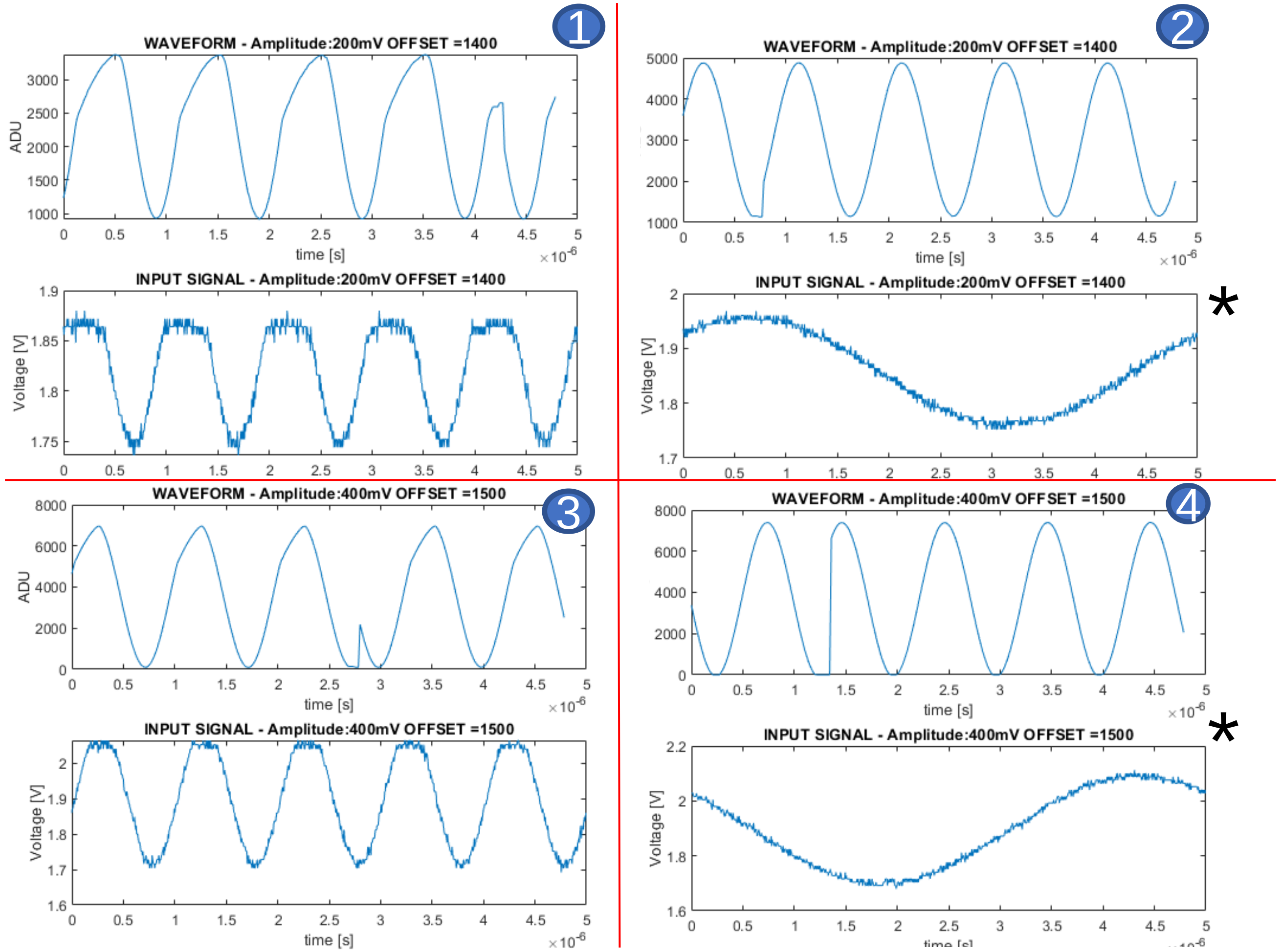
Figure 59. AFE5808A LNA With DC Offset Correction Circuit

OFFSET TESTS – Effect of Active Termination disabling

- With this configuration, the clipping is the positive semi cycle is mitigated allowing the signal to take advantage of the dynamic range.
- In 1 and 2; 3 and 4, we compare the input signal at 200mV and 400mV, respectively, with the same OFFSET value. We see no clipping at the input and good response in the acquire waveform.
- *Apologies, the oscilloscope took less samples that the previous configuration.

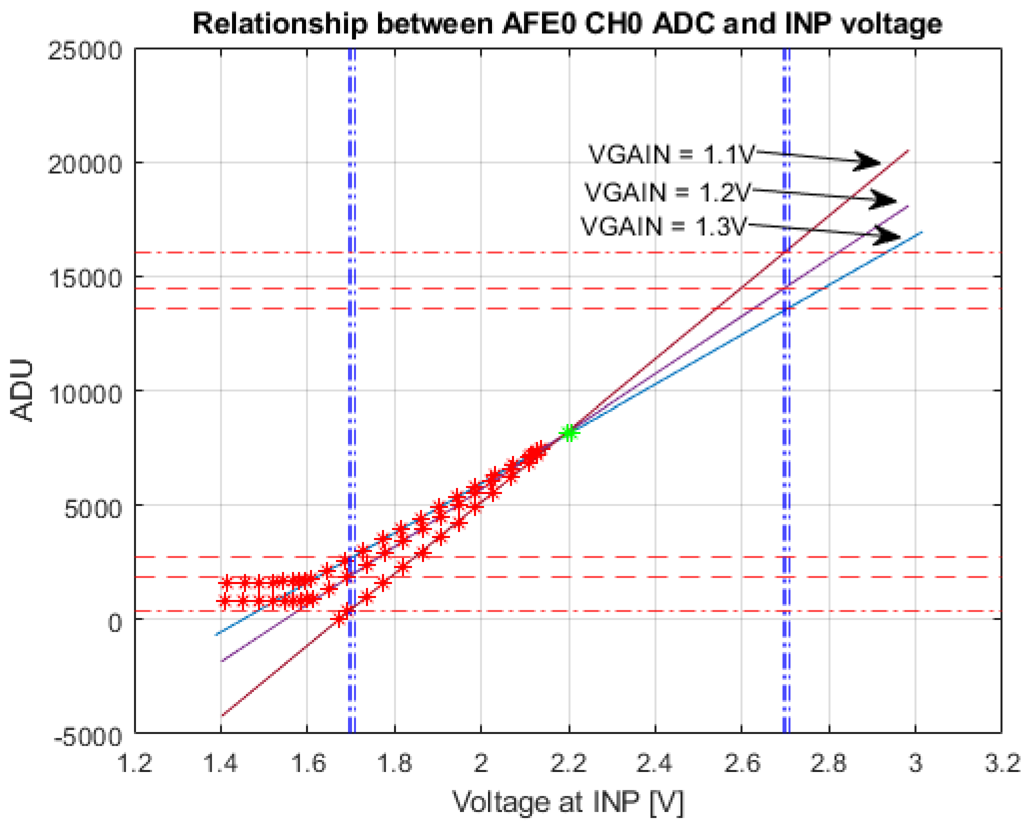
Active termination: Enabled

Active termination: Disabled



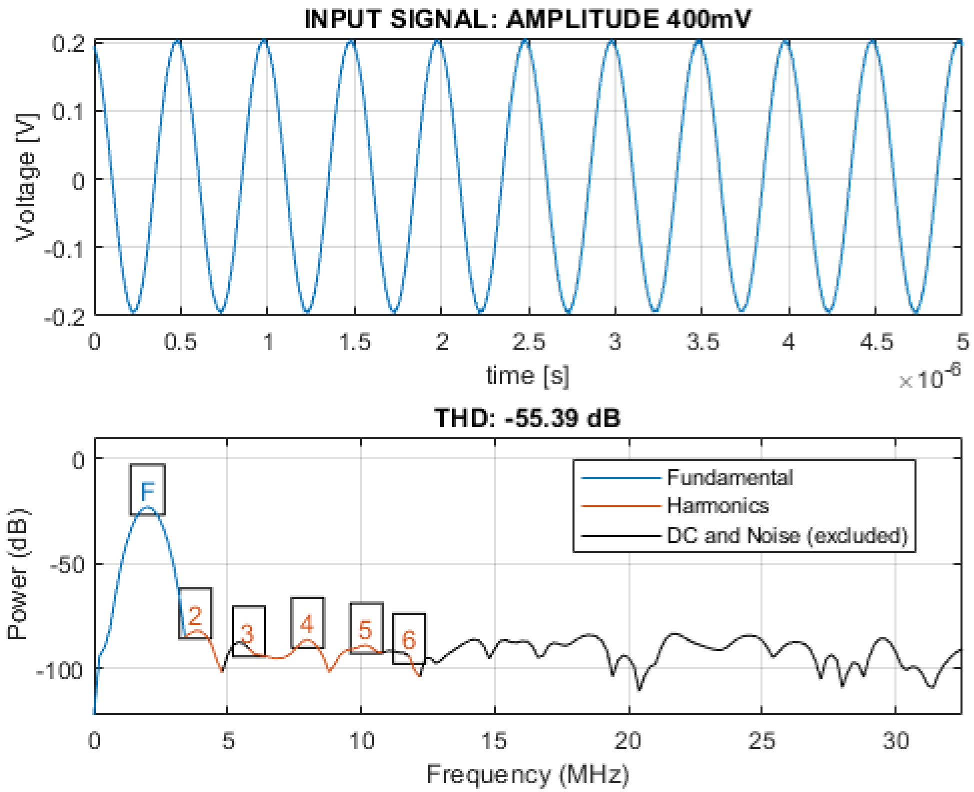
OFFSET TESTS – Configuration selection and linear limits

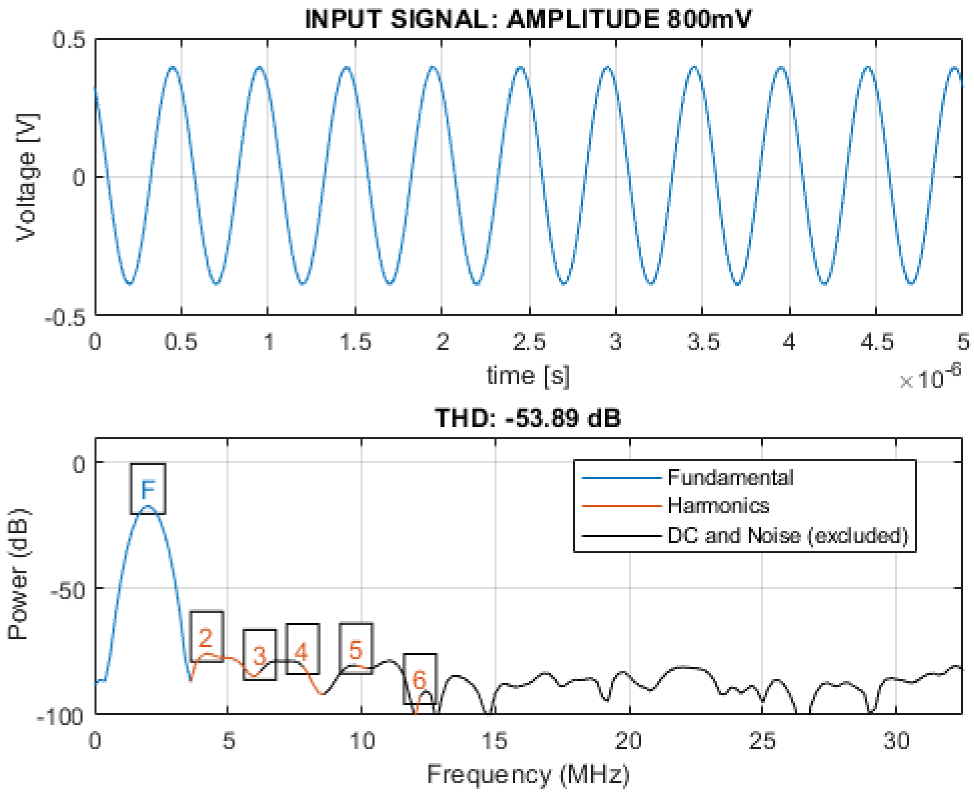
- To determine more clearly the linear response of AFE 0 – CH0, we select two VGAIN values to make tests. VGAIN = 1,2V and VGAIN = 1,1V.
- With these configurations, we sweep the DAC OFFSET value from 0 to 2047 in steps of 10.
- As the input, we select 400mVpp and 800mVpp 2Mhz sinusoidal signals.
- We use the total harmonic distortion (THD) of the signal as a figure of merit.



OFFSET TESTS – Input signal characteristics

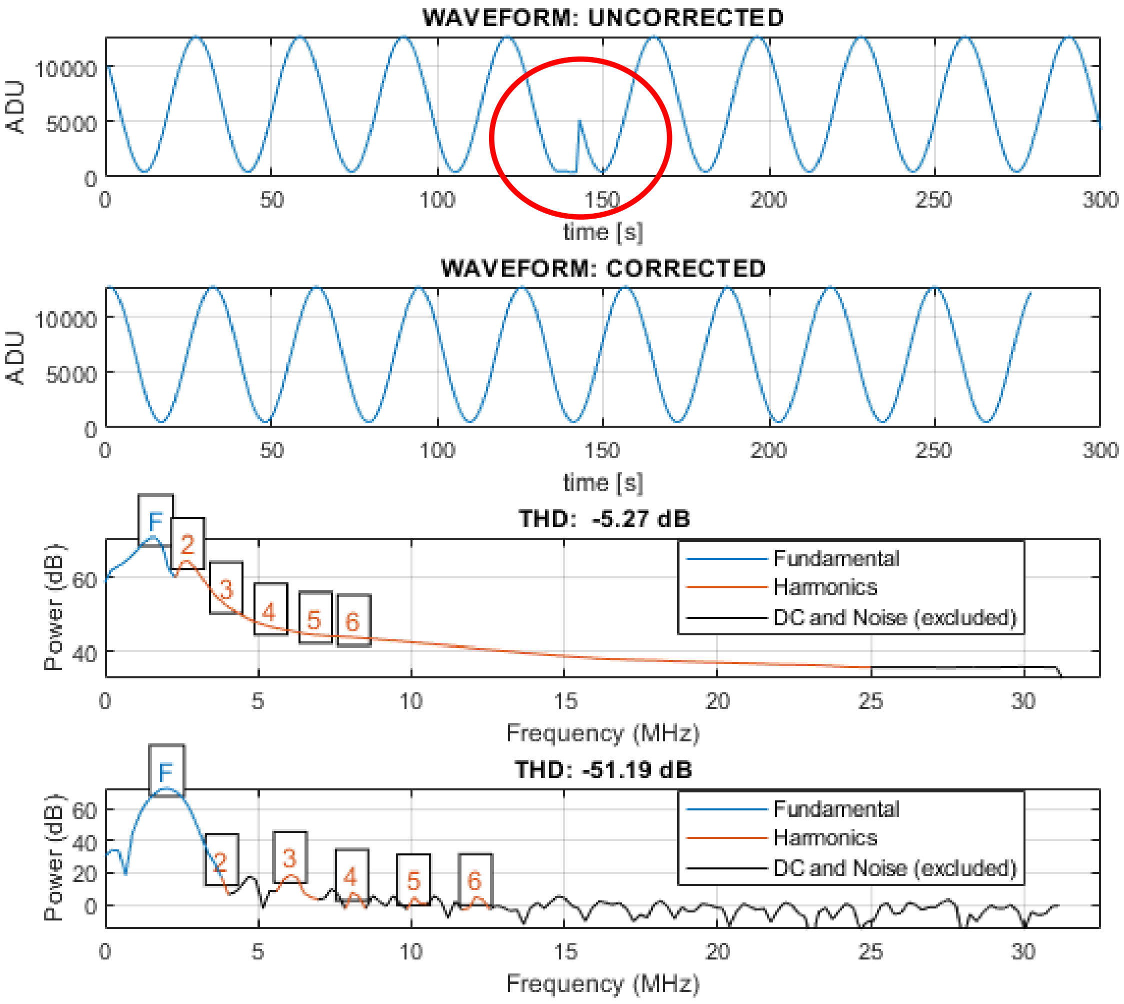
- The figures below show the THD of the input signal measured directly in the oscilloscope with a 50Ω input impedance. The THD values will be used as a comparative reference for the acquired waveforms.





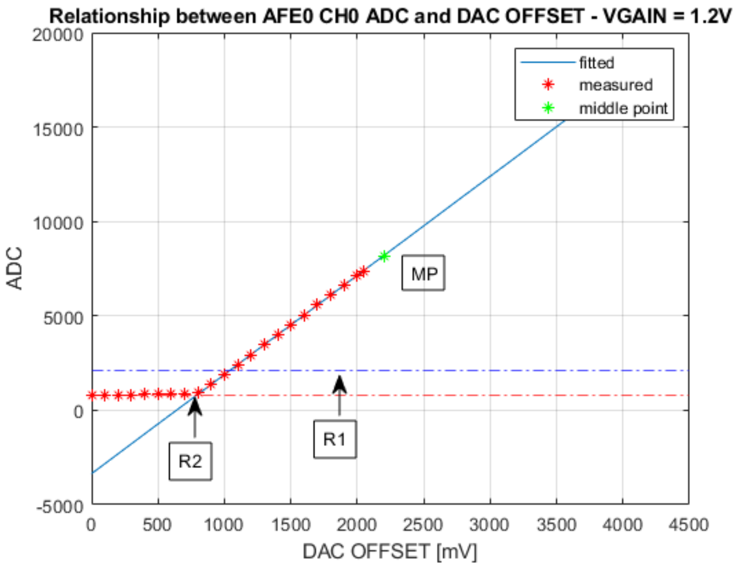
OFFSET TESTS – THD and correction of waveforms

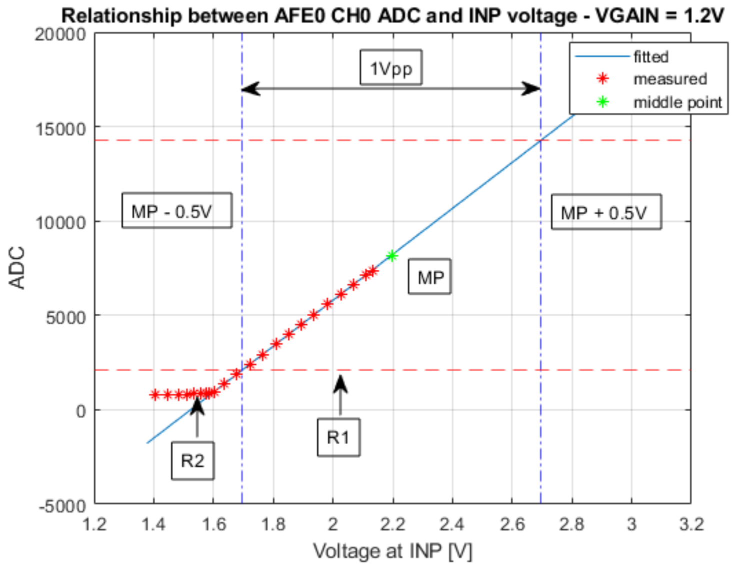
- We have seen a discontinuity effect in the acquired waveforms that we attribute to the AFE buffers.
- When we send RD FPGA, this discontinuity displaces to the right.
- As can be seen in the red circle, the discontinuity greatly affects the result of the THD calculation.
- A correction of this effect was performed by selecting the unaffected cycles and clipping away the discontinuity segment.
- We refer to these as uncorrected and corrected signals.

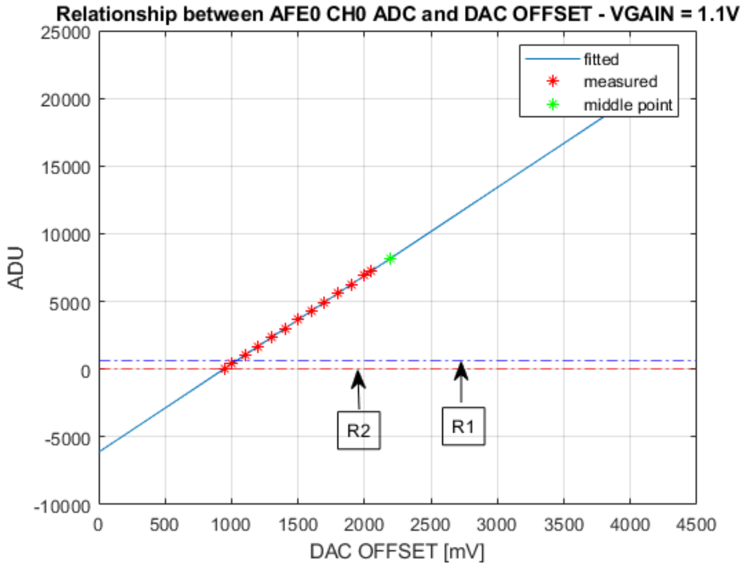


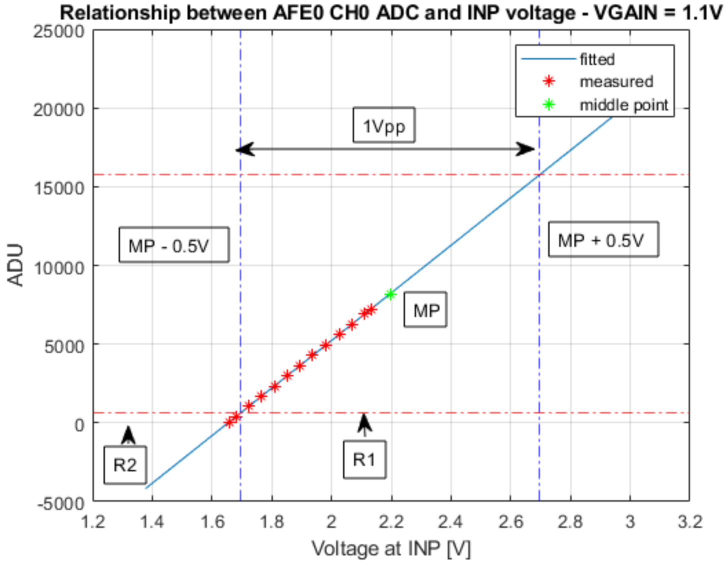
OFFSET TESTS – Linear Limits

- Going back to the relationship figures. We now define the limits R1 and R2.
- R1 is the expected lowest input linear value as specified by the datasheet for this configuration in ADU.
- R2 is the minimum allowed low value in ADU before clipping or ADC saturation.
- In the following slides L1 and L2 will be used a limits references where we expect to see linear behavior.
- $L1 = f(R1 + \frac{Amplitude_{ADU}}{2})$
- $L2 = f(R2 + \frac{Amplitude_{ADU}}{2})$
- $f(\mathrm{x})$ is the fitted function from ADU to offset values



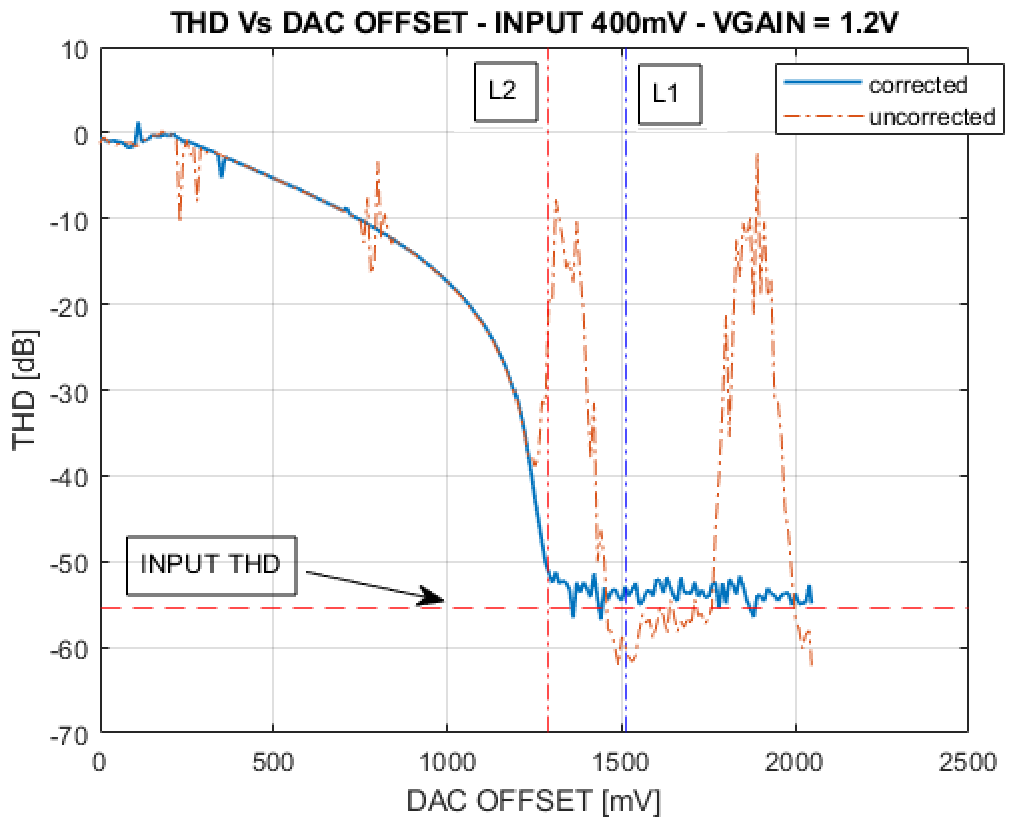


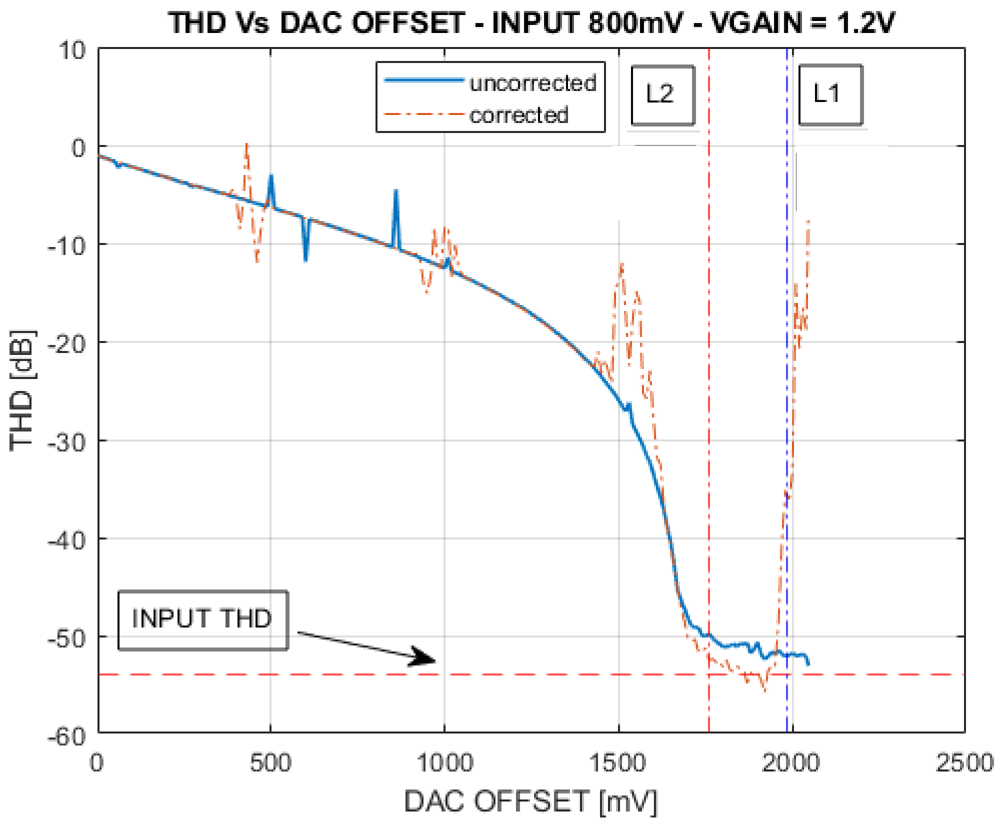




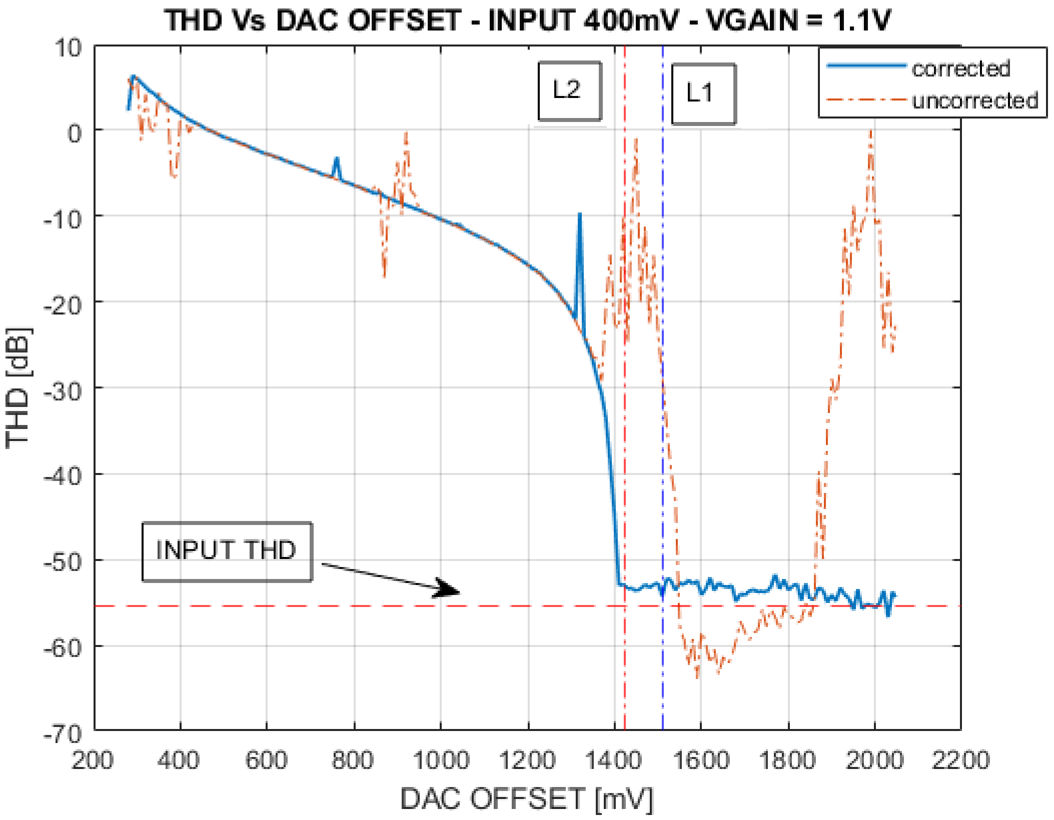
UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA INFN Istituto Nazionale di Fisica Nucleare DUNE

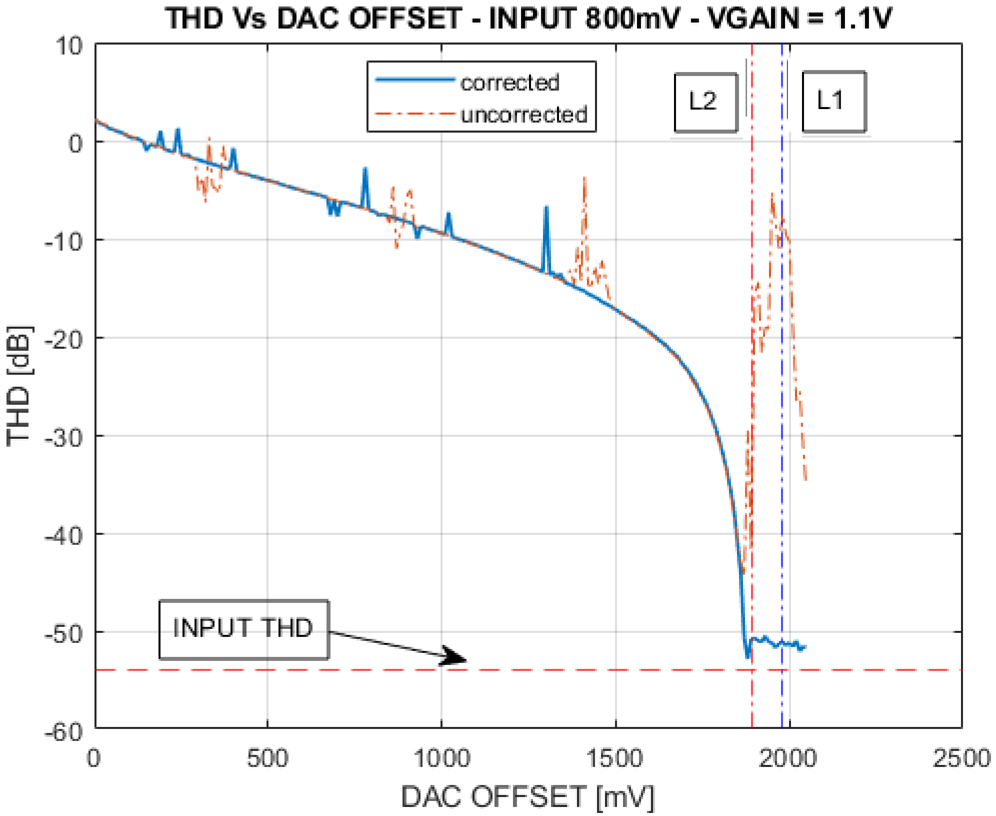
OFFSET TESTS - THD





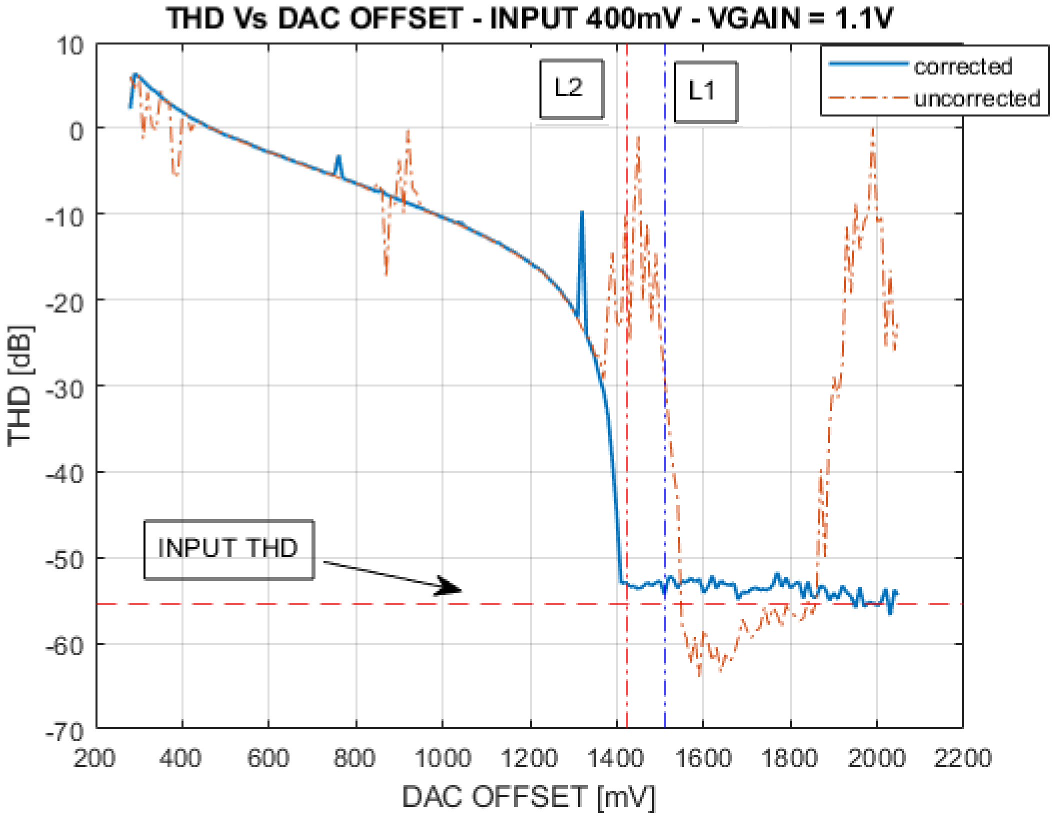
OFFSET TESTS - THD



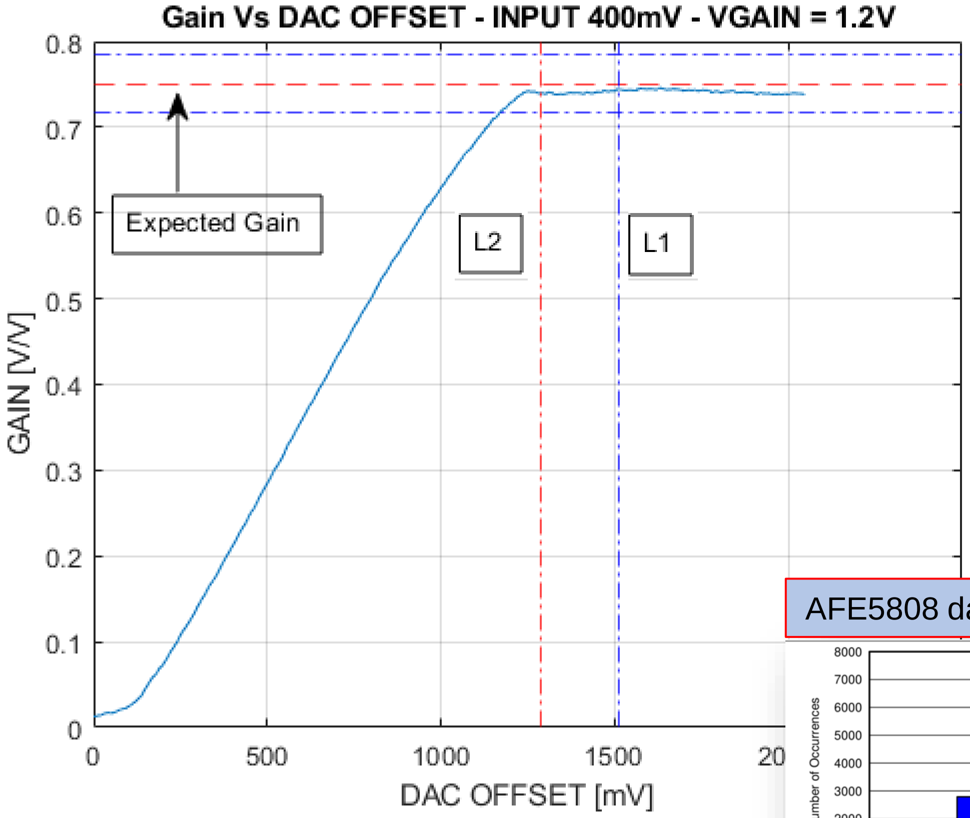


OFFSET TESTS – THD conclusions

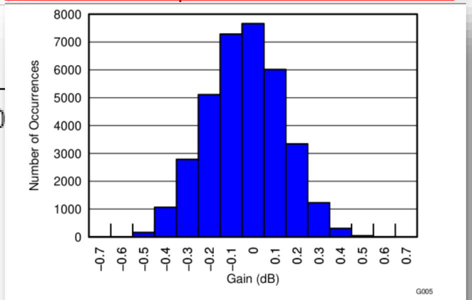
- Some conclusions on the THD:
- The figures presented in the previous 2 slides show that a THD value close to the input reference value was obtained in the range where linear behavior is expected.
- No noticeable difference was found between VGAIN = 1.2V and VGAIN = 1.1V regarding signal distortion.
- Therefore, the DAC OFFSET circuit does not have an appreciable negative impact on signal distortion.



OFFSET TESTS - GAIN

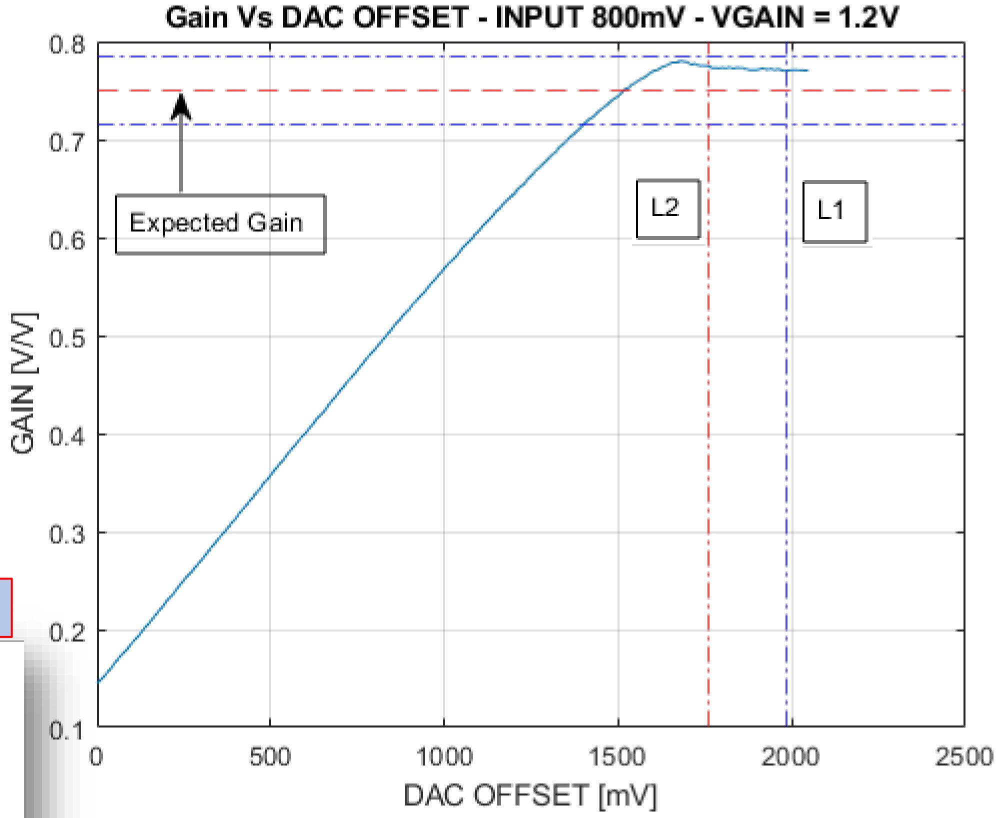


AFE5808 datasheet page 19

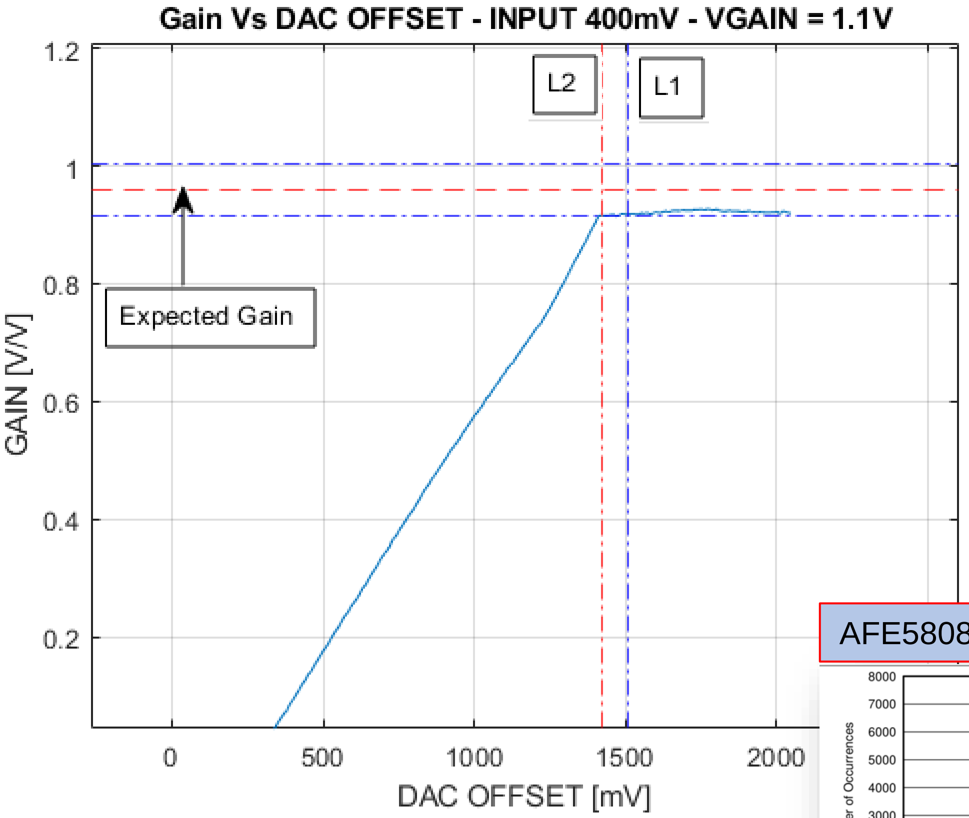


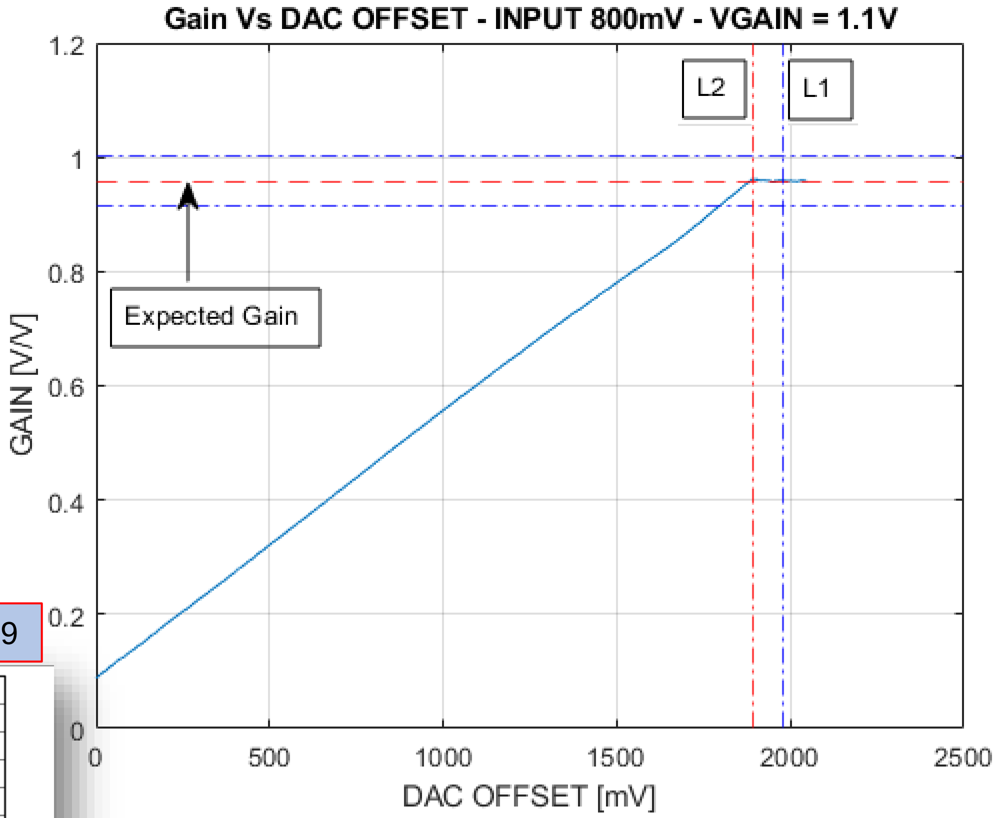
VCNTL = 0.9 V (34951 channels)

Figure 6. Gain Matching Histogram

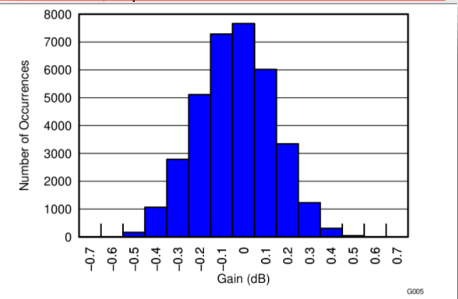


OFFSET TESTS - GAIN





AFE5808 datasheet page 19

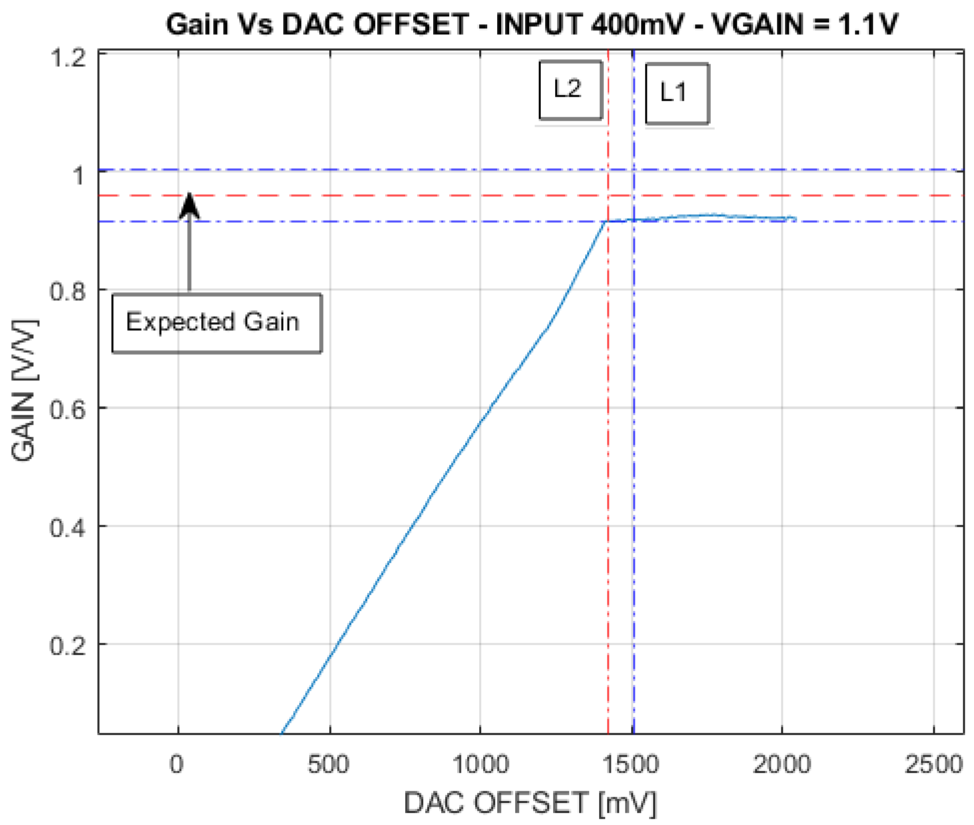


VCNTL = 0.9 V (34951 channels)

Figure 6. Gain Matching Histogram

OFFSET TESTS – Gain conclusions

- Some conclusions on the gain values:
- The figures presented in the previous 2 slides show that a GAIN value remain almost constant and within the expected value.
- No noticeable difference was found between VGAIN = 1.2V and VGAIN = 1.1V regarding GAIN of the signal.
- Therefore, the DAC OFFSET circuit does not have an appreciable negative impact on the GAIN of the signal.



DAPHNE TEST AT CERN

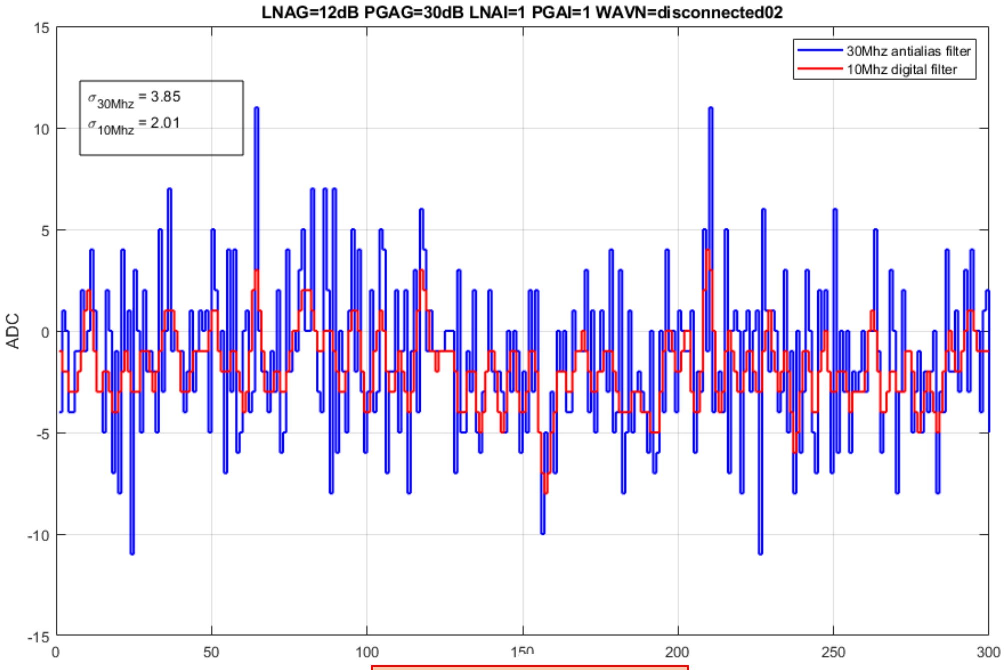
- Test were performed on March 14th and 15th
- Daphne was taken to CERN to test the integration with the Vertical Drift cold electronics receiver.
- Electrical integration was a relative success. We were able to connect and acquire signals with DAPHNE with no hardware modifications.
- Due to the lack of triggering capability, the data analysis is limited to waveform inspection.

DAPHNE TEST AT CERN – NOISE

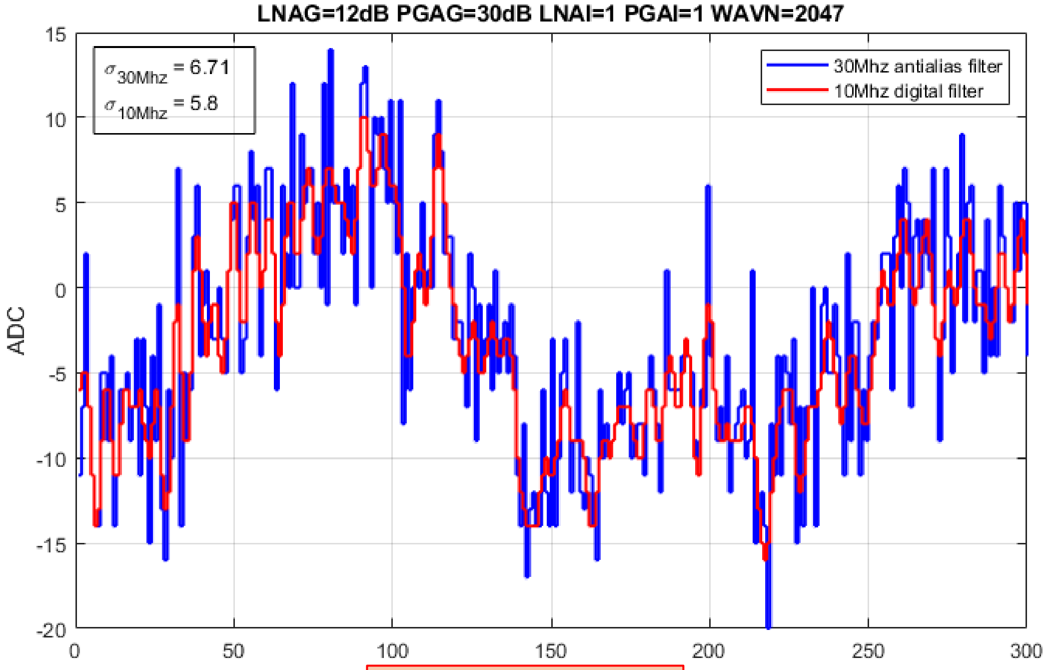
- The figure below represent the acquired waveforms with the system connected and disconnected form the receiver. Noise figures are show with 30Mhz AFE LPF and 10Mhz post-processing digital LPF.

Disconnected

Connected



$\sigma_{30Mhz} = 3,85$
$\sigma_{10Mhz} = 2,01$

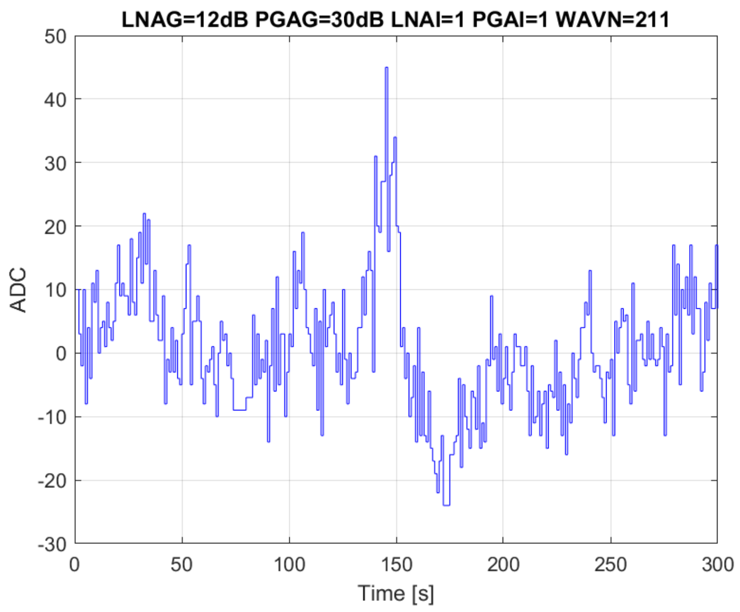


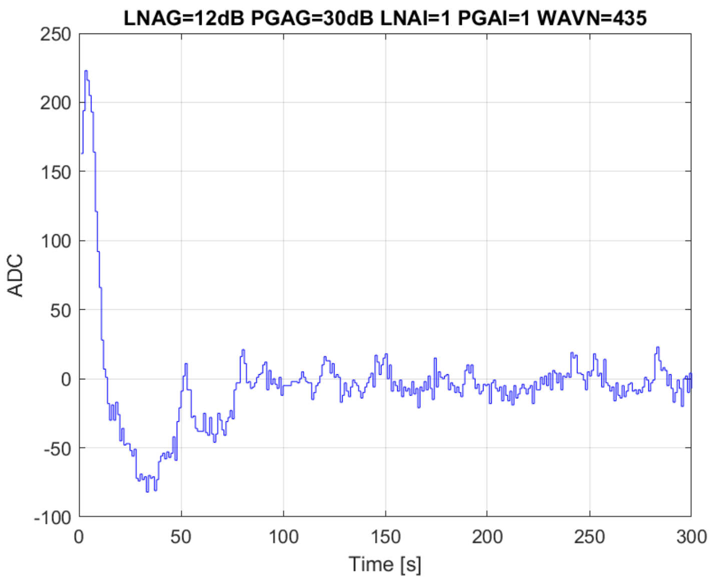
$\sigma_{30Mhz} = 6,71$
$\sigma_{10Mhz} = 5,8$

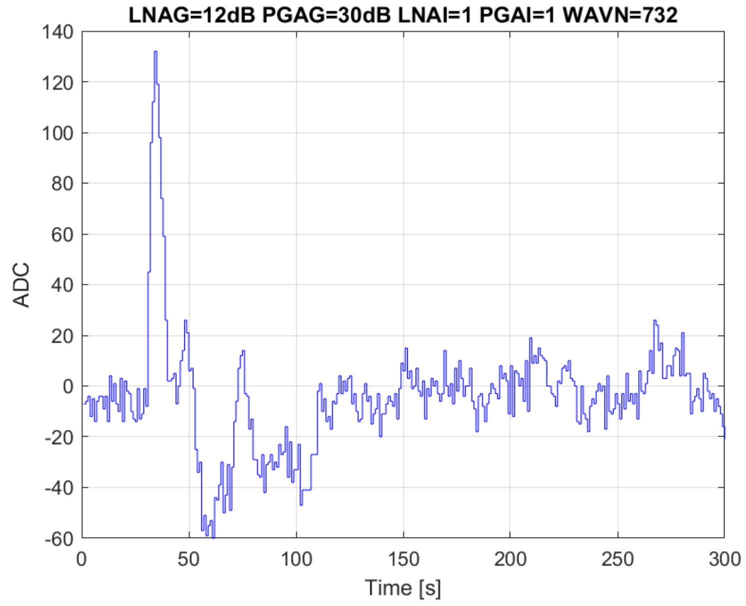
UNIVERSITÀ DEGLI STUDI DI MILANO BICOCCA INFN Istituto Nazionale di Fisica Nucleare DUNE

DAPHNE TEST AT CERN – Acquired Waveforms

- With the Vertical Drift systems on, DAPHNE was left acquiring waveforms for a period of 30 minutes. Over 2000 waveforms were acquired where it can be observed multi-photoelectrons hits.
- Single P.E. is around 3mV; the dynamic range is limited.

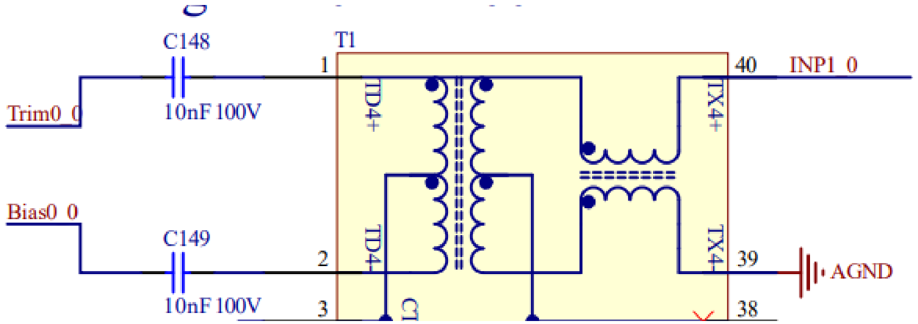


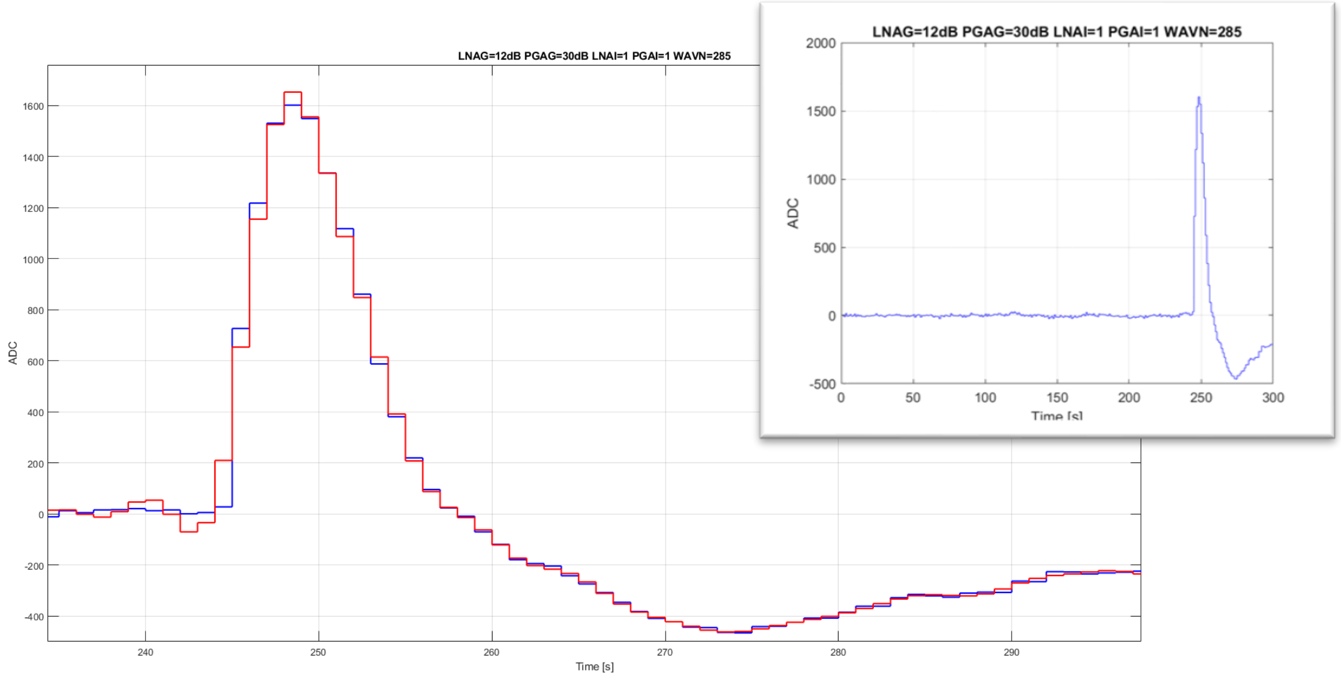




DAPHNE TEST AT CERN – Acquired Waveforms

- This figure shows a large event where signal characteristics is appreciated.
- One of the very first things we and our colleagues noticed is the significant undershoot of the signal. This large effect is probably caused by the 10nF decoupling capacitor at the input.

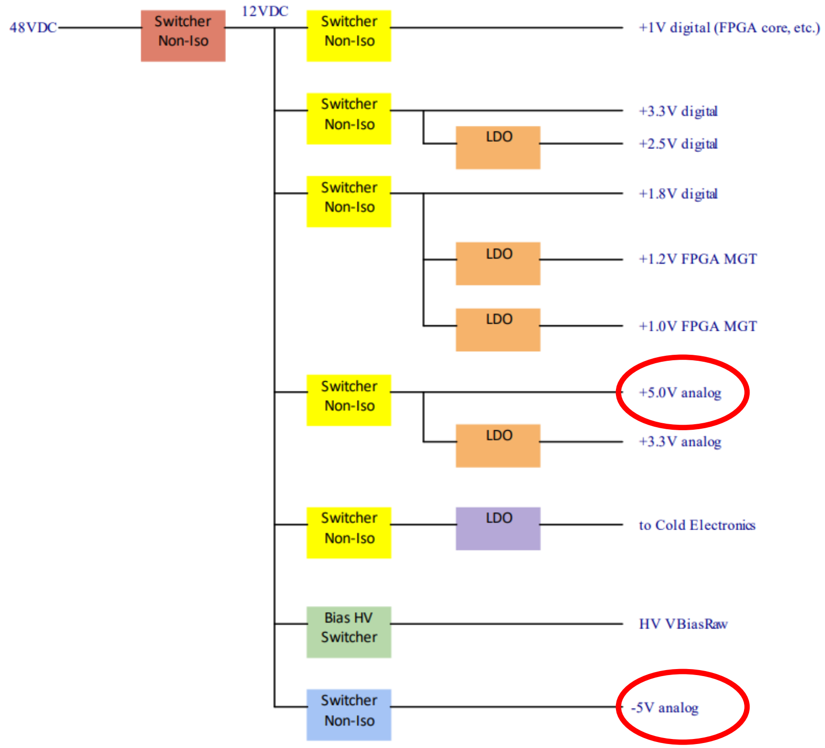


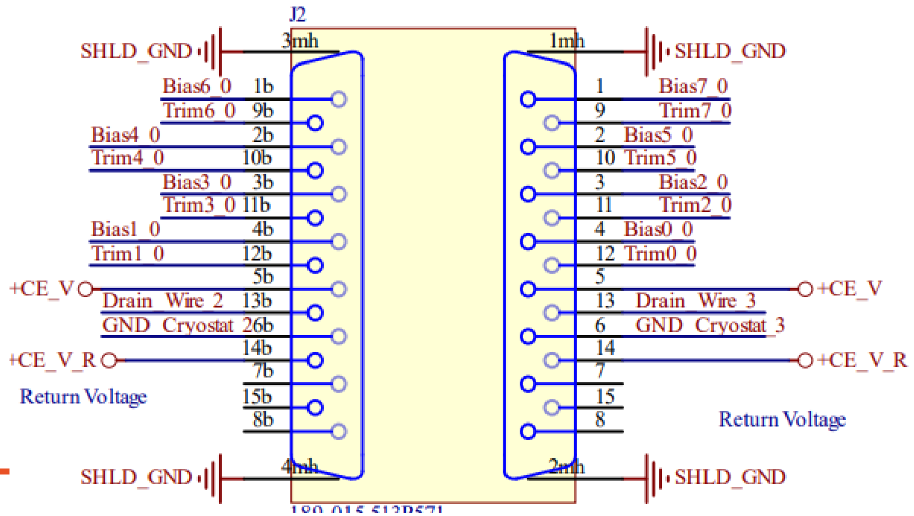


- Our colleagues have asked to bypass entirely the BALUN, given that their signal is single ended. This can be easily achieved just by removing the component.

DAPHNE TEST AT CERN – Power Distribution

- One of the requirements of our colleagues is the ability to power their receiver through DAPHNE's DB15 connector pins.
- Currently the vertical drift receiver is using Koheron PD100 receiver based in the TI OPA847 which require a supply of ±5V @18mA.
- DAPHNE cannot provide these voltages natively through the DB15.
- A work around could be to used the analog voltages and making a bridge to the unused pins 7,15,8 or 7b,15b,8b.
- This workaround must take into consideration the power limitations of the regulators.





DAPHNE TEST AT CERN – Conclusions

- Noise figures seems to be higher than allowed, but this was also observed when the receiver was connected to the oscilloscope.
- An excessive undershoot is observed in the acquired waveforms, this can be mitigated by replacing the 10nF capacitor at the input or by bypassing entirely the BALUN stage, since the receiver signal is already single ended.
- Power delivery to the receiver is possible with some hardware modifications, which require to bridge the supply voltages to the unused pins in the DB15 connector. This modifications depends on the actual current burden of the regulators. This limitation must be determined to know the number of receiver channels DAPHNE can deliver current to.

NEXT STEPS

- Upgrade DAPHNE triggering and data acquisition capabilities:
  - Test the new FPGA firmware that enables trigger and fast ethernet connection.
  - Update the data acquisition software to add compatibility with the ethernet interface.

- Perform Cold Amplifier measurements:
  - Signal integrity (undershoot)
  - Signal-to-noise Ratio.
- Give return to our Vertical Drift colleagues about the compatibility of DAPHNE and the required modification, if needed.