REPORT ON DAPHNE

Integration and Analog studies

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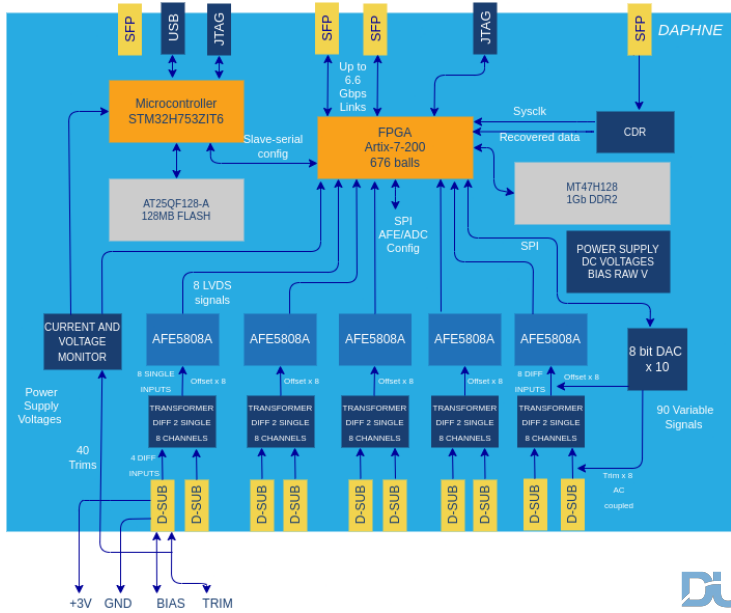
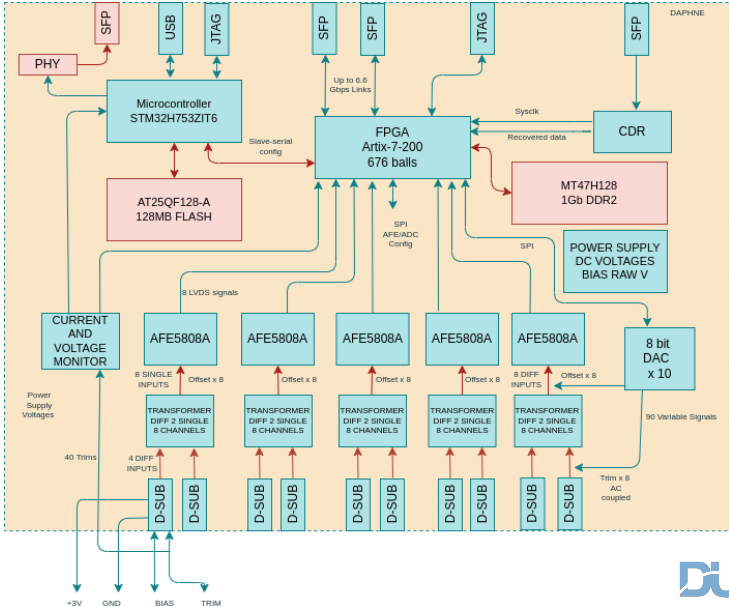
Introduction

- We present an updated status using the hardware and software diagrams
- Results on analog tests on different labs is presented
- Activities related with plans for integration

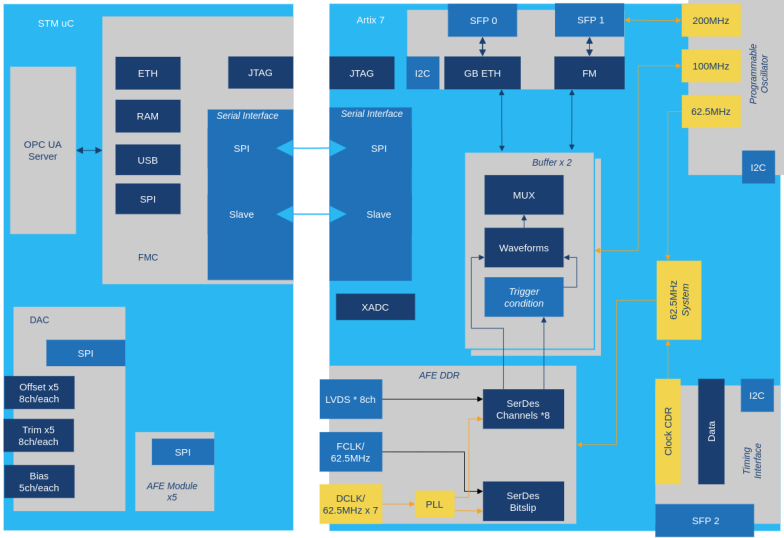
Hardware Scheme



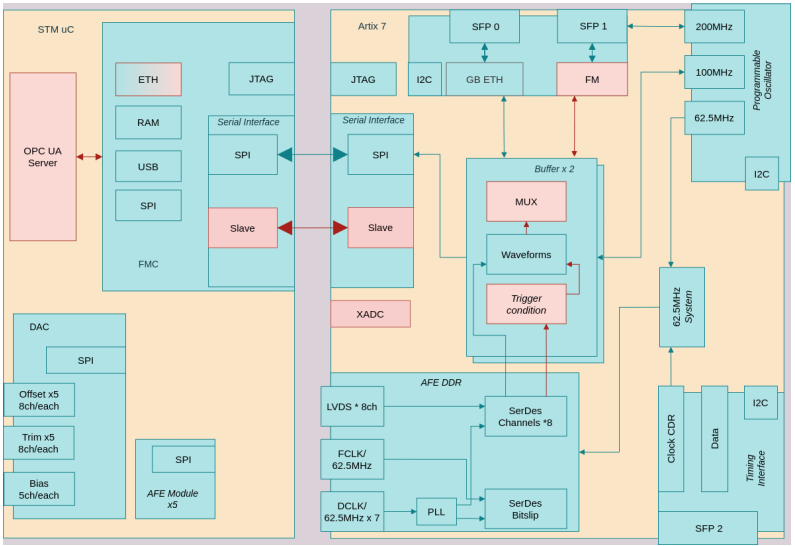
Hardware Scheme Status



Firmware Scheme



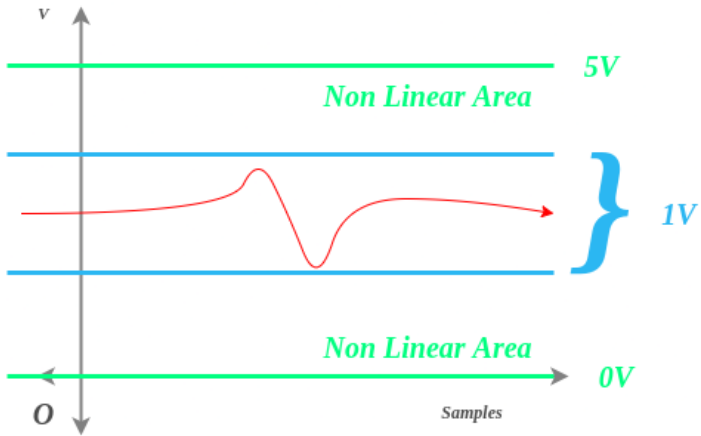
Firmware Scheme Status



Data Acquisition AFE Characterization

Firmware:

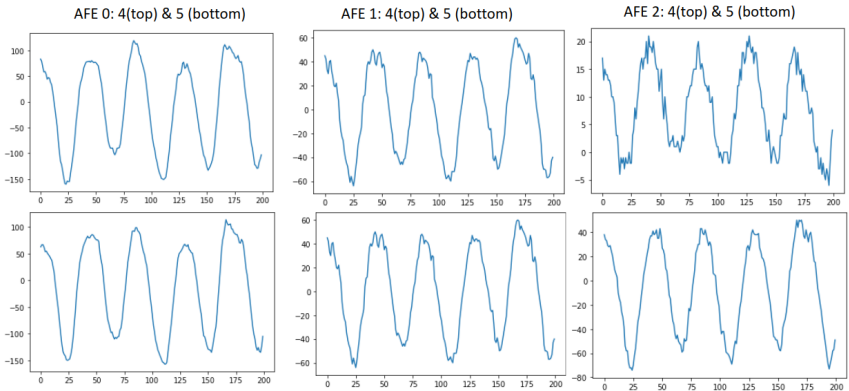
- 1 Channel Version
  Almost Streaming
  self alignment by
  hardware
- 40 Channel Version
  SPY Buffers
  manual alignment
- AFE Configuration
  No integrator
  Active Termination



Data Acquisition AFE Characterization

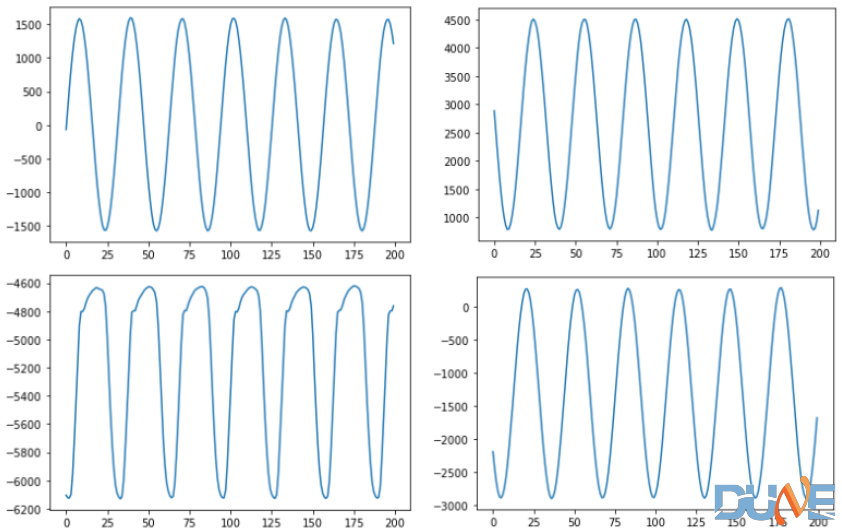
Hardware:

- AFE 0
  Offset Disabled
  Transformer rm
- AFE 1
  Offset Disabled
- AFE 2
  Offset DAC
  Referenced 4.096



Data Acquisition AFE Characterization: Offset

- Using Active termination enhances the Signal
- We have control on the pedestal of the signal
- Issue: We are getting different pedestal for different boards



Data Acquisition AFE Characterization

Crosstalk:
less than .02%

AFE 1

Input (mV)	Output p-p	neighbor RMS	Inferred crosstalk	Inferred crosstalk (%)
10	210	1.87		
100	1175	1.81		
500	5527	2		
1000	10871	2.3	1.34	1.2E-04
1225	13282	2.6	1.81	1.4E-04
1450	15691	2.8	2.08	1.3E-04

AFE 2

Input (mV)	Output p-p	neighbor RMS	Inferred crosstalk	Inferred crosstalk (%)
10	253	1.85		
100	1156	1.85		
500	5494	1.98		
1000	10785	2.37	1.48	1.4E-04
1225	12972	2.6	1.83	1.4E-04
1450	15499	2.83	2.14	1.4E-04

Development Activities on the coming weeks: uC

Serial Port

- enhance responsiveness on commands
- support for different terminals (pyserial), for automation

Slave Serial

- Write and Read from Flash Memory
- Program FPGA over slave serial using actual bitstreams.
- DMA related enhancement

Development Activities on the coming weeks: uC

Slow Control

- PHY TX RX pins are Swapped. Plan to correct those on multiple boards.
- PHY Firmware Development.
- OPCUA 62541 on STM uC
- OPCUA Server on Raspberry Pi as a second plan for Slow Control.
- Prepare documentation on the monitoring variables for Slow Control.

Development Activities on the coming weeks: FPGA

Readout

- Enhance 40Ch lecture of AFEs over ETH. Autamatic.
- IPCore for 14 - 32 bit format and data type for DAQ.
- Test external trigger on different boards.
- Test ETH on Italy
- Analog Characterization using cold amplifiers.

FullMode

- Demonstrate 40Ch lecture over FullMode Using DAPHNE hardware.
- Test single and dual output


DEEP UNDERGROUND
NEUTRINO EXPERIMENT