Cold Digital Readout Status and Component Qualification

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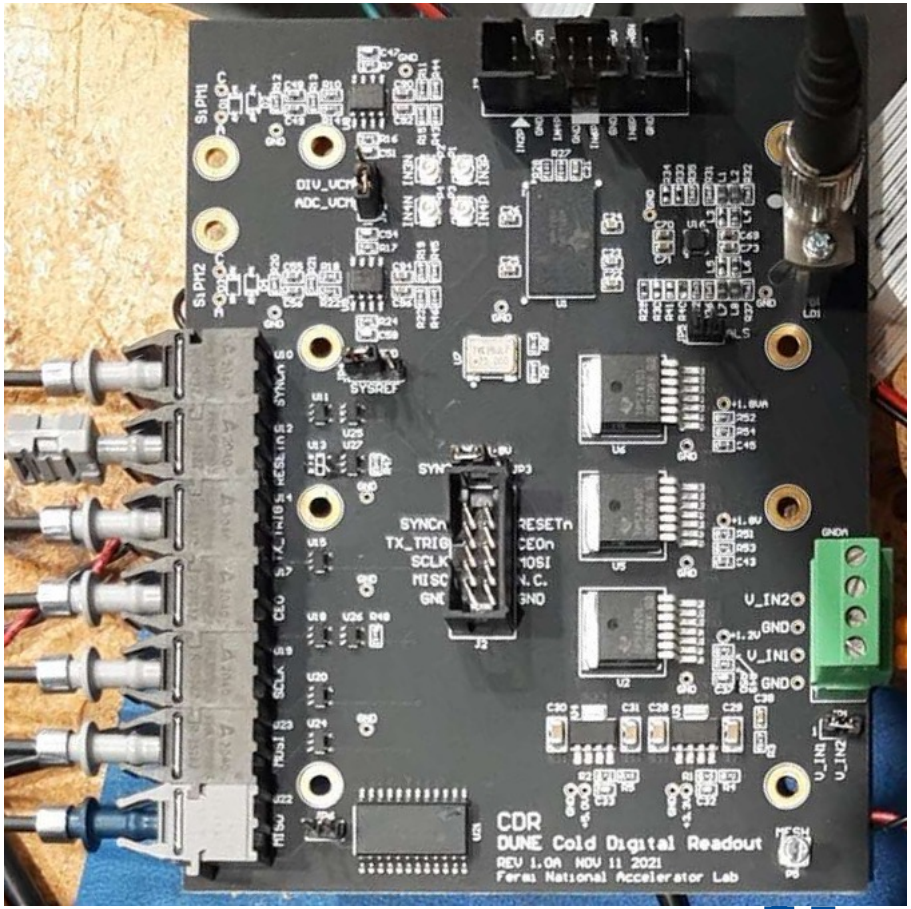
Cold Digital Readout Concept

Objective: Low part-count digital ADC solution compatible with cryogenic operation.

Cold Digital Readout Operation

1. **A single low-power ADC clocked by a free-running oscillator continuously digitizes multiple input-channels.**
2. **The samples are transmitted over a single optical fiber using the deterministic-latency JESD204B subclass 2 protocol.**
3. **An FPGA in the warm recovers the transmission/sampling clock and decodes the samples for multiple digitizers.**



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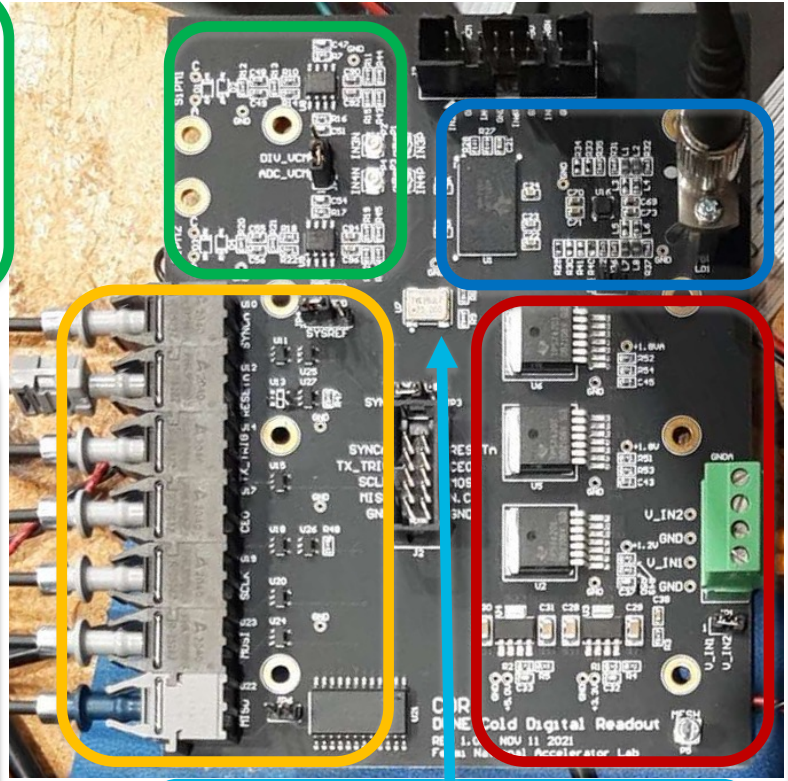
Analog front-end

X10 gain, copied from analog design
Could use multiple gains.

Control and timing

LED-based signaling over plastic optical fiber, stable at DC levels and multiple MHz in liquid argon.



75MHz free-running crystal oscillator with CMOS output.

ADC and Laser Driver

Unique to this design (laser diode shared with analog design)

Power

Linear regulators chosen from existing cryo designs.
5V (Analog front end and controls)
3.3V Laser driver and Oscillator
1.8V digital and analog for ADC

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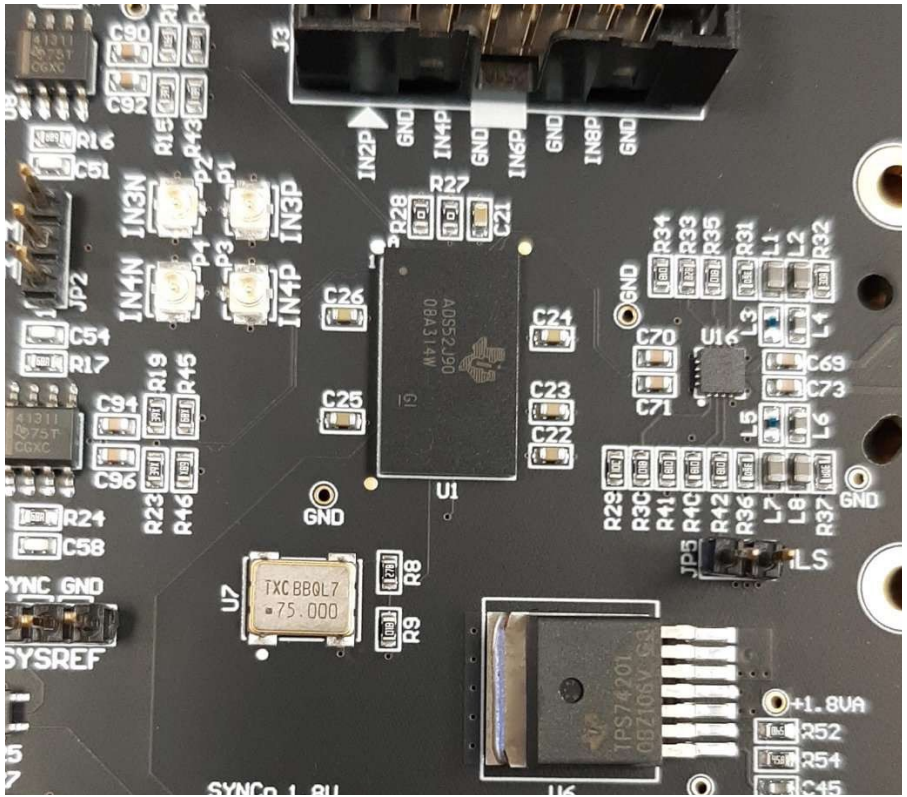
Unique Critical Components

- **ADC: TI ADS52J90**
  - 14-bit 16-channel ADC with 5Gbps JESD204B serial output
  - Chosen from experience with cold operation in LBNL-Fermilab CryoDAQ targeting Liquid He operation.
  - Supports up to 32 differential input channels (configurable)
- **Laser Driver: ADI ADN2526 11-Gbps laser driver**
  - Bias currents set with passive resistors, needs no further configuration
  - Stable operation at both lab and cryogenic temperatures without reconfiguration.



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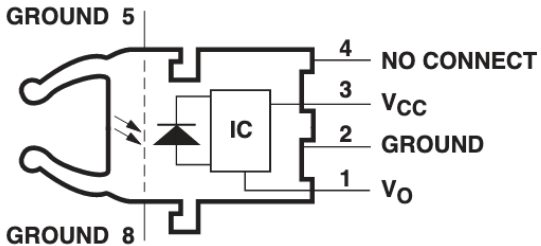
Other Unique Components

- **Oscillator: TXC 7W-75.000MBB-T**
  - Free-running oscillator chosen from parts known to work in liquid Helium.
  - Other parts have been tested
- **POF 650nm receiver: Broadcom HFBR-2528Z**
  - TTL/CMOS compatible push-pull output stage.
  - Tested working at Liquid Argon/Nitrogen temperatures.
  - Wavelength could be seen by SiPMs
- **POF 650nm transmitter: Broadcom AFBR-1521CZ**
  - Just a LED in a case.
  - Not needed for operation, only register readback for testing.
- **Inverters: SN74LVC1GU04DBVR**
  - Taken from database
- **Level-shifter: SN74LVC8T245DWR**
  - Taken from database



HFBR-2528Z Receiver, top view

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Power ICs

- **Linear Regulator: LP3964EMPX**
  - Taken from AROGON2_2CH design.
  - Supply 3.3V and 5.0V
- **Linear Regulator: TPS74201KTWR**
  - Taken from database
  - Supplies 1.8V analog and digital

- **None of these choices are critical for the design.**

- **In general, C0G were used where possible, and X5Rs were used where needed.**

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Control Scheme

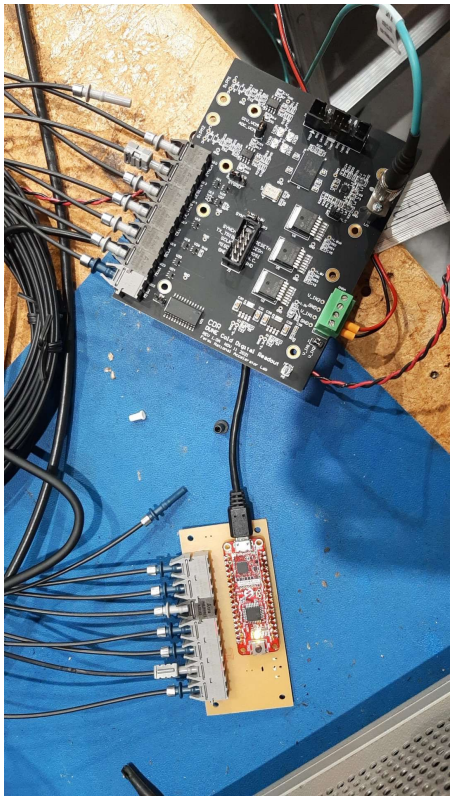
This ADC, the ADS52J90, must be configured over SPI before it will transmit data over the JESD204B interface.

The existing board implements the full set of control signals (1 Reset, 4 for full SPI R/W, two timing synchronization)

This could easily be reduced to 4, which could be shared by multiple devices.

By inverting some signals, no transmitters need to be on during normal operation.

The transmitters and receivers have been tested in liquid Argon and have operated reliably.



Power Considerations

- Current design uses 3 voltages,
  - no obvious way to reduce those with the current parts
- Usual power draw is 520mA @ 5.5V digitizing two channels at 75Mhz.
  - 450mA before configuration
  - From the datasheet: "**The ADC is designed to scale its power with the conversion rate.**"
  - 4 channels would likely only use slightly more power and could still be transmitted over a single fiber.
- Each controls receiver uses 14mA @ 5V (measured in liquid nitrogen)

System Flexibility

The ADS52J90 has 16 ADCs

Each ADC is attached to 2 sampling circuits, allowing a software choice of either input, or to alternate, sampling up to 32 channels at half the clock rate.

If one input is connected to the sampling circuits for two adjacent ADCs, it can also digitize at twice the clock rate, or digitally averaged for a 3-dB SNR improvement.

While keeping under the serial data limit of 5Gbps, the data from up to 8 ADCs can be transmitted over a single optical fiber. 4x 14-bit ADCs/fiber at 70MHz, for instance.

Table 1. Scheme of Driving the Input Pins (16-, 32-, 8-Channel Input Modes)

INPUT PAIR	CONNECTION TO THE EXTERNAL ANALOG INPUT SIGNAL		
	16-CHANNEL INPUT MODE[1][2]	32-CHANNEL INPUT MODE	8-CHANNEL INPUT MODE[1]
IN1	AIN1	AIN1	AIN1
IN2	—	AIN2	—
IN3	AIN2	AIN3	AIN1
IN4	—	AIN4	—
IN5	AIN3	AIN5	AIN2
IN6	—	AIN6	—
IN7	AIN4	AIN7	AIN2
IN8	—	AIN8	—
IN9	AIN5	AIN9	AIN3
IN10	—	AIN10	—
IN11	AIN6	AIN11	AIN3
IN12	—	AIN12	—
IN13	AIN7	AIN13	AIN4
IN14	—	AIN14	—
IN15	AIN8	AIN15	AIN4
IN16	—	AIN16	—
IN17	AIN9	AIN17	AIN5

Table 17. Lane Mapping to CML Pins[1]

DEFAULT LANE ID	MAPPING TO THE PINS	2 ADCS PER LANE (8-Lane Mode)[2]	4 ADCS PER LANE (4-Lane Mode)[2]	8 ADCS PER LANE (2-Lane Mode)[2]
1	CML1_OUTP-CML1_OUTM	ADC1, ADC2	ADC1…ADC4	ADC1…ADC8
2	CML2_OUTP-CML2_OUTM	ADC3, ADC4	—	—
3	CML3_OUTP-CML3_OUTM	ADC5, ADC6	ADC5…ADC8	—
4	CML4_OUTP-CML4_OUTM	ADC7, ADC8	—	—
5	CML5_OUTP-CML5_OUTM	ADC9, ADC10	ADC9…ADC12	ADC9…ADC16
6	CML6_OUTP-CML6_OUTM	ADC11, ADC12	—	—
7	CML7_OUTP-CML7_OUTM	ADC13, ADC14	ADC13…ADC16	—
8	CML8_OUTP-CML8_OUTM	ADC15, ADC16	—	—

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Status of Testing at Fermilab

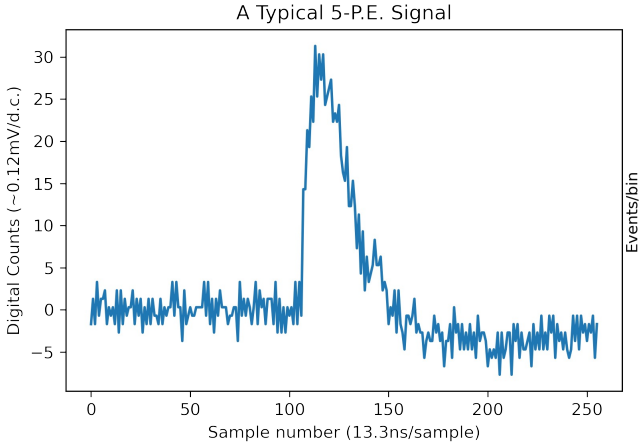
SiPM and Cryogenic test-stand is shared with the analog ARGON2 testing effort.

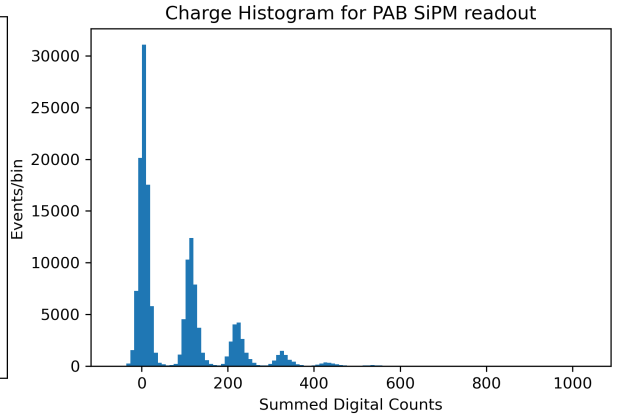
The Cold Digital Readout board operates reliably at both lab temperatures and in liquid Argon/Nitrogen without any configuration changes.

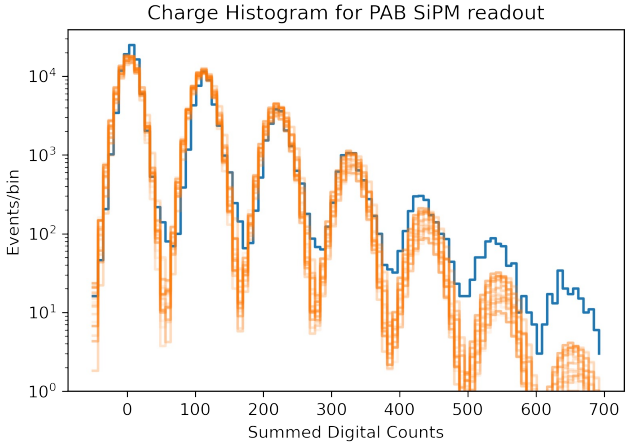
Benchmark data (shown here) taken last Friday. 14-bit digitization at 75MHz

Best fit results

Pedestal: 5dc
Pedestal RMS: 11.9dc
SPE: 107dc
SPE RMS: 5.0dc
Average SPE/trigger: 0.75







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Additional plots from the datasheet

CURRENT CONSUMPTION WITH JESD INTERFACE ENABLED				
I_{JESD}	Supply currents: JESD204B interface enabled, LVDS interface disabled at 12-bit, 80-MSPS, 4 ADCs per lane mode	AVDD_1P8 current(1)	170	mA
		DVDD_1P2 current(1)	260	
		DVDD_1P8 current(1)	40	
P_{JESD_CH}	Power dissipation in active mode per input channel: f_C = 80 MSPS, 12-bit mode, LVDS interface disabled, JESD interface enabled (4 ADCs per lane mode)	16-channel input mode	43.1	mW/channel
		32-channel input mode	21.6	

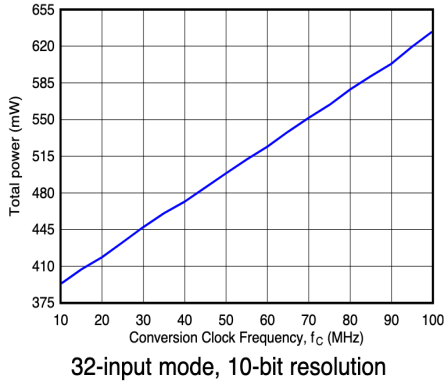

Figure 36. Total Power vs Conversion Clock Frequency

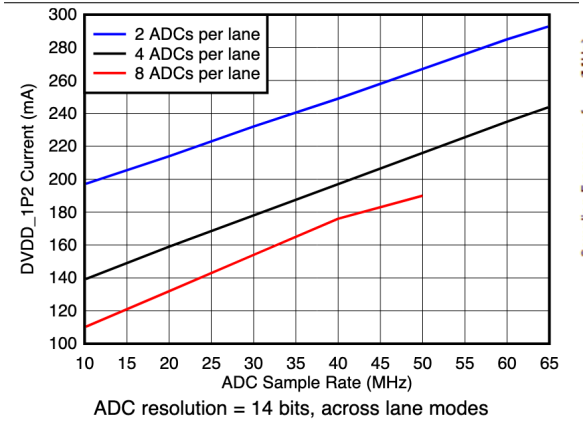

Figure 46. DVDD_1P2 Current vs ADC Sample Rate

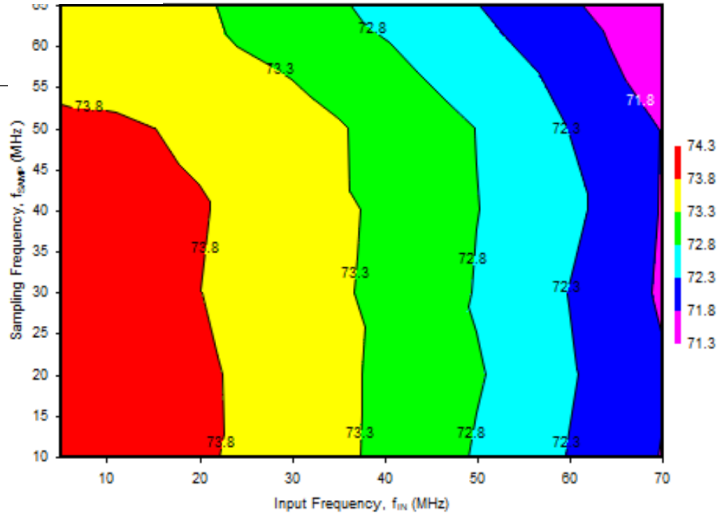

Figure 54. Signal-to-Noise Ratio in 14-Bit, 16-Input Mode

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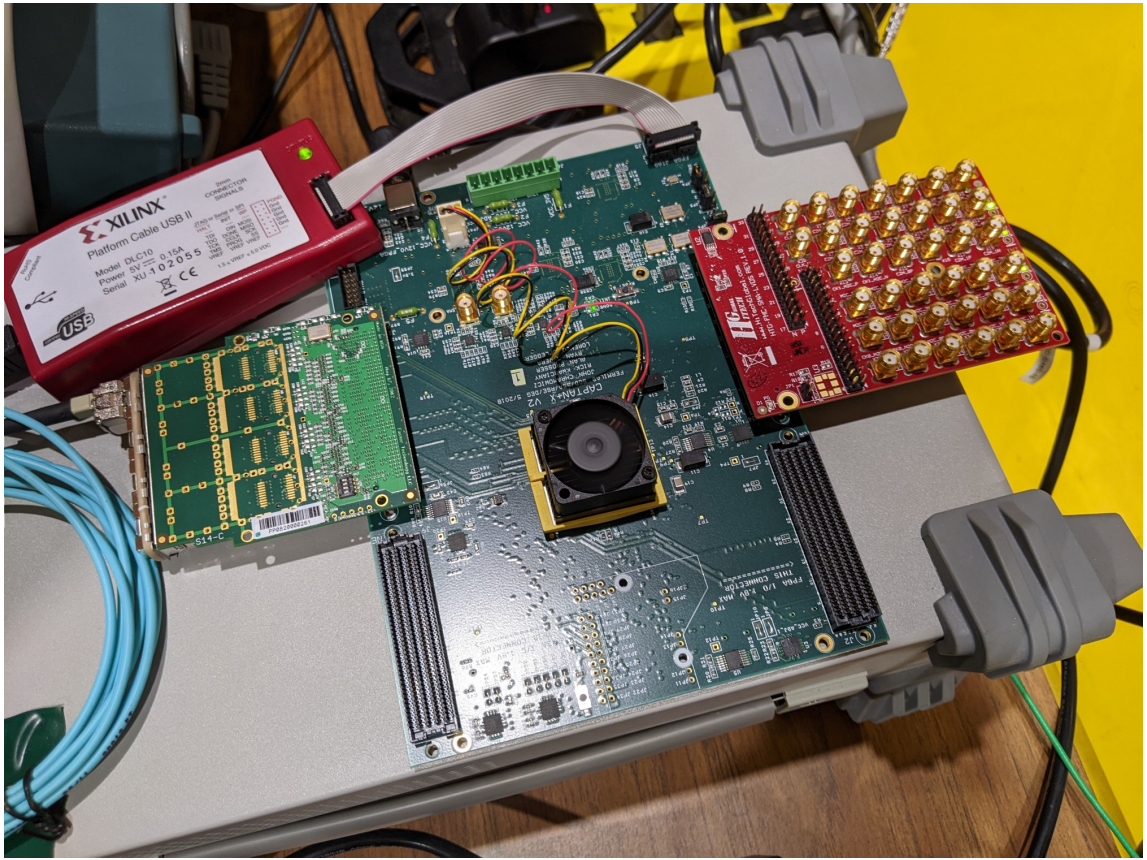
Test-stand warm-side readout



CAPTAN+X V2 (Kintex-7) board with 4x SFP+ Mezzanine board and SFP+ module installed. SMA board for external triger.

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