Lifetime study of COTS components for SBND/ProtoDUNE-I (ADC, LDO and FPGA)

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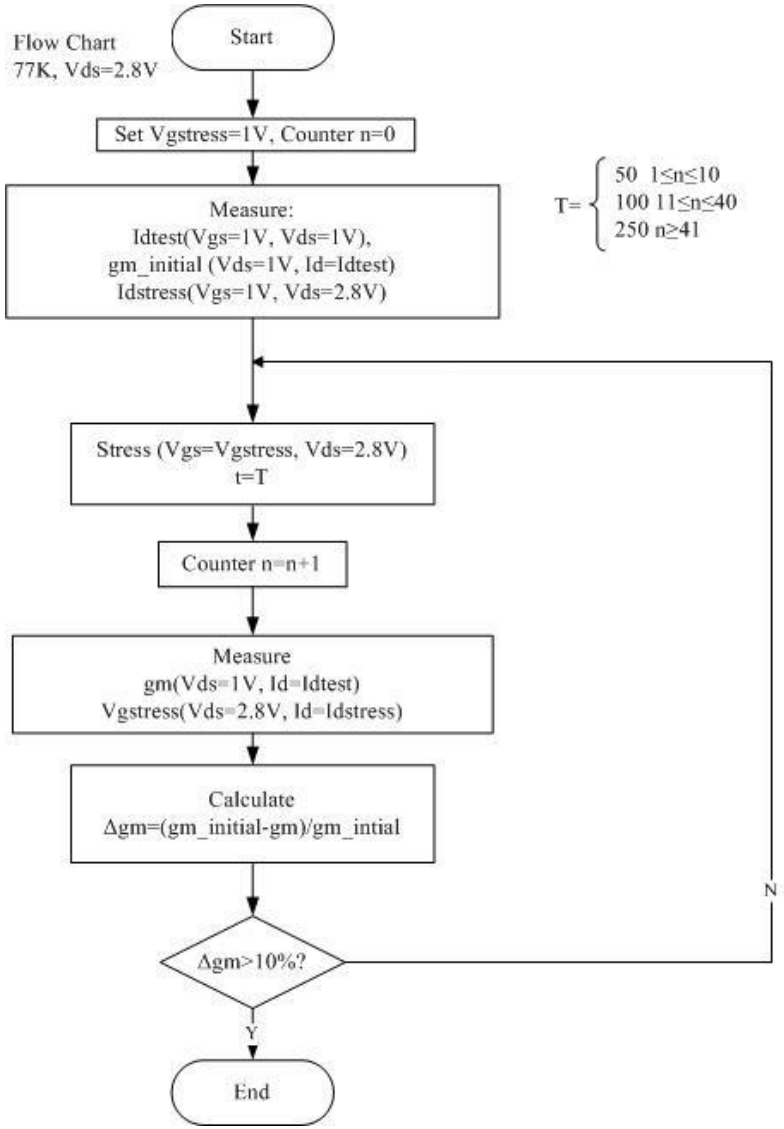
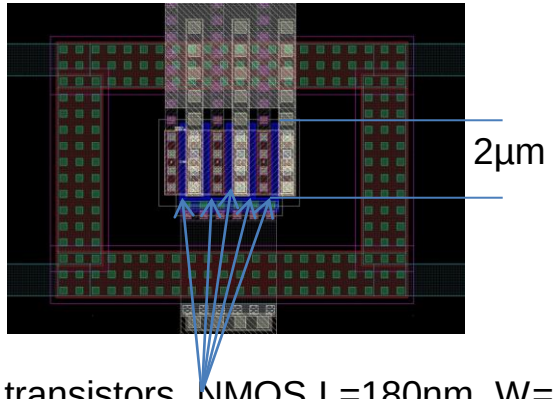
CMOS Lifetime Study – Principal Findings

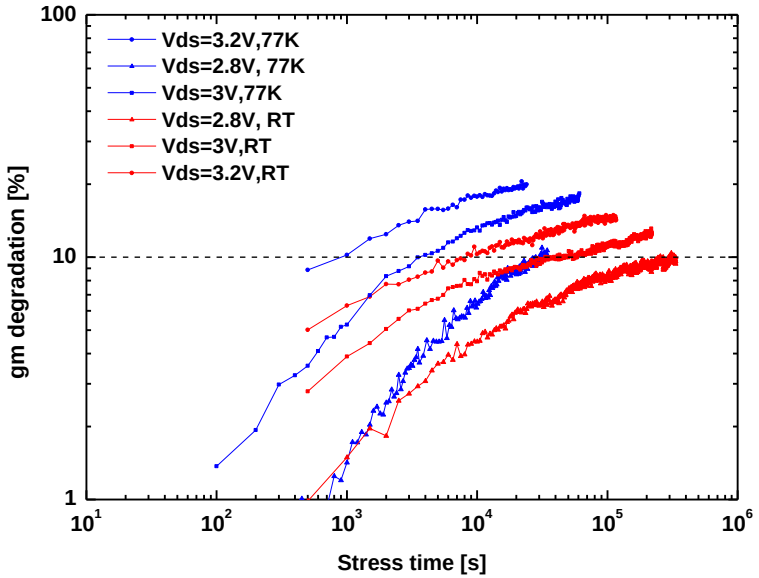
- A study of hot carrier effects on the device lifetime has been performed for the TSMC NMOS 180nm technology node at 300K and 77K. Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage (V_{ds}), and a separate measurement of the substrate current (I_{sub}) as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, $\tau \propto I_{sub}^{-3}$, and the latter confirms that below a certain value of V_{ds} *a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for MicroBooNE and DUNE falls naturally into this domain, where hot-electron effects are negligible.*
- The lifetime of a logic circuit driven at a clock frequency can be related to the lifetime of the NMOS transistor under continuous ***ac*** operation in terms of the ratio of the effective stress time during a change of state and the clock period. Thus the *Lifetime of digital circuits (**ac** operation) is extended by the inverse duty factor* $4/(f_{clock}t_{rise})$ *compared to **dc** operation.* This factor is large (>100) for deep submicron technology and clock frequencies needed for TPC readout.

Stress Test Flow Chart and Layout of test NMOS Transistors





Test transistors, NMOS L=180nm, W=10μm (5 fingers x 2μm), designed to have negligible IR drop and power dissipation <15mW in stress tests to prevent temperature change due to self-heating.



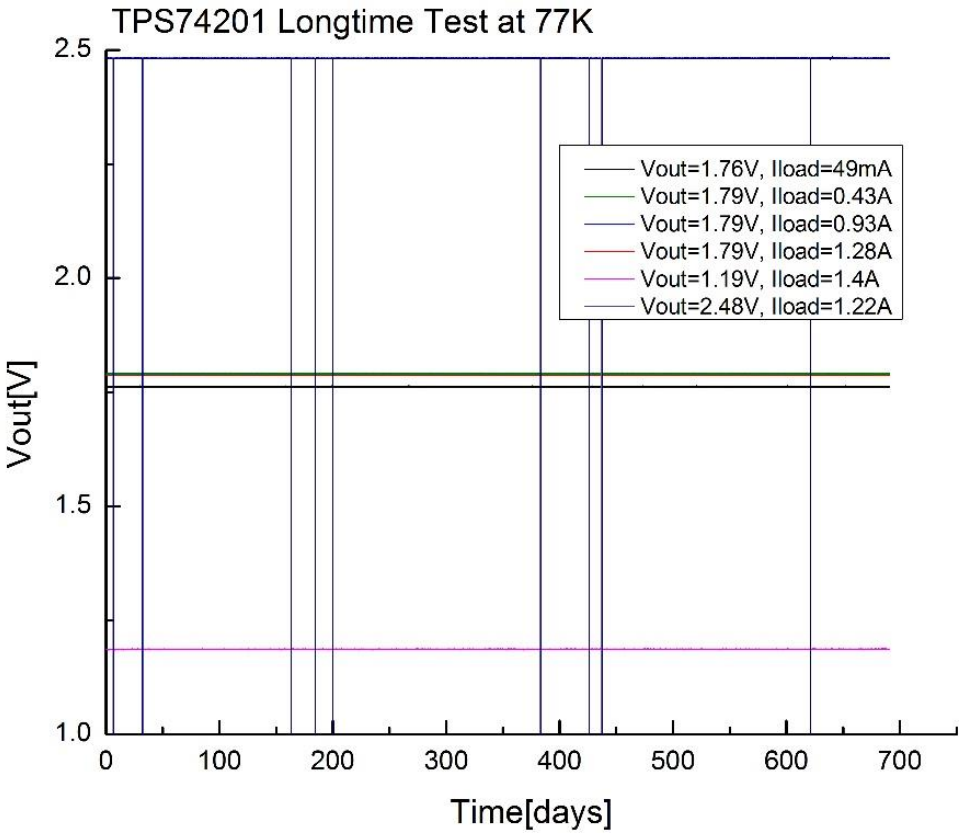
Regulator in LN2

Vendor	Part Number	Iout	Vout	Vin
ADI	ADP1708	1A	0.8V to 5.0V	2.5V to 5.5V
ADI	ADP1741	2A	0.75V to 3V	1.6V to 3.6V
ADI	ADP124ACPZ-1.8	500mA	1.8V	2.3V to 5.5V
ADI	ADP130AUJZ-1.8	350mA	1.8V	2.3V to 3.6V
ADI	ADP170AUJZ-1.8	300mA	1.8V	2.0V to 3.6V
Globaltech	GS2915L18F	150mA	1.8V	2.3V to 6.0V
Intersil	ISL9021	250mA	0.9V to 3.3V	1.5V to 5.5V
Intersil	ISL80113	3A	0.8V to 3.3V	1V to 3.6V
Linear	LTC3026	1.5A	0.4V to 2.6V	1.14V to 5.5V
Linear	LTM4616	16A	0.6V to 5V	2.7V to 5.5V
Linear	LTM4619	8A	0.8V to 5V	4.5V to 26.5V
Maxim	MAX8517	1A	0.5V to 3.4V	1.425V to 3.6V
National	LP38502TJ-ADJ	1.5A	0.6V to 5V	2.7V to 5.5V
TI	TPS73701	1A	1.2V to 5V	2.2V to 5.5V
TI	TPS78601	1.5A	1.2V to 5.5V	2.7V to 5.5V
TI	TPS78618	1.5A	1.8V	2.7V to 5.5V
TI	TPS78625	1.5A	2.5V	3.0V to 5.5V
TI	TPS74201	1.5A	0.8V to 3.6V	0.9V to 5.5V

- 18 regulators from major venders are evaluated. Two of them operate normally at 77K. TPS74201 is selected as the regulator applied in DUNE due to its relatively large output current and adjustable output voltage.
- Two sets of tests are performed to evaluate its stability and lifetime at 77K.

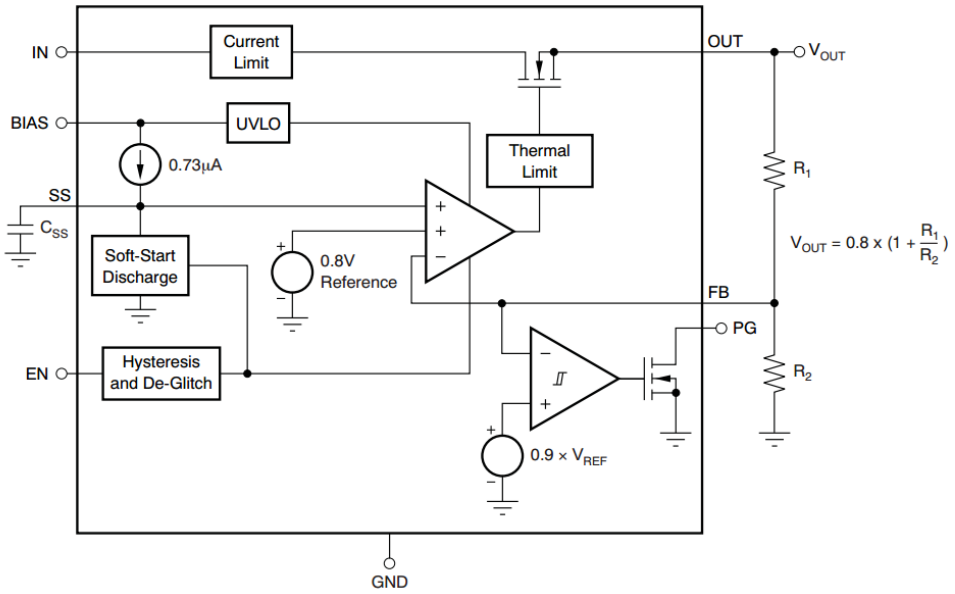
TPS74201 in LN2

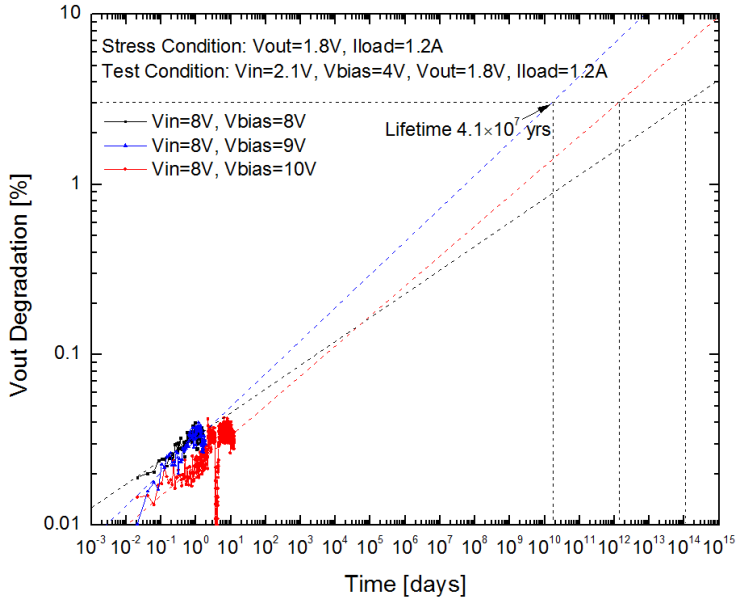
Regulator at 77K-Two Year Continuous Non-stress Test



A 2-year continuous non-stress test of six regulators biased at different operating condition has been performed. The output voltage of the regulator is stable over the full range of two years. Voltage drops are due to power glitch (power supply or computer shut down), movement of experiment setup, etc.

Regulator Stress Test



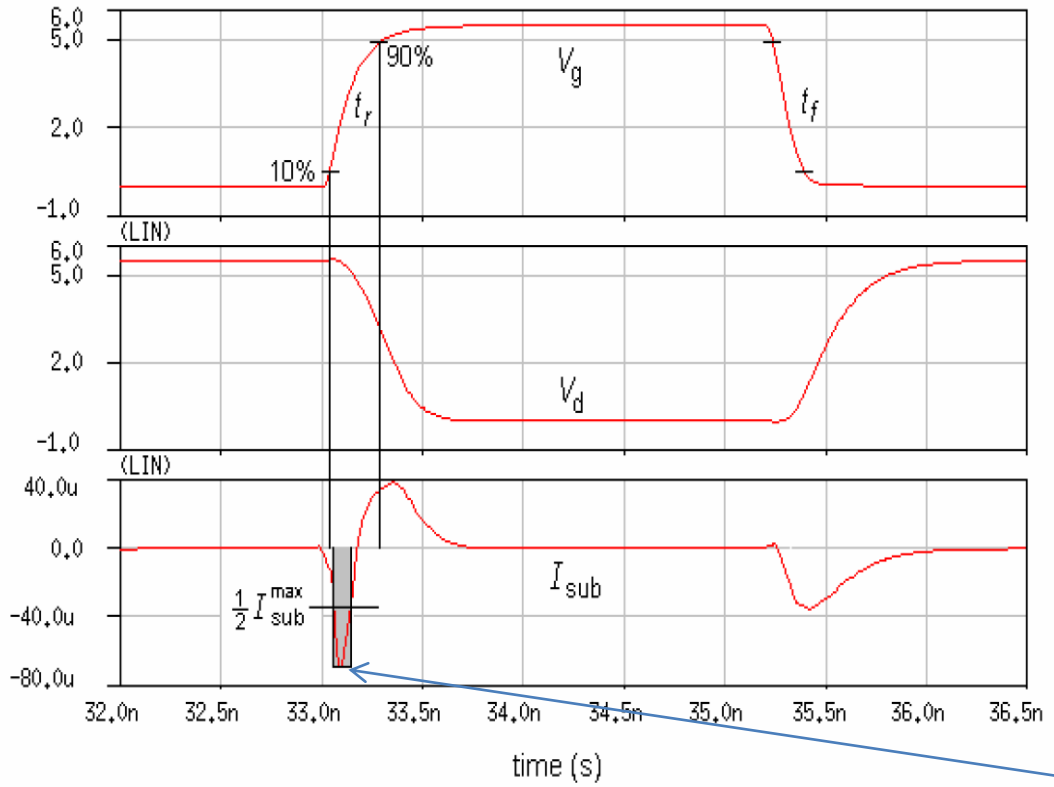


Block diagram of TPS74201 from the datasheet. Pin IN is the input voltage of the regulator while BIAS is the bias voltage for the internal logics. The absolute maximum voltage for both voltages is 6V.

Regulators are stressed under different voltages. For criteria of 3% degradation, the regulator under stress (Vin=Vbias=8V) already exhibits a lifetime of more than 10^7 years. Therefore, the operation of the regulator under normal operation (Vin=2.5V, Vbias=5V) at 77K is not of concern.

Effective Stress Time is a small fraction of the Clock Cycle

A standard method for evaluating the digital circuit lifetime is to apply accelerated stress test on a Ring Oscillator (RO) and observe the RO frequency degradation under severe stress. Degradation of drain current leads to increased rise (propagation) time and reduced frequency.



$$\left[\frac{ac\ stress\ time}{dc\ stress\ time}\right] \approx \left(f_{clock} t_{rise}\right)/4$$

Lifetime of digital circuits (ac operation) is extended by the inverse duty factor compared to dc operation.

This factor is large (>100) for advanced COTS chips with $f_{clock} > 32$ MHz and $t_{rise} < 500$ ps.

Hot-carrier induced degradation occurs only when the *substrate current* is high, i.e., nominal V_{ds} and high I_{ds}.

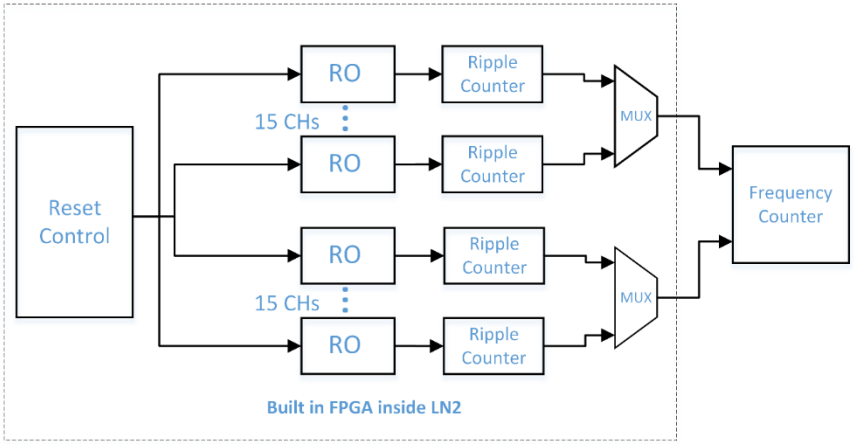
FPGA Candidates for Cryogenic Operation

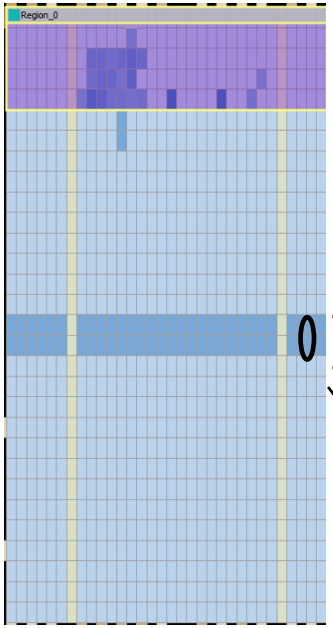
Vendor	Family	Technology	Speed of GTX [Gbps]	# of GTX	Memory [Mbit]	Core Voltage [V]	Status	
Altera	Arria GX	90 nm	3.125	4-12	1.2-4.5	1.2	Tested by BNL	✓
Altera	Arria II	40 nm	6.375	8-24	2.9-16.4	0.9	Tested by BNL	✗
Altera	Stratix II GX	90 nm	6.375	4-20	1.4-6.7	1.2	Tested by SMU	✓
Altera	Cyclone IV E	60 nm	n/a	n/a	0.3-3.9	1.0, 1.2	Tested by BNL	✓
Altera	Cyclone IV GX	60 nm	3.125	2-8	0.5-6.5	1.2	Tested at BNL	✓
Altera	Cyclone V	60 nm	3.125	2-8	0.5-6.5	1.2	Tested by BNL	✗
Xilinx	Virtex 5	65 nm	6.5	0-24	0.9-18.6	1.0	Tested by BNL	✗

List of FPGA screening tests: configuration (JTAG & Active Serial), embedded memory, high speed transceiver, I/O interface.

- Stress Methodology
  - The stress methodology we adopted follows the standard Accelerated Lifetime Strategy. The experiment is composed of two steps performed alternately:
    - Measurement Step: measure frequency of RO at Vccint=1.2V for 30s.
    - Accelerated Stress Step: accelerate degradation of RO at higher core voltage. Stress device (e.g. Vccint=1.8V) for 3600s.
  - In each measurement step, frequency measured from 15s to 30s are averaged for reliable result.
  - The degradation criteria is defined as 3% degradation of the frequency which is widely adopted [J. Zhang and S. S. Chu, 2002].

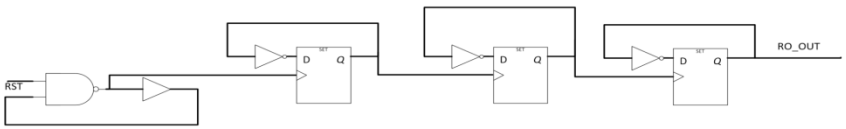
Experiment Block Diagram and FPGA Floor Plan



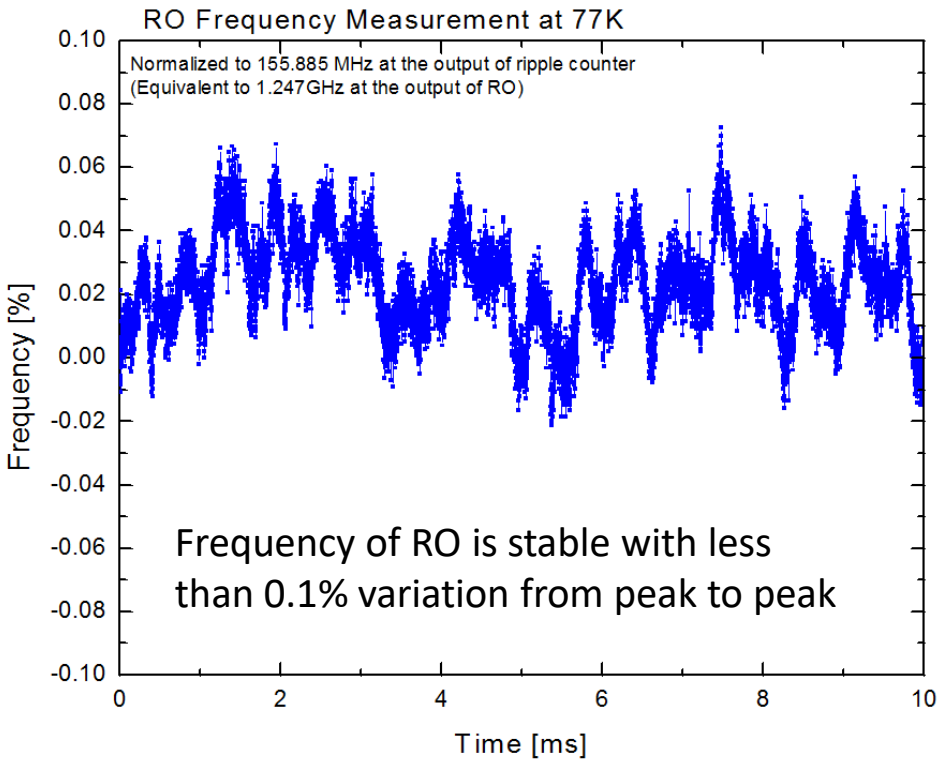


Control Logic. Control logic is locked down in the area with Logic-Lock

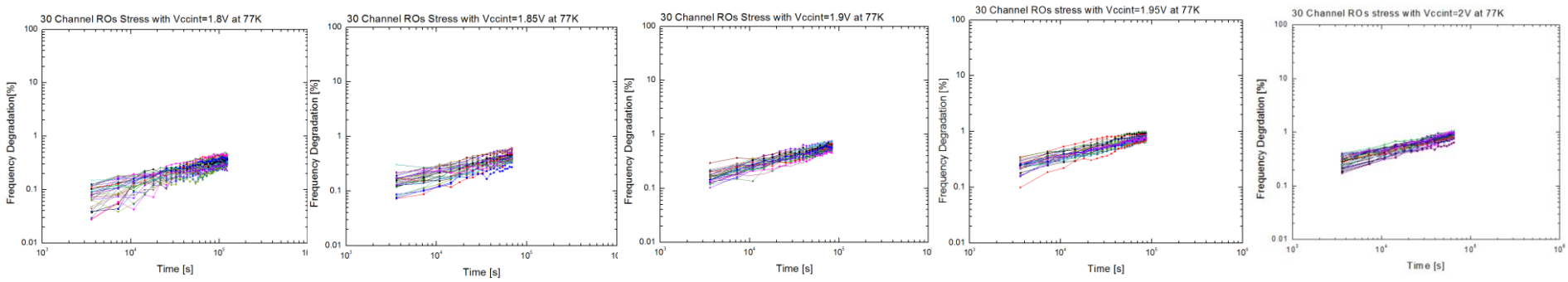
Array of 30 ROs. After the device is stressed under one voltage, another array of ROs will be locked down for stress.



FPGA Floor Plan

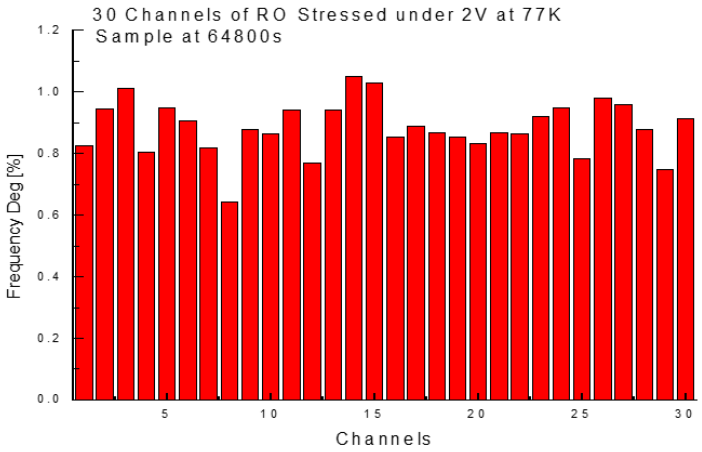


Degradation Result

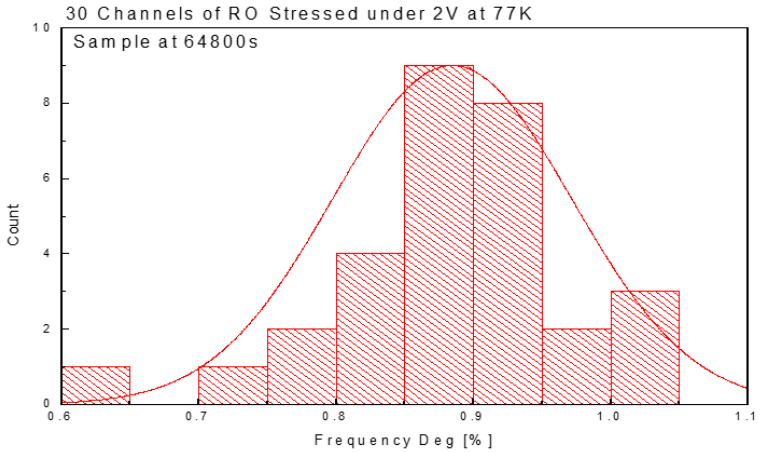


(a) (b) (c) (d) (e)

Degradation of RO stressed at (a) 1.8V, (b) 1.85V, (c) 1.9V, (d) 1.95V, (e) 2V



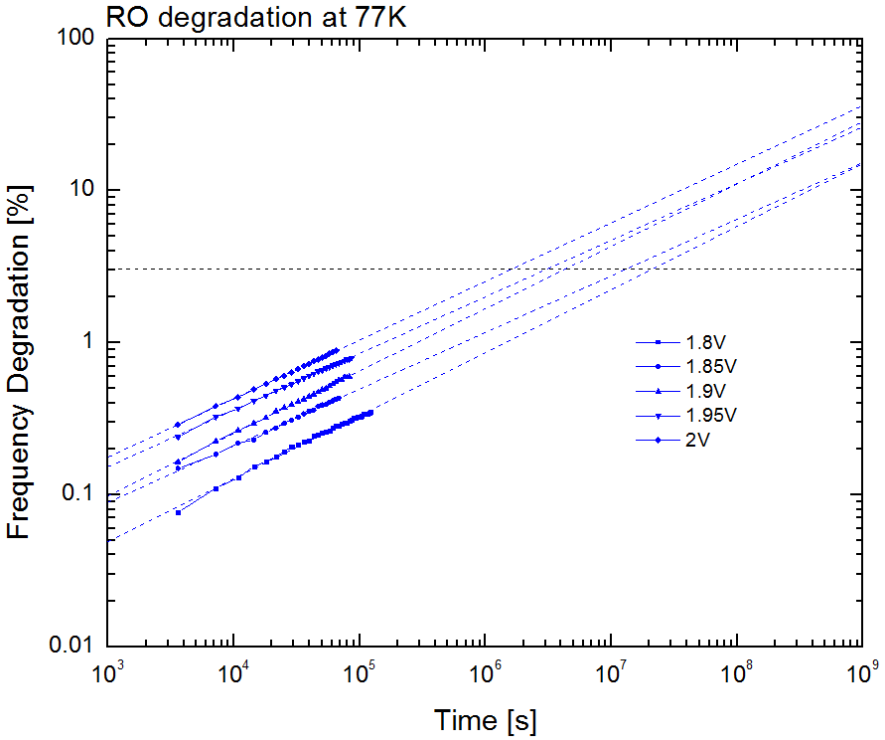
Frequency of 30 RO Channels

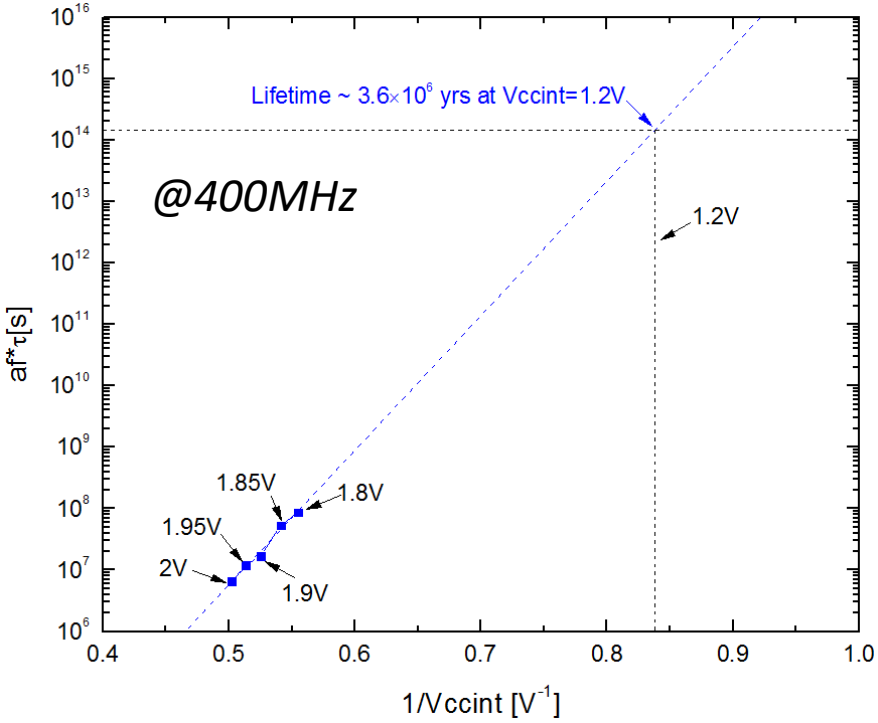


Frequency Histogram of 30 RO Channels.

- Statistical View of the Degradation of 30 RO Channels: μ=0.88, σ=0.087
- The mean of 30 RO Channels is used for each stress point to calculate the frequency degradation

Lifetime Projection of FPGA





- Traditionally, lifetime is projected by empirical equation $log_{10}\tau \propto 1/V_{ds}$. The target operation frequency is 400MHz while the RO is stress under 1.7GHz. To include the effect of higher stress frequency, frequency acceleration factor α_f is introduced which is defined as $\alpha_f = \frac{f_{stress}}{f_{target}}$. The equation for lifetime projection is modified as:

$$log_{10}\alpha_f\tau \propto 1/V_{ds}$$

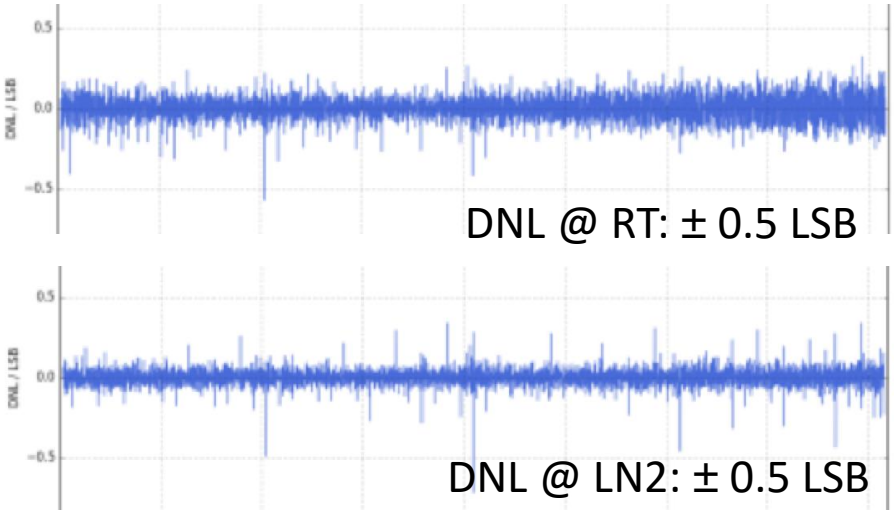
- Following the above equation, lifetime of FPGA at 77K is projected to be 3.6×10^6 years for 3% degradation criteria, giving a wide margin over the physical target (20~30 years) .

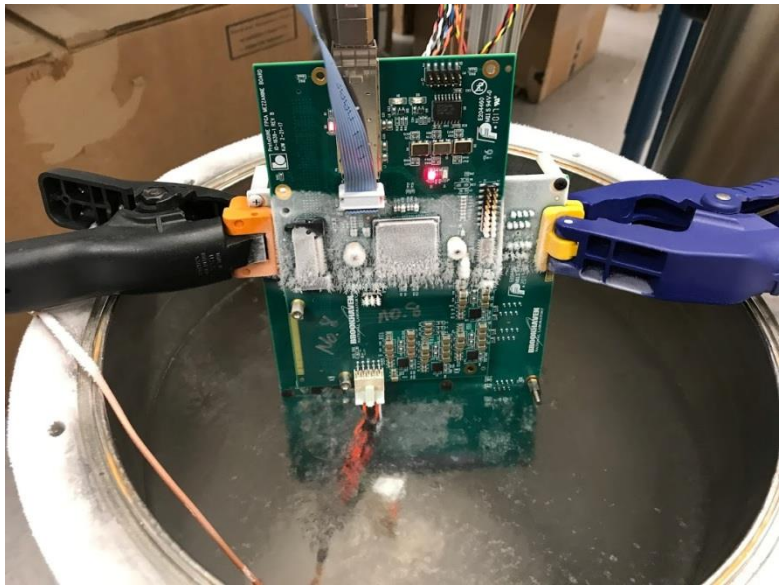
COTS ADC Lifetime Study

- COTS ADC candidates
  - ADI AD7274: 350nm CMOS TSMC foundry
  - TI ADS7049-Q1: 180nm CMOS TI foundry
  - TI ADS7883: 500nm CMOS TI foundry
- No internal regulator for the ADC candidates, a stress test can be devised based on the technology node
  - Given the degraded DNL performance of ADS7883 at LN2 temperature, AD7274 and ADS7049 will be main focus for lifetime study
  - With long channel length (350nm) of AD7274, the outlook to have long lifetime is reasonably high
  - Operating AD7274 well below its rated V_{ds}~3.6V, but within its operating range, e.g., at V_{ds}~2.8V, will provide a large lifetime margin
  - **ADI AD7274 commercial 12-bit SAR ADC is the main focus**
- Lifetime study of COTS ADC will take place in two different phases
  - The first phase is Exploratory phase
  - The second phase is Validation phase
  - Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is Preparation phase

Exploratory Phase (1)

- Preparation phase
  - Goal is to make test stand suitable for lifetime study
  - Parameters to be evaluated
    - Power consumption
    - Linearity: DNL/INL



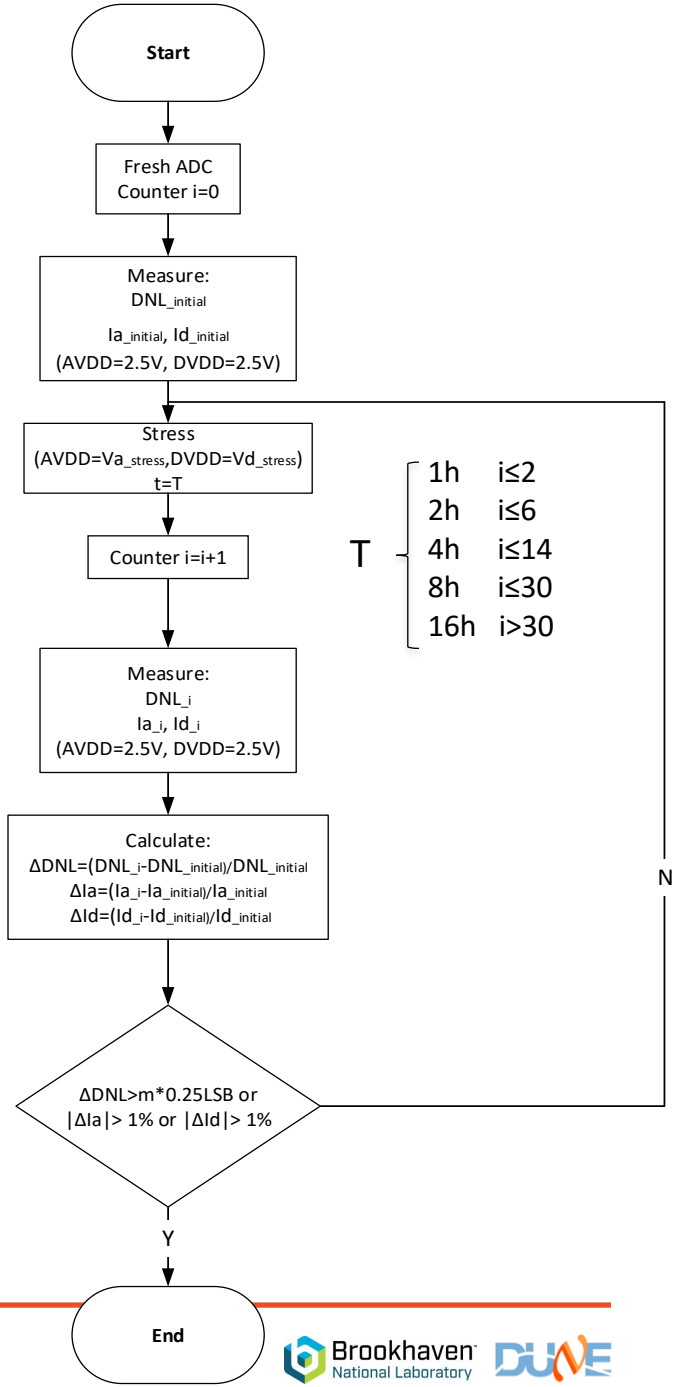


Test stand for cold screening test

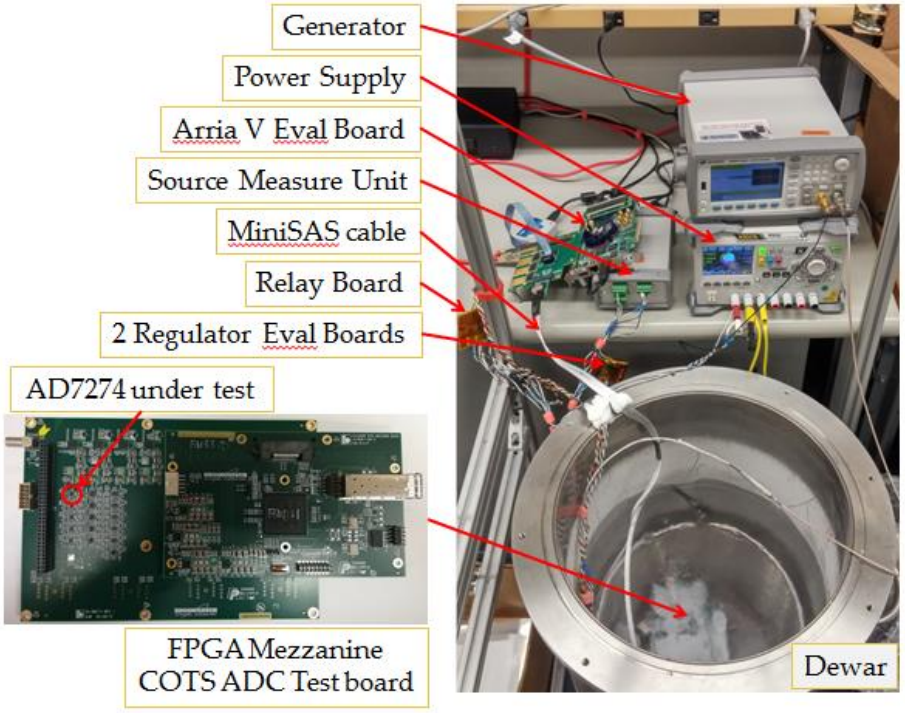
- Goal of exploratory phase is to define criteria of lifetime from the stress test
  - We will gain or lose confidence based on the test results in this phase
  - The ADC does not “fail”; the “lifetime” is a limit to specified performance

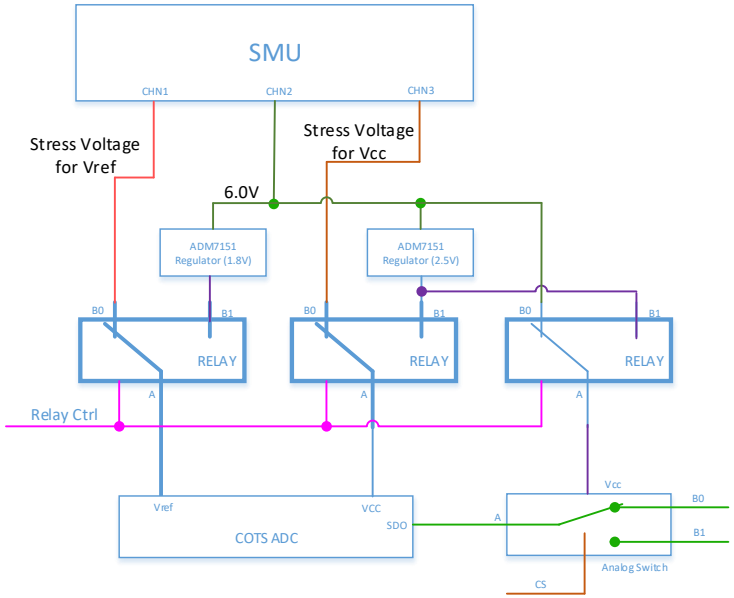
Exploratory Phase (2)

- Operation limit of COTS ADC was identified
  - The limit could be the ones which cause the ADC malfunctioning
- Only **fresh device samples** will be stressed within the operation limit
  - **Continuous** current monitoring
  - **Periodical** performance characterization
    - DNL / INL
- Stress test results will be used to extrapolate the lifetime of the COTS ADC
  - The development of lifetime criteria will be an iterative process, tailored to ADC technology, based on the test data to be collected and analyzed



ADC Stress Test Setup for the Exploratory Phase



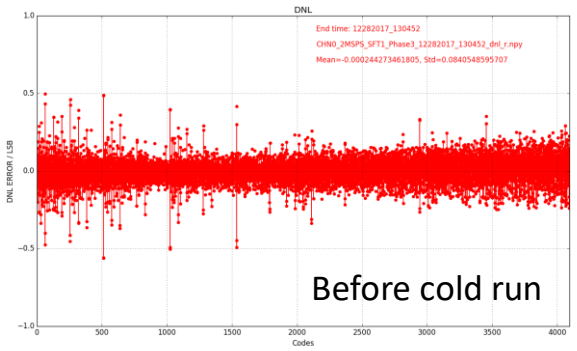


- Challenges of the stress test at cold
  - Cryogenic (77K)
    - Cold qualified components
  - Long term
    - Non-stop running at cold up to a month
  - Sensitivity
    - Current monitoring with μA level
    - Sigma of DNL with 0.01 LSB level
    - Signal integrity

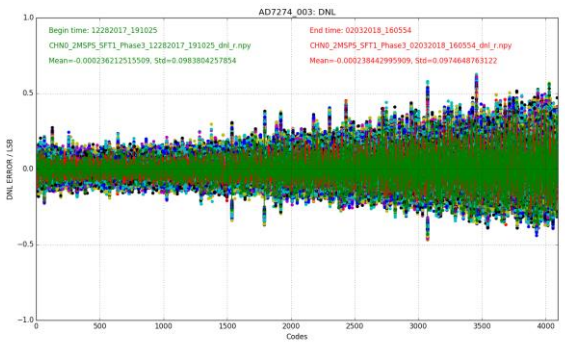
- ADC power scheme
  - Stress test
    - Precision current measurement
    - Powered by SMU directly
  - Performance characterization test
    - Lower noise gets right DNL/INL
    - Power from low noise regulator
  - Automatic switching for long term run

ADC with Nominal Operation Voltage

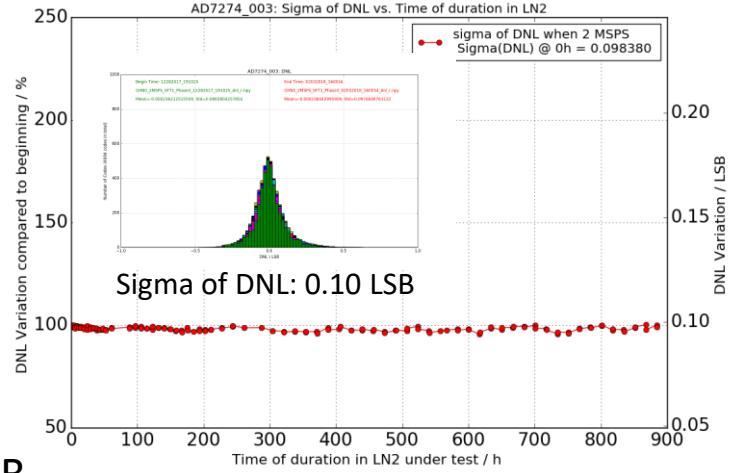
- A sample has run for 870 hours with nominal operation voltage
  - To verify if there is any significant change of current and DNL performance compared to the samples running with stress voltage as a crosscheck
  - V_{DD} = 2.5V, V_{REF} = 1.8V
    - Current or performance change is not significant
      - Variation of < 1% requires sources with the resolution of μA



DNL @ RT: ± 0.5 LSB

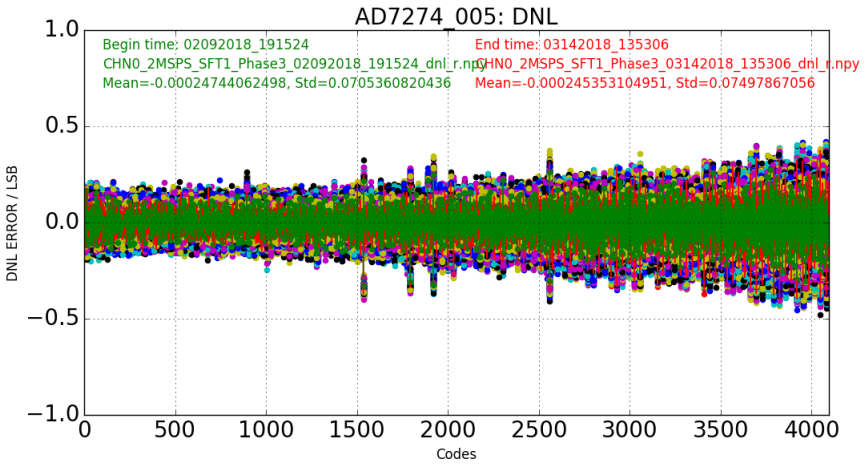


DNL overlap @ LN2: ± 0.5 LSB

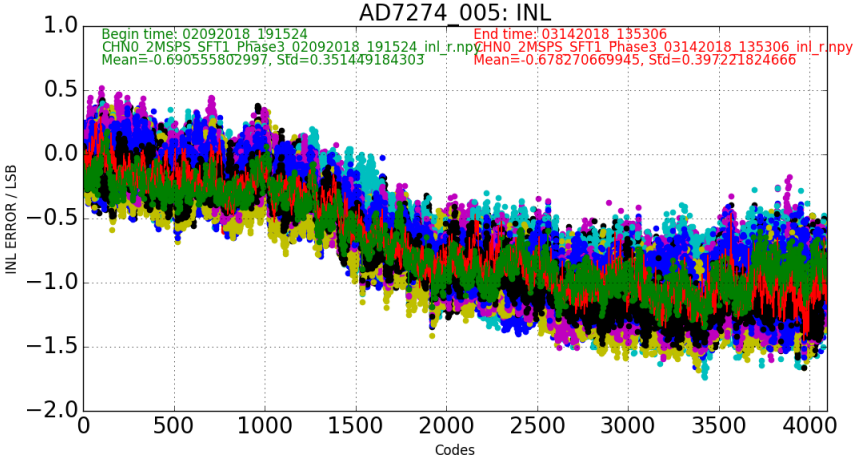


Sigma of DNL along the stress time

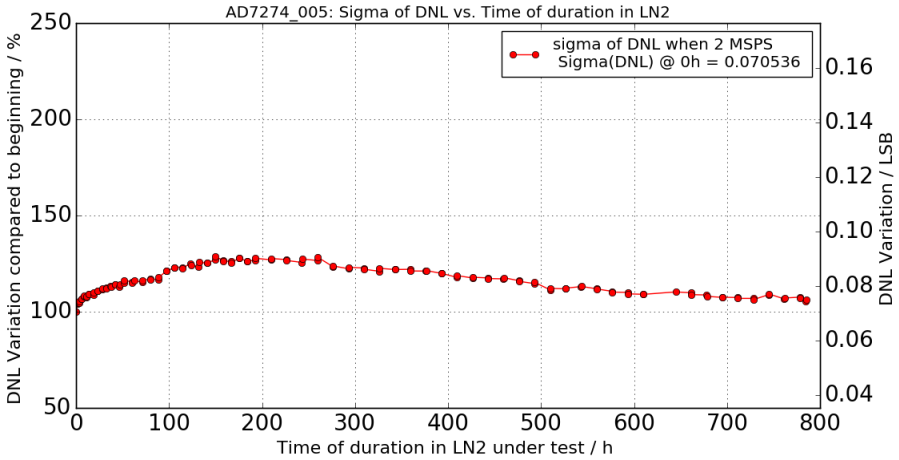
A Sample ADC Stressed at 5.25V at LN2 for 718 Hours



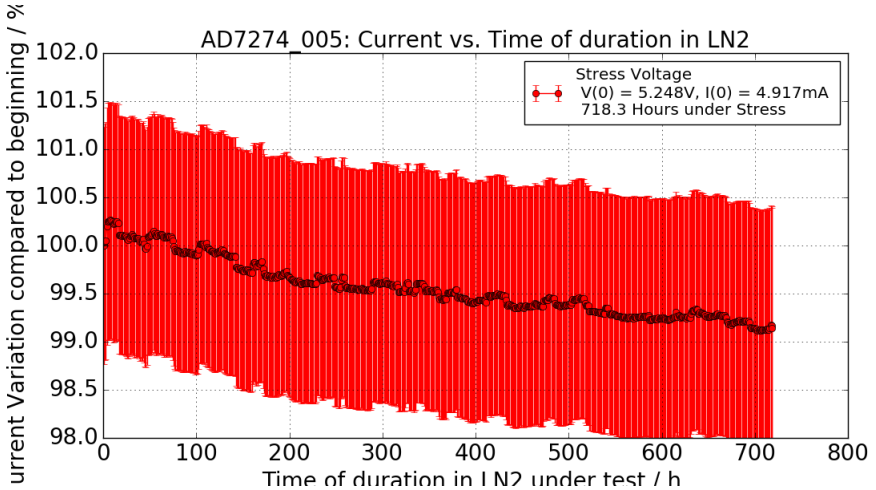
DNL overlap @ LN2: ± 0.5 LSB



INL overlap @ LN2: 2 LSB



Sigma of DNL smaller than 0.10 LSB



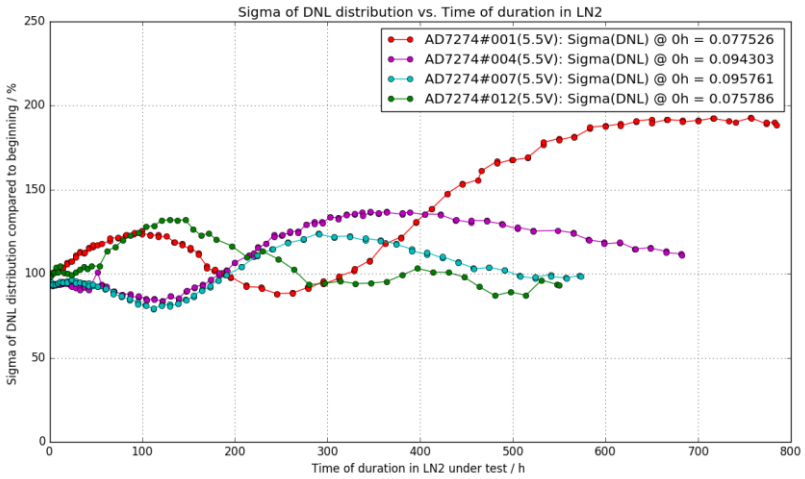
I_{VCC} decreases ~1%

Note: INL also includes the non-linearity of input triangle waveform

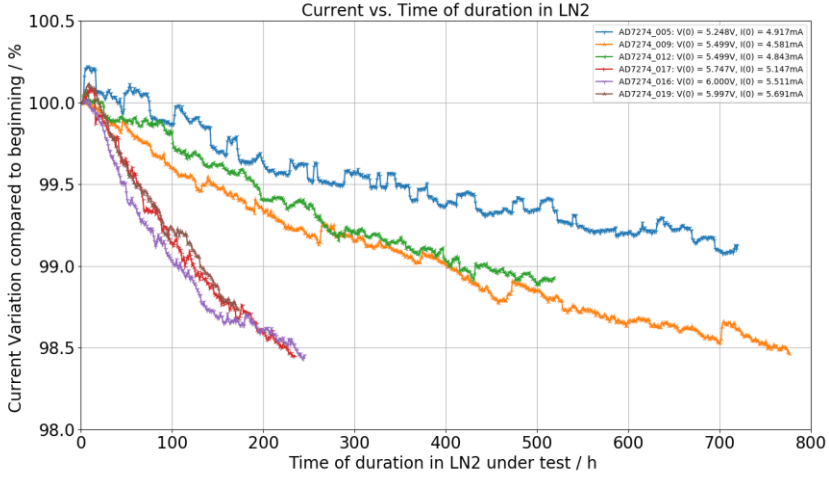
Brookhaven National Laboratory DUNE

The Criteria for Lifetime Study

- Li, S., Ma, J., De Geronimo, G., Chen, H., & Radeka, V. (2013). LAr TPC electronics CMOS lifetime at 300 K and 77 K and reliability under thermal cycling. IEEE Transactions on Nuclear Science, 60(6), 4737-4743.
  - The lifetime due to HCE at both the cryogenic temperature, as well as at room temperature, is limited by a predictable and a very gradual and monotonic degradation (aging) mechanism
  - Lifetime can be defined by any arbitrary but consistent criterion



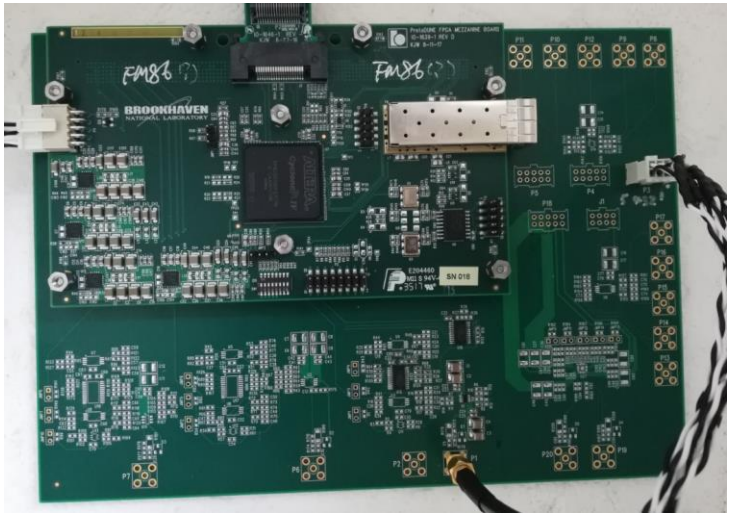
Sigma of DNL is less than 0.2 LSB
Non-monotonic change

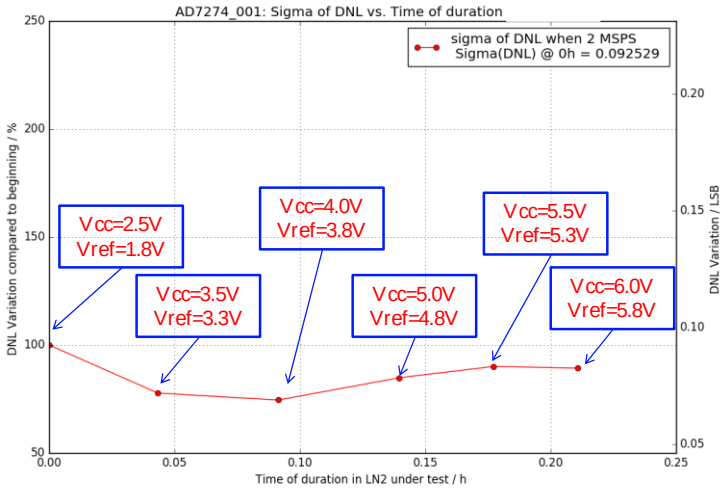


Variation of I_{VCC} will be used to assess the lifetime of COTS ADC

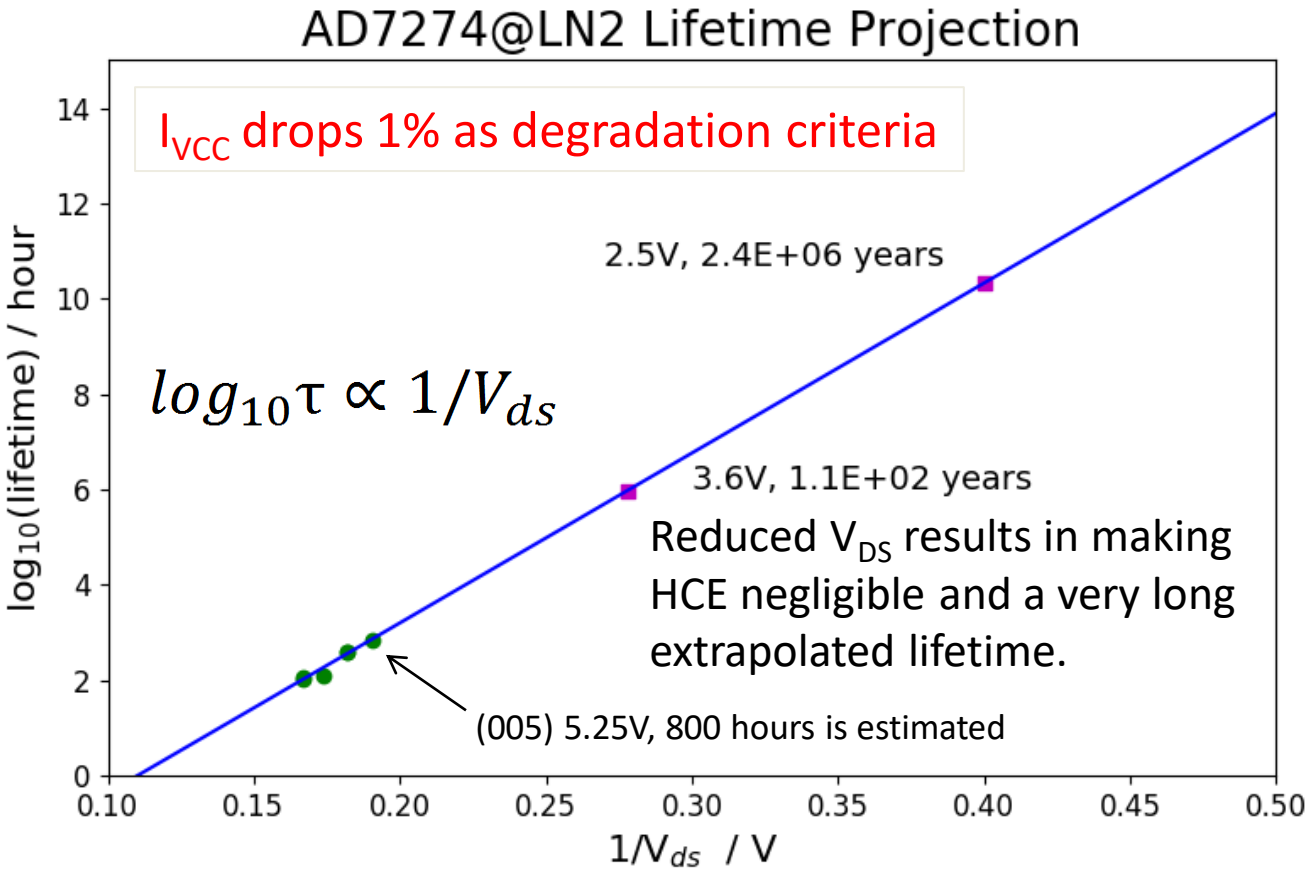
Validation Phase

- Goal is to collect more data to validate what we had learned in the exploratory phase
- Upgrade of the stress test stand
  - Support stress voltages up to 6V
    - The former one up to 5.5V
  - DNL/INL can be monitored as well as current with stress voltages
    - The former one can’t monitor DNL/INL during the stress





ADC Lifetime Projection



- The HCE (hot carrier effect) is negligible for COTS ADC, and **we'll be staying out of HCE during the detector operation**
- SBND collaboration has made decision to use COTS ADC

Summary

- Most of the major failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature
  - **channel hot carrier effects (HCE)**: The only remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature
- Accelerated lifetime test at any temperature (well-established by foundries)
  - transistor is placed under a severe electric field stress (large V_{DS}), to reduce the lifetime due to hot-electron degradation to a practically observable range.
  - It is widely used in industry
- This lifetime study has helped us to establish confidence about lifetime of the CMOS FPGA, ADC and Regulator to be operated in LAr.
- Lifetime is a very steep function of 1/Vds. HCE can be made negligible by a moderate reduction of V_{ds}.
- **The positive lifetime results on the FPGA, voltage regulator and ADC suggest, for their use in LAr, the lifetime shouldn't represent a concern. The HCE (hot carrier effect) will be negligible for these devices in long-term experiments (SBND or DUNE), and we'll be stay out of HCE during the detector operation.**

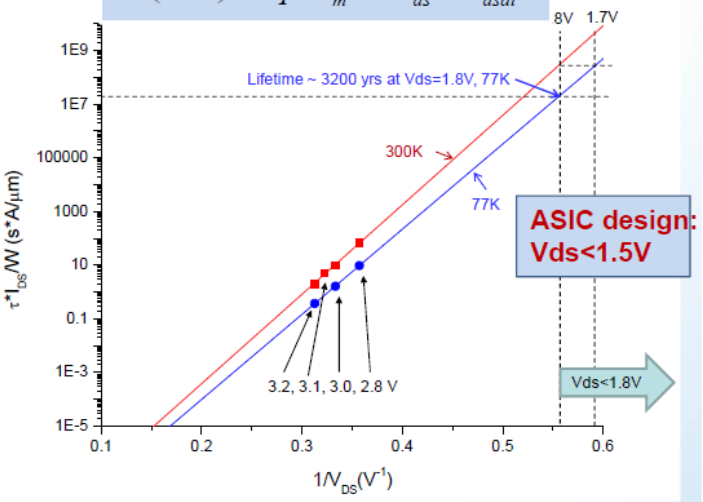
Backups

Lifetime Study

- The only remaining mechanism that may affect the lifetime of CMOS devices at cryogenic temperature is the degradation (aging) due to channel hot carrier effects (HCE).
  - Most failure mechanisms are strongly temperature dependent and become negligible at cryogenic temperature.
  - Lifetime due to HCE aging: A limit defined by a chosen level of monotonic degradation
    - The device “fails” if a chosen parameter gets out of the specified circuit design range. This aging mechanism does not result in sudden device failure.

- LArASIC is designed for long lifetime at cryogenic temperatures, with minimum gate length of 270 nm in TSMC 180 nm technology.
  - To alleviate the lifetime risk, custom ASIC should be designed for one or two orders of magnitude longer lifetime than 30 years, by selection of Vdd and L, essentially to get out of the region of degradation measurable after 30 years.
    - S. Li, et al, “LAr TPC Electronics CMOS Lifetime at 300K and 77K and Reliability under Thermal Cycling,” IEEE Transactions on Nuclear Science, Volume: 60, Issue: 6, Part: 2, Pages: 4737-4743 (2013)

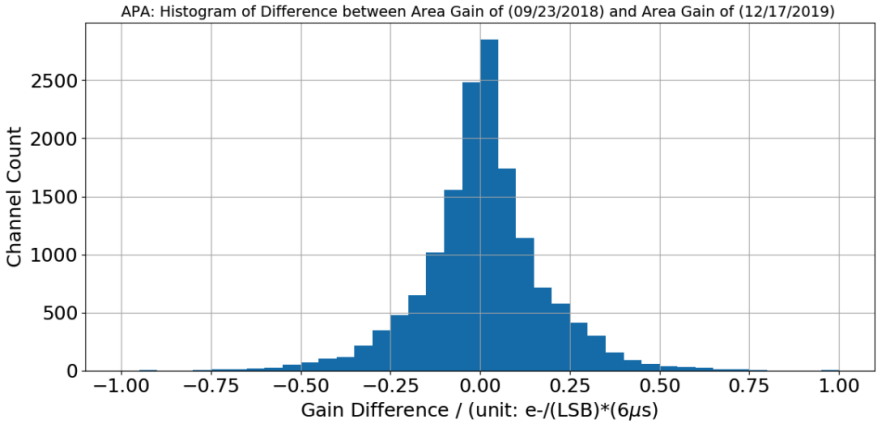
$$\ln\left(\frac{\tau I_{ds}}{W}\right) \propto \frac{\varphi_{it}}{q\lambda E_m} \propto \frac{1}{V_{ds} - V_{dsat}}$$



Accelerated Lifetime Measurements (180 nm)

Lifetime Study

- MicroBooNE: **LArASIC gain stability < 0.2% over 3-4 years**
- ProtoDUNE-I (SP): No measurement degradation is observed over a year
  - The measured gain shift is around 0.13% and 0.4%RMS, with an excellent agreement between 2018 and 2019 (around 0.01% shift with 0.3% RMS)
- The lifetime study of LArASIC will take place in two different phases, the exploratory phase and the validation phase. Before that, we will need to prepare the test stand to make it suitable for lifetime study, which is the preparation phase. The most time and effort will focus on the exploratory phase, we will gain (or lose) confidence based on the test results in this phase. Validation phase will be useful to validate what we would learn in the exploratory phase, and collect more information to prepare for future review(s)
  - **A P5 LArASIC was stressed at 3.0V over 300 hours in liquid nitrogen, no significant change in current drawn is observed.**
  - The recommended voltage for CM018/G is 1.8 V + 10%, which limits the stress voltage
    - commercial chips designed in TSMC 180 nm, e.g., AD9265 and AD9650, the absolute maximum rating is 2.0 V which is consistent with 1.8V + 10%
  - Test setup will be optimized with the dual-dut test board to observe more performance parameters
  - More tests will be carried out after the busy ProtoDUNE-II production



ProtoDUNE-SP: Good reliability over a year operation