FD1-HD PD* cold amplifier
Design, reliability, ganging results

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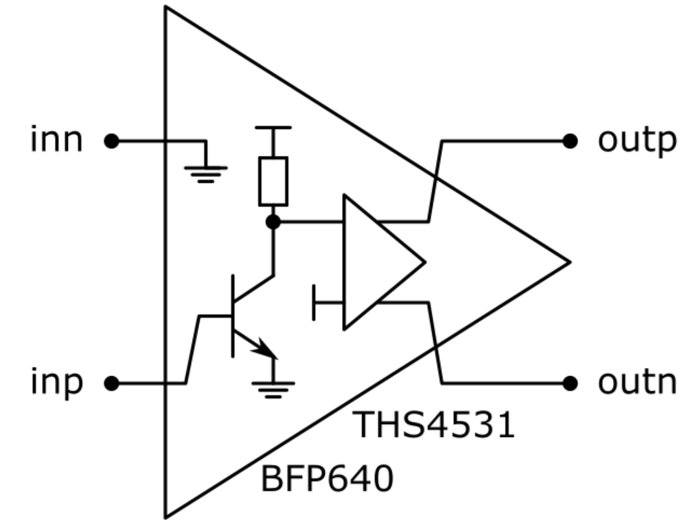
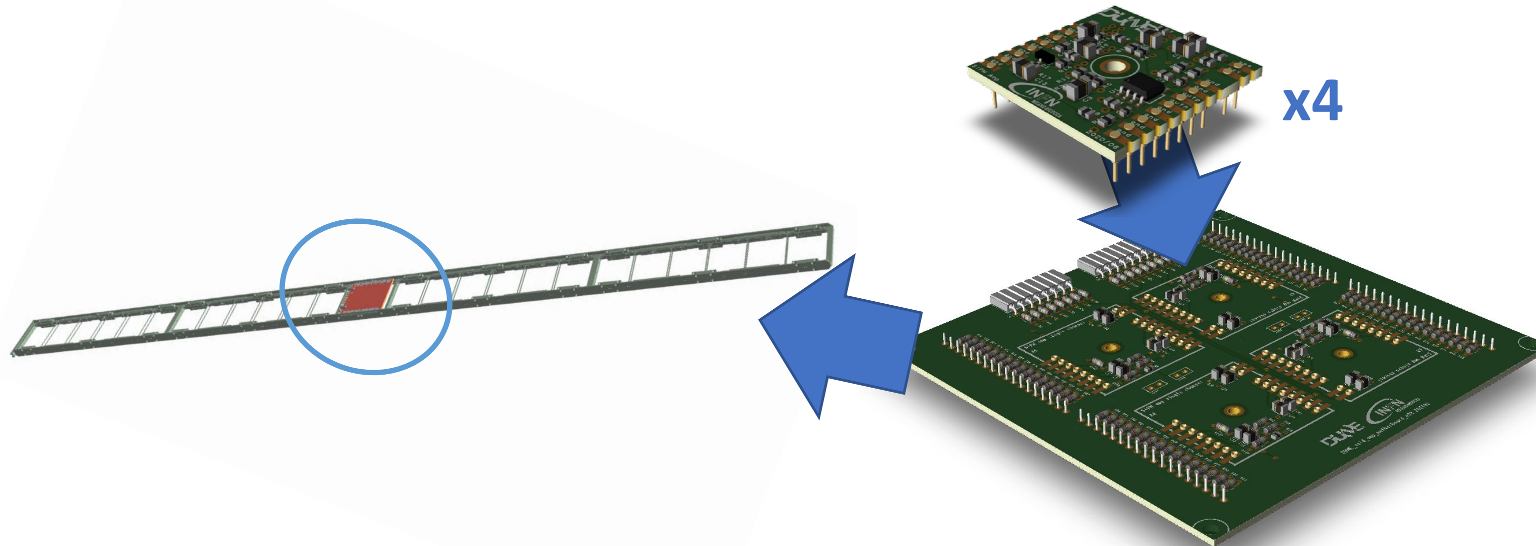
On behalf of the DUNE FD1-HD PD Electronics and Photosensors Working Groups

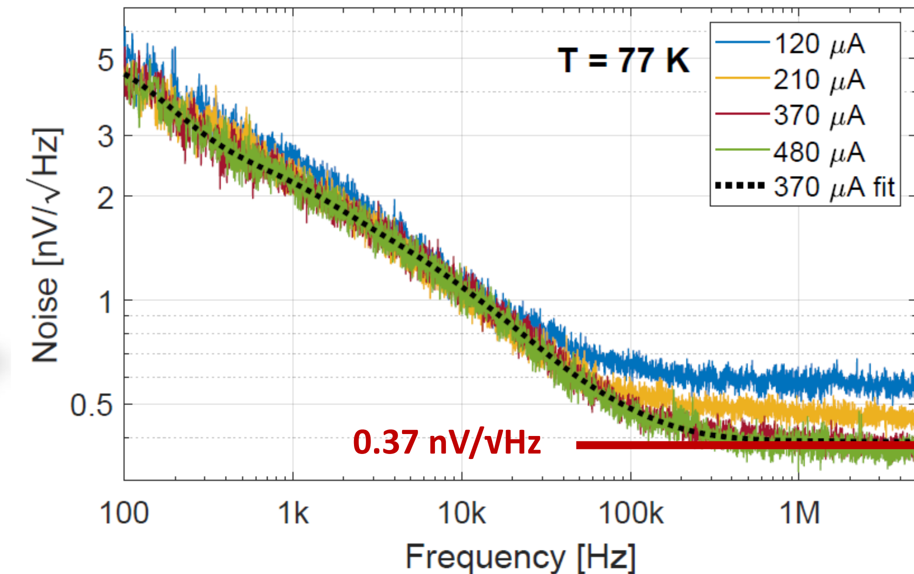
*DUNE Far Detector 1 Horizontal Drift Photon Detector

Design (1)

- 48x 6x6 mm^2 SiPMs in parallel: total input capacitance ≈60-80 nF
- SiPM signal time constant: ≈400 ns [High Rq SiPM models were favoured for lower correlated noise (afterpulse, xtalk)]
- **→ Series white noise must be kept small**
- Pseudo-differential configuration based on discrete commercial components
  - **BFP640 SiGe bipolar transistor** for low series noise at low bias current (0.4 nV/√Hz @ Ic=0.4 mA)
  - **THS4531 differential opamp** for high loop gain & differential outputs
  - More details here: https://doi.org/10.1088/1748-0221/15/01/P01008
- For ProtoDUNE2: single channel daughter cards mounted on 4-channel motherboards





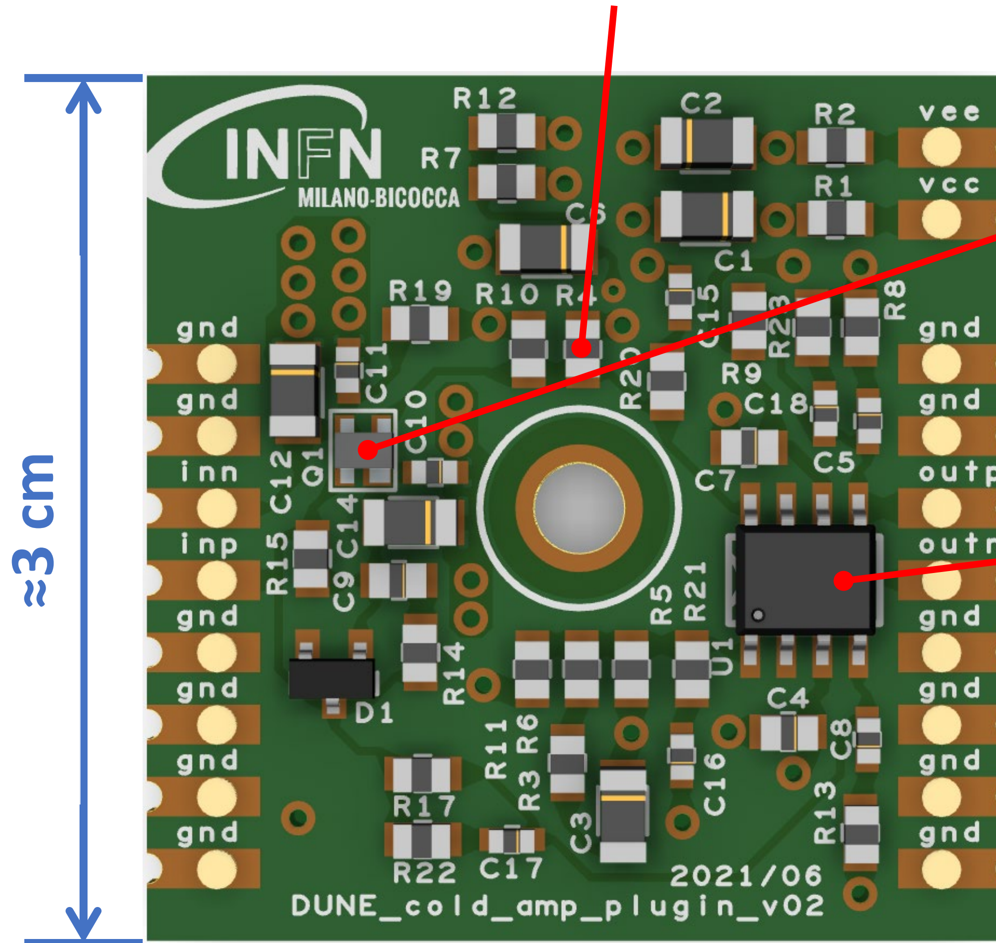


Design (2)

- Total power at cold (one channel):
  0.7 mA x 3.3 V ≈ **2.4 mW**
- Max power density **< 1mW/mm²** (1 kW/m²)

0603 size: 1.55*0.85 = 1.3 mm²
Power density: 0.75 mW/mm²

Bias resistor for the input transistor:
1 mW [0603]



Input transistor:
0.45 mW [SOT343]

SOT343 size: 2.1*1.25 = 2.6 mm²
Power density: 0.17 mW/mm²

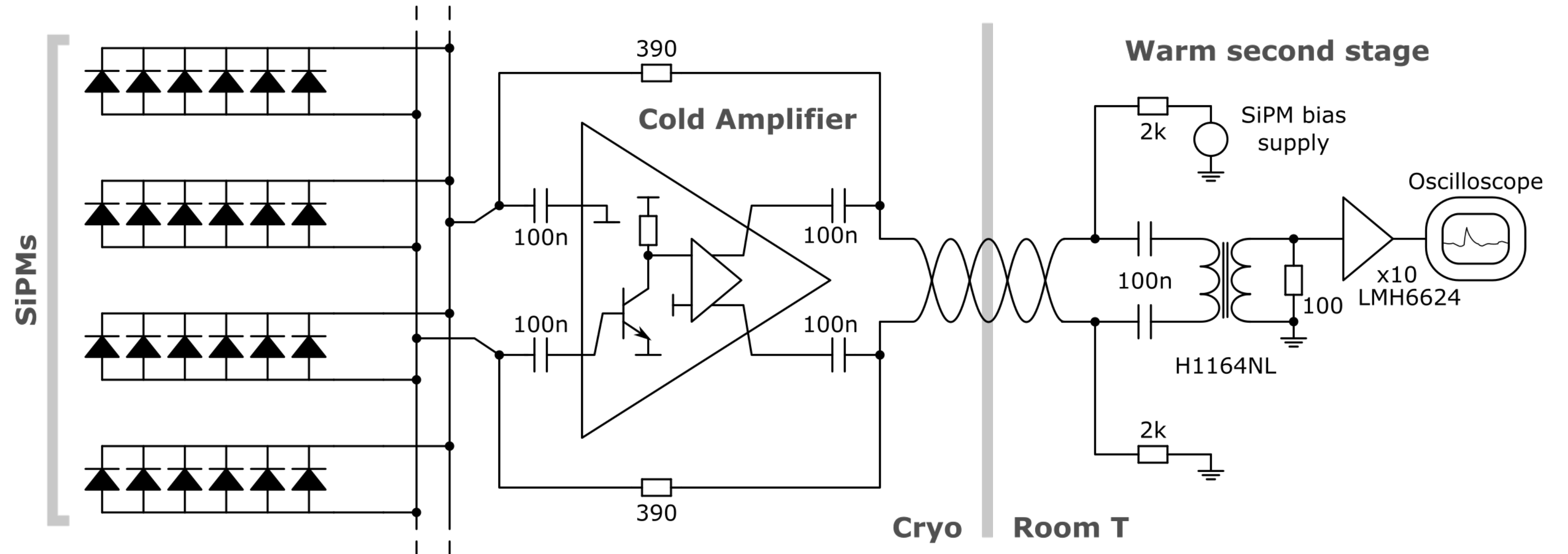
Opamp:
0.6 mW [SOIC8]

SOIC8 size: 4.9*3.9 = 19 mm²
Power density: 0.03 mW/mm²

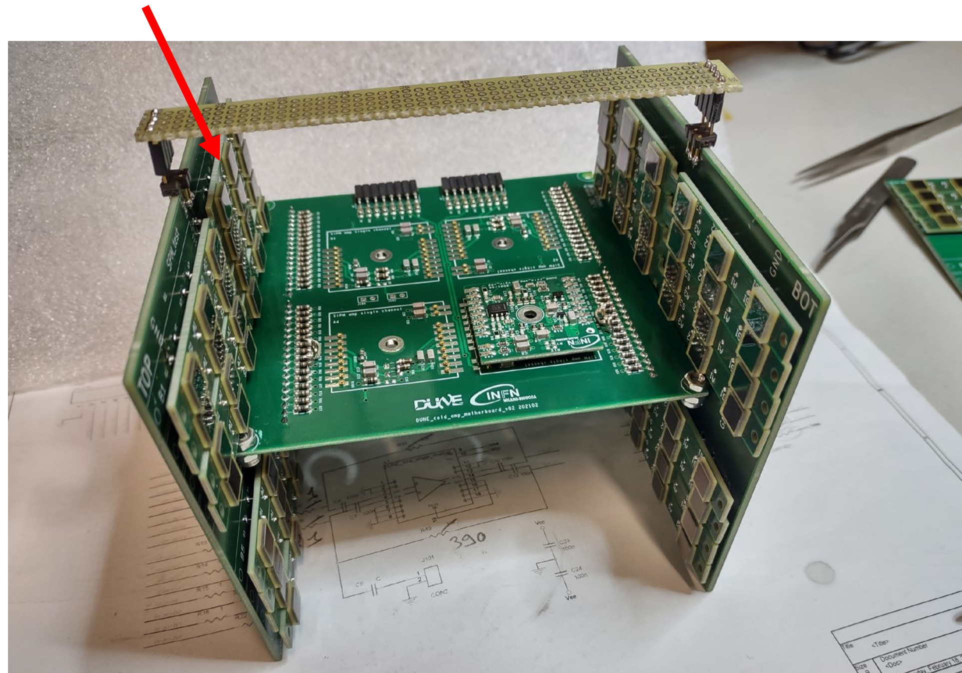
(Assuming dissipation only on the top face of components)

Signals and S/N (1)

- Scheme used to characterize the amplifier on the test bench
- The warm second stage mimics the input stage of the DAPHNE digitizer board



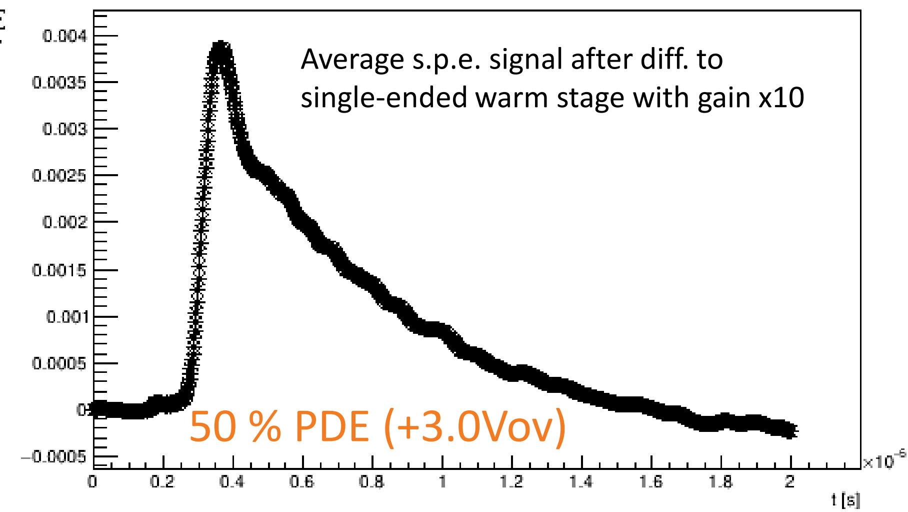
FD1-HD SiPM boards (6 SiPMs each)

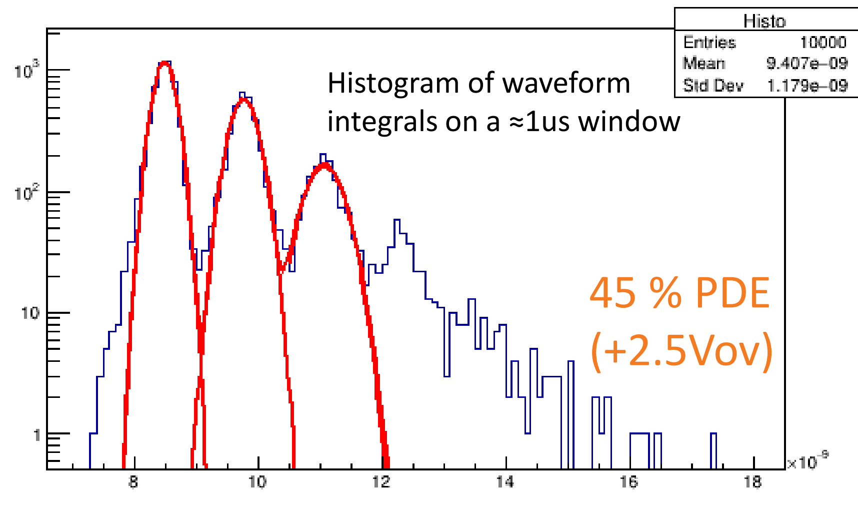


Signals and S/N (2)

Requirements:
- **≈2000 p.e. dynamic range (at typical Vov for 45% PDE)**
- **<100 ns signal rise time**
- **S/N>4**

Hamamatsu 75um HRQ (48 6x6 mm^2 SiPMs in parallel)



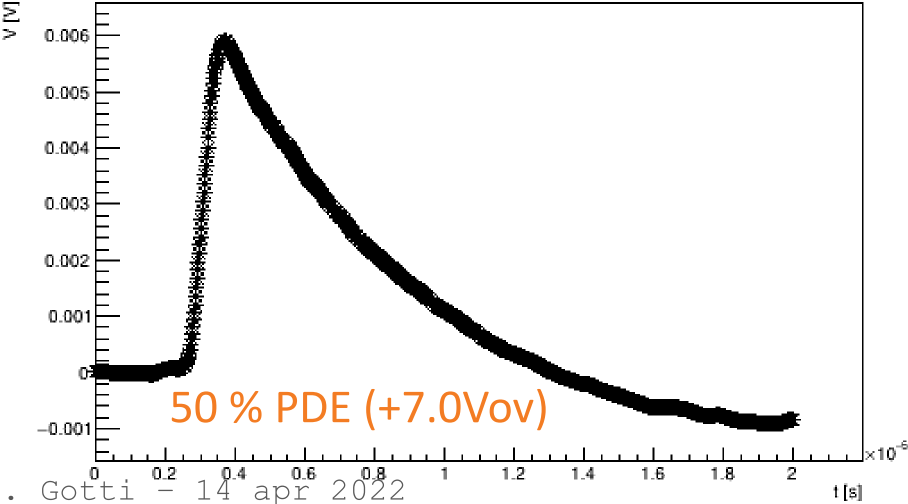


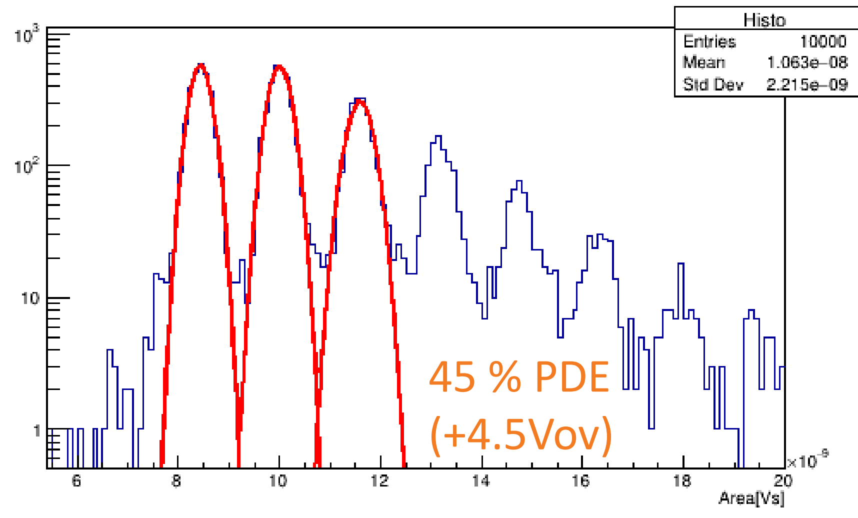
Dynamic range before saturation of the opamp output stage on 100-ohm diff. load

PDE	Vov	DR (p.e.)	S/N
40%	2.0	≈2900	6.30
45%	2.5	≈2350	7.49
50%	3.0	≈2000	8.92

Single p.e. gain divided by sigma of the baseline

FBK 50um TT (48 6x6 mm^2 SiPMs in parallel)





PDE	Vov	DR (p.e.)	S/N
40%	3.5	≈2500	5.64
45%	4.5	≈2000	7.56
50%	7.0	≈1250	11.32

Reliability: sources

IEEE TRANSACTIONS ON NUCLEAR SCIENCE, VOL. 60, NO. 6, DECEMBER 2013 4737

LAr TPC Electronics CMOS Lifetime at 300 K and 77 K and Reliability Under Thermal Cycling

Shaorui Li, Jie Ma, Gianluigi De Geronimo, Hucheng Chen, and Veljko Radeka

Abstract—A study of hot-carrier effects (HCE) on the 180-nm CMOS device lifetime has been performed at 300 K and 77 K for Liquid Argon Time Projection Chamber (LAr TPC). Two different measurements were used: accelerated lifetime measurement under severe electric field stress by the drain-source voltage V_{ds}, and a separate measurement of the substrate current as a function of $1/V_{ds}$. The former verifies the canonical very steep slope of the inverse relation between the lifetime and the substrate current, and the latter confirms that below a certain value of V_{ds} a lifetime margin of several orders of magnitude can be achieved for the cold electronics TPC readout. The low power ASIC design for LAr TPC falls naturally into this domain, where hot-electron effects are negligible. Lifetime of digital circuits (ac operation) is extended by the inverse duty factor $1/(f_{clock} t_{eff})$ compared to dc operation. This factor is large (> 100) for deep submicron technology and clock frequency ... may be re... in previou... cuit board... immersion... total failu... low.

Index T...

at cryogenic temperature is t... ionization, which causes interf... trapped charge. The degradatio... ductance, output resistance, and... mainly concerns n-channel de... devices (PMOS), affected by a ... [7], [8], typically exhibit a lifet... nitude longer than that of the n-... represent a concern in our cas... not result in sudden device failu... ization depends on the operatin... the maximum for minimum ch... at the maximum drain-source...

Reliability and Lifetime of Electronics in the cold : past, present and future

Veljko Radeka

radeka@bnl.gov

DUNE CE Workshop 07/16-18/2018

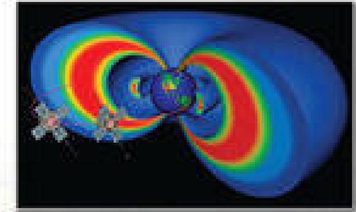
Development of Cold COTS ADC for SBND TPC Readout

H. CHEN ON BEHALF OF SBND COLD ELECTRONICS TEAM

BROOKHAVEN NATIONAL LABORATORY

MAY 16TH, 2018

EXTREME ENVIRONMENT ELECTRONICS



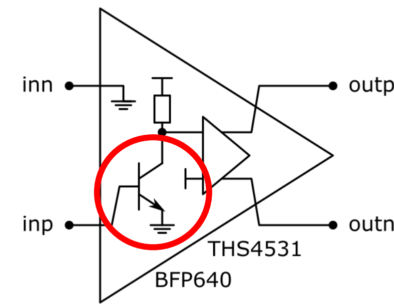
Edited by John D. Cressler H. Alan Mantooth

CRC Press

→Resulting in the plan we are now following:

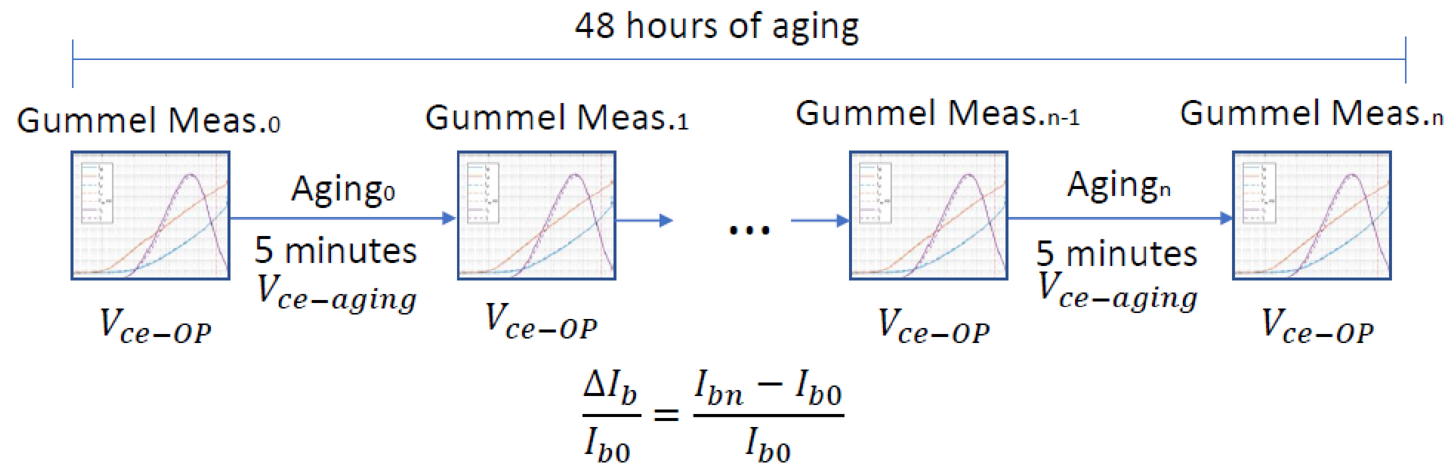
https://1drv.ms/b/s!Aosd9whger-2jOZDORuu_itSFx8wEg?e=xz0KYh

Reliability: BFP640 SiGe BJT (1)



Hot Carrier Effects:

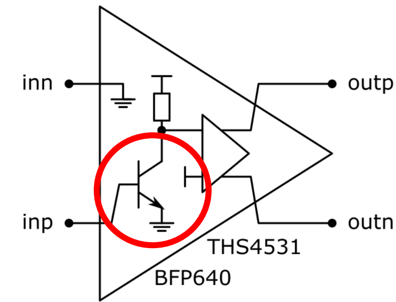
- Tested at Milano-Bicocca
- Operating conditions: **VCE=1.1V**, IC=0.4 mA → VBE≈1V (77K)
- Stress (aging) conditions: **VCE=6.5V-7.0V** , IC≈0.4 mA (VBE set to 1.03 V)
- Degradation criterion: 10% increase in base current (decrease in beta)



$$\frac{\Delta I_b}{I_{b0}} = \frac{I_{bn} - I_{b0}}{I_{b0}}$$

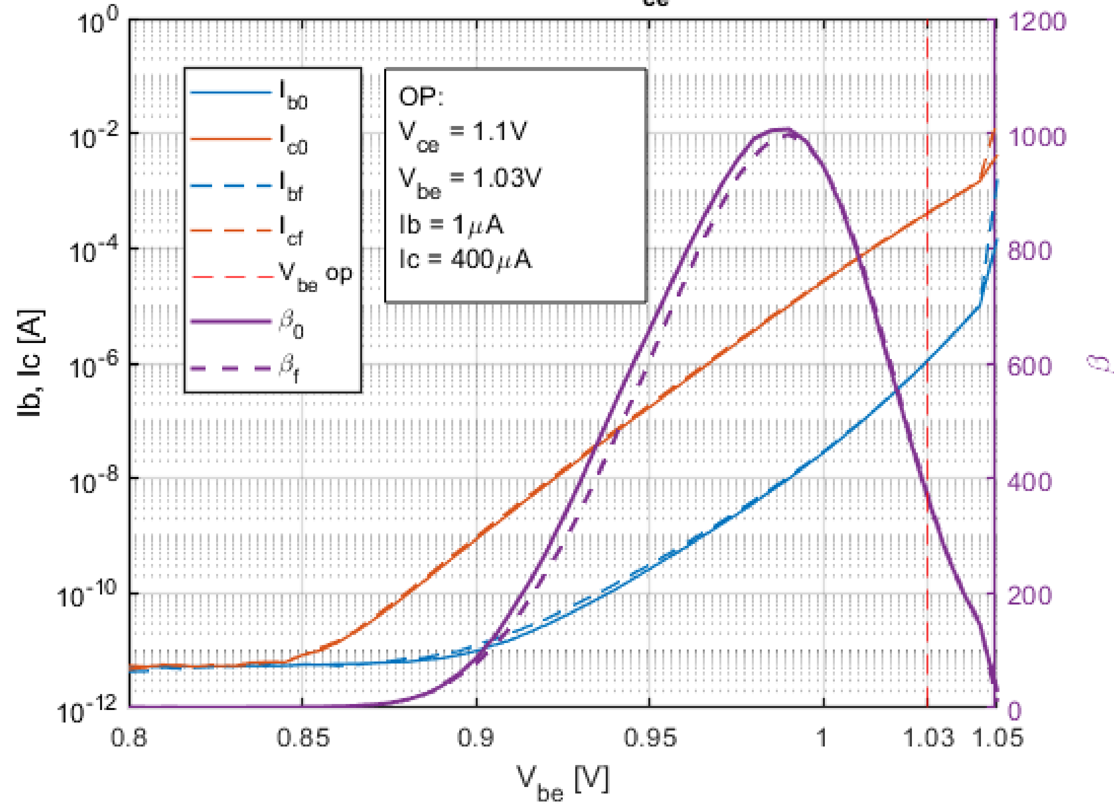
BFP640

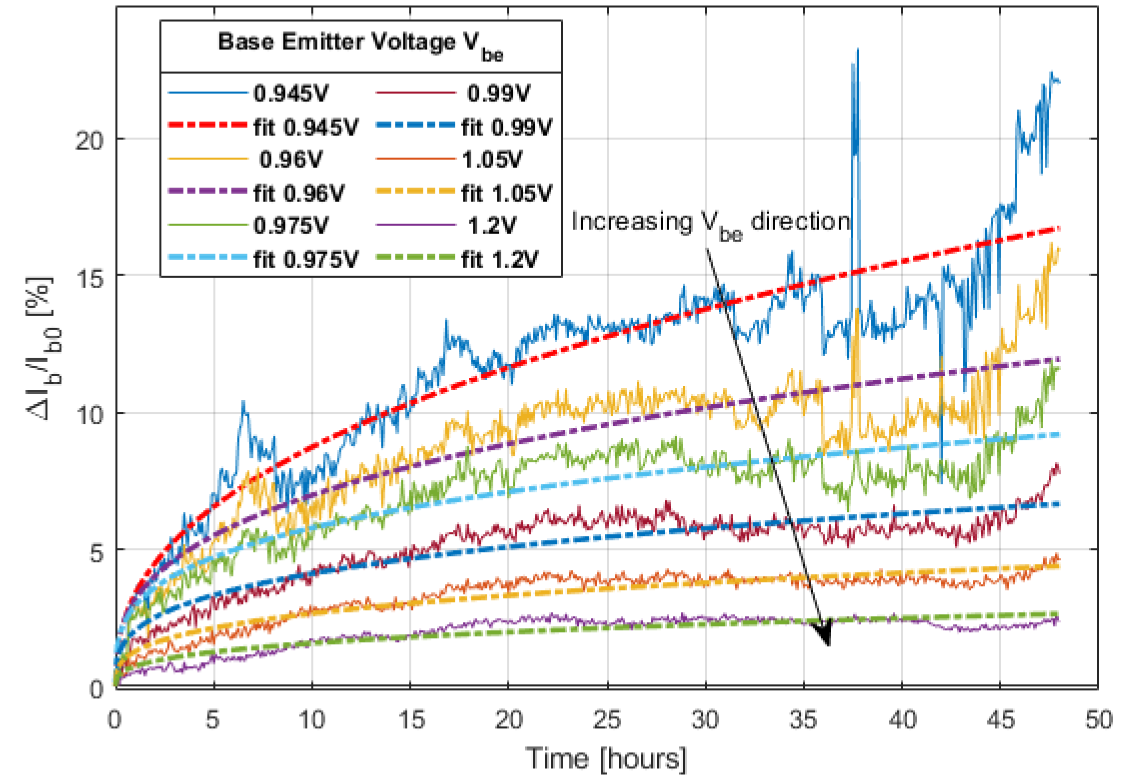
Reliability: BFP640 SiGe BJT (2)



Hot Carrier Effects:

- Degradation in beta is seen at lower currents (below IC≈0.01 mA)
- Hard to see any effect at the operating point (IC=0.4mA, VBE=1.03V)

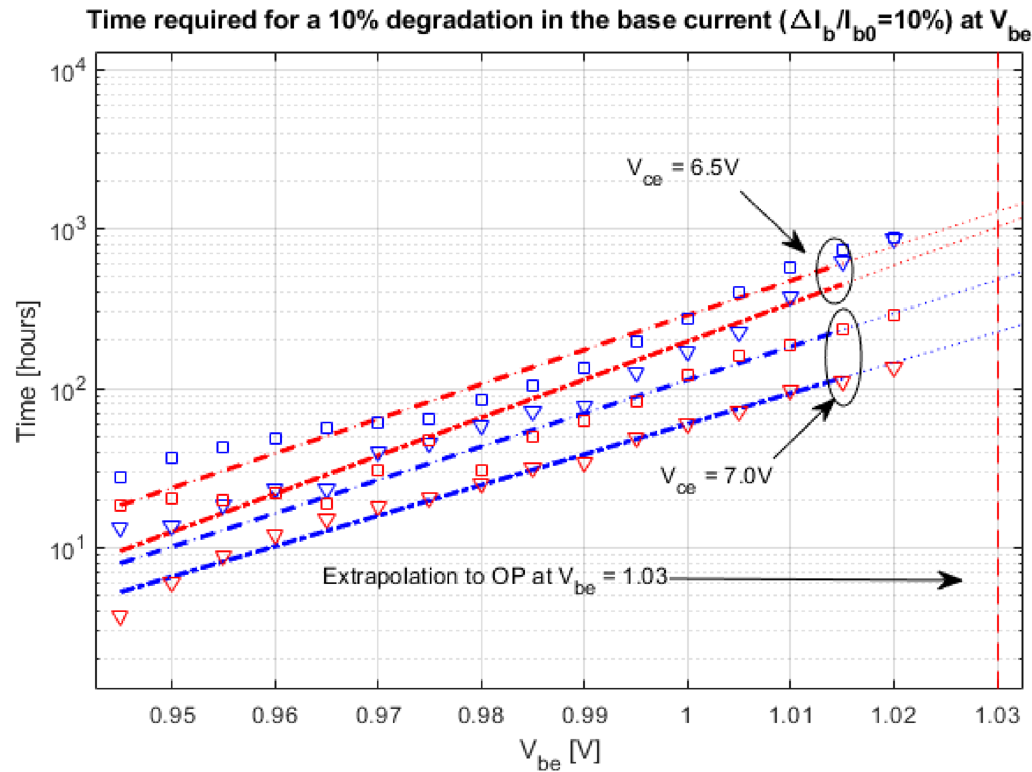


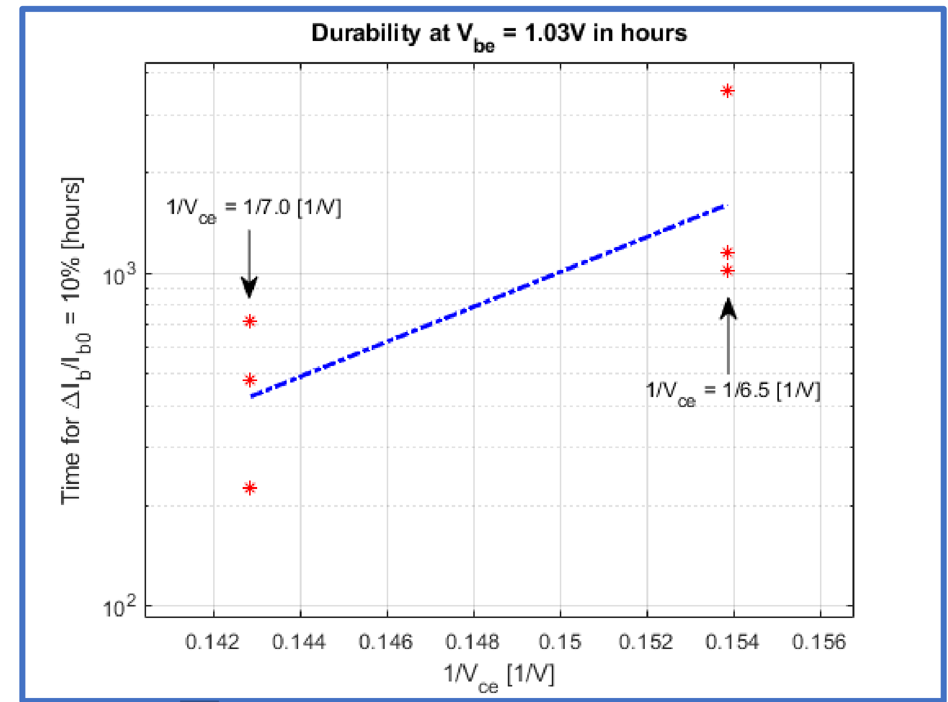


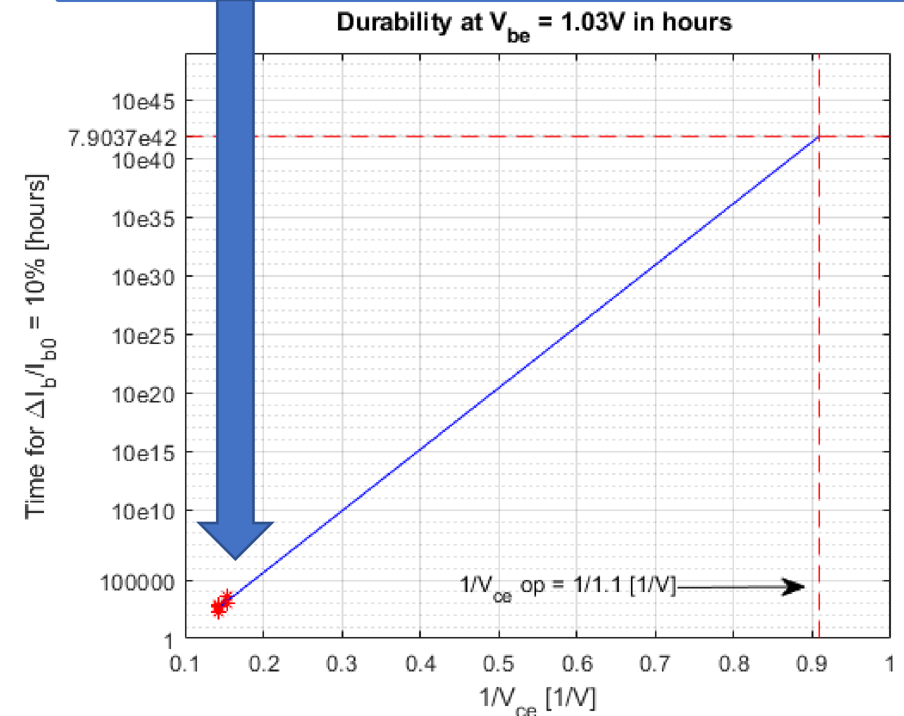
Reliability: BFP640 SiGe BJT (3)

Hot Carrier Effects:

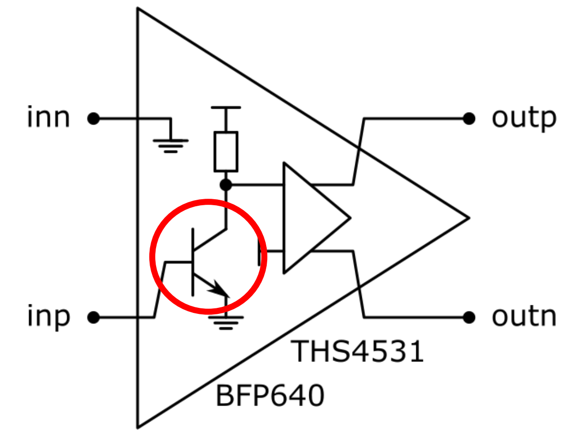
- First extrapolation: from lower current to operating current
- Second extrapolation: from aging 1/VCE to operating point
- (measurement repeated on 3 BJT samples)
- Result: **10^{42} hours lifetime** at the operating point







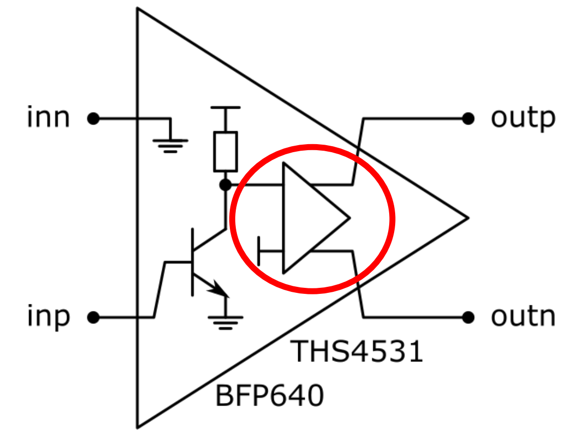
Reliability: BFP640 SiGe BJT (4)



ESD sensitivity:

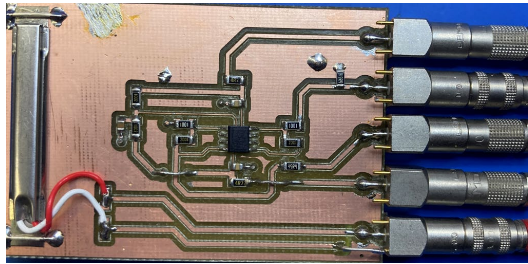
- The base terminal of the BJT is the input node of the circuit
- Standard ESD precautions are advised
- Schottky diode protects from reverse VBE

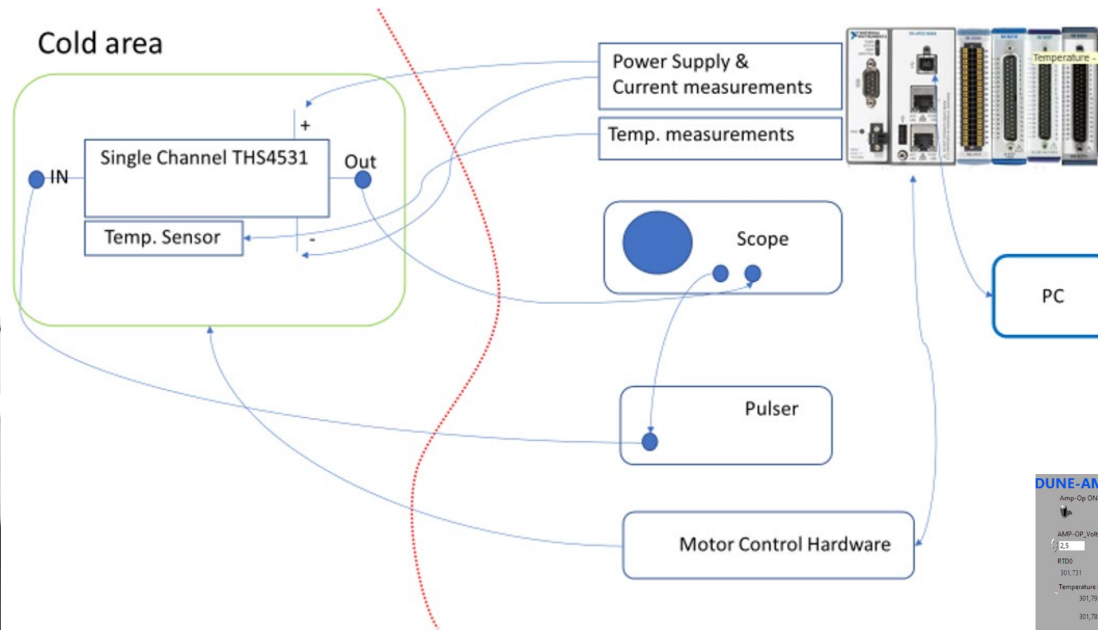
Reliability: THS4531 CMOS opamp (1)

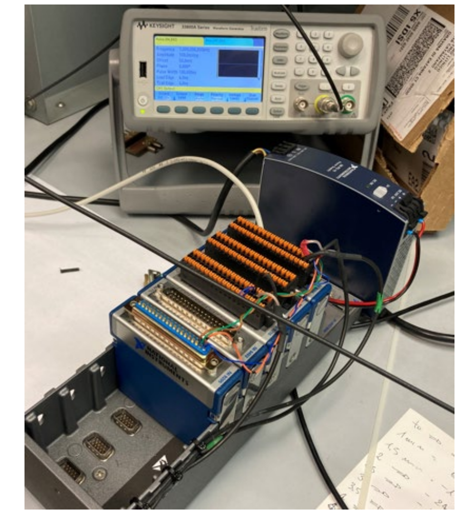


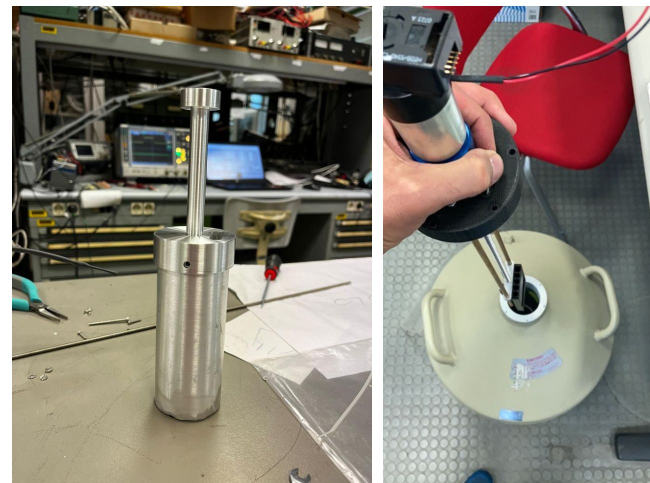
Hot Carrier Effects:

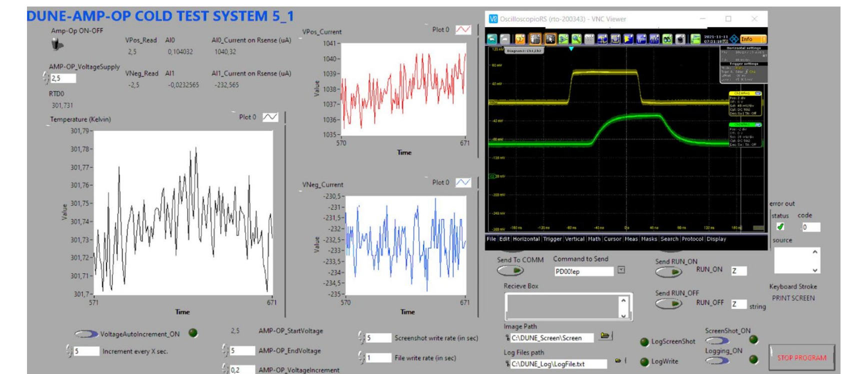
- Automated setup for lifetime VS operating voltage at INFN LNS (Catania)
- THS4531 mounted on a dedicated PCB
- Measurement of supply currents with NI cRio-9364 system
- Monitoring of signals & bandwidth with oscilloscope



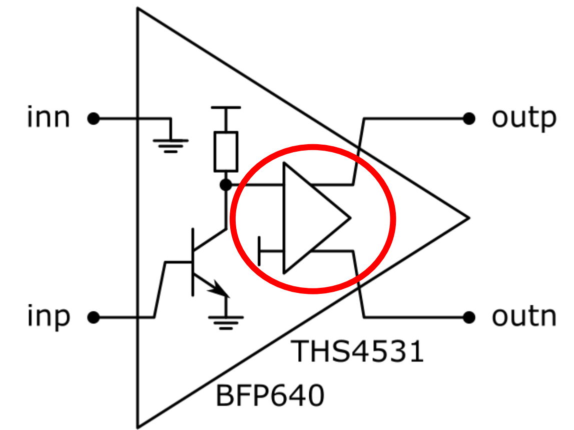






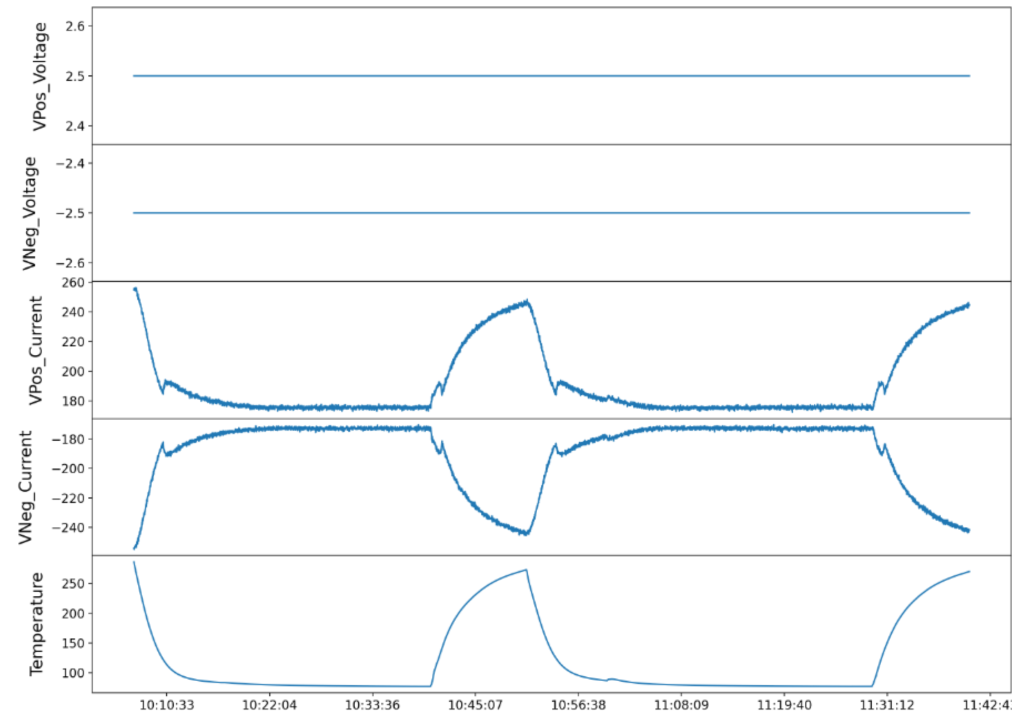


Reliability: THS4531 CMOS opamp (2)

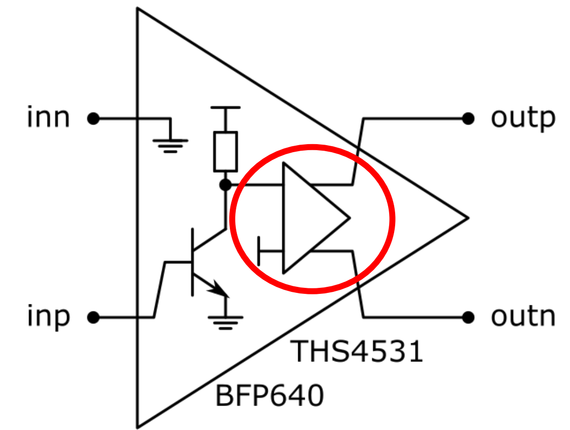


Hot Carrier Effects:

- THS4531 draws 0.25 mA at 300K, 0.18 mA at 77K
- Look for 1% supply current variation as degradation criterion
- Ample margin: **component is rated up to 5.5 V, and operated at 3.3V**
- Measurements still in progress

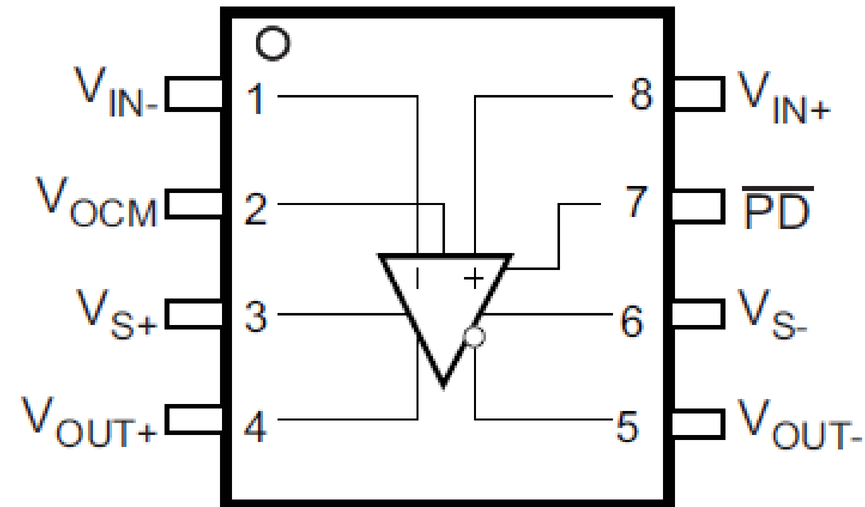


Reliability: THS4531 CMOS opamp (3)



Power down pin:

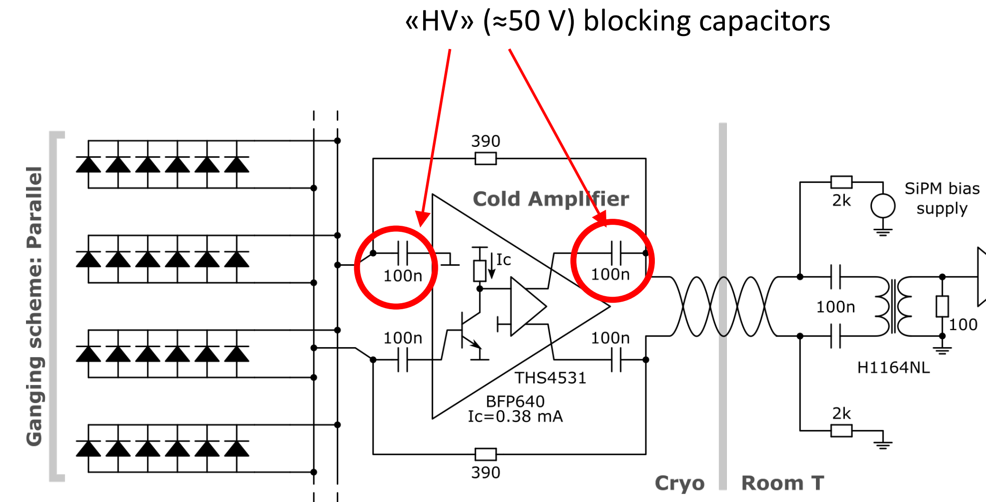
- The amplifier has a «power down» pin, which must be tied to Vcc
- At 300K, enable threshold is 2.1 V
- At 77K, operation below Vcc≈2.8V resulted in some (≈30%) devices not exiting power down
- VCE=3.3 V has been enough for all (≈100) opamps used so far



Reliability: passives and PCB

Capacitors

- Multilayer ceramics, C0G dielectric, as generous voltage rating as possible
- «HV» capacitors (AC coupling at the amplifier input/output):
  100 nF, 100 V C0G ceramics in 1206 package
  (TDK C3216C0G2A104J160AC)
- SiPM bias up to ≈55 V at 300K and ≈45 V at 87K →**Vop ≈ 50% Vmax**
  (values for Hamamatsu model; FBK operates at lower voltage)



Resistors

- All thin metal film, low thermal coefficient
- Low currents, not critical

Interconnects, soldering, PCB

- Multiple thermal cycles to check failures due to thermal contraction and stress
- Not yet done as a dedicated test, but amplifier prototypes have been cycled hundreds of times in several labs
- No issue ever observed related with thermal cycling
- Dedicated test foreseen at INFN LNS (Catania)

Beyond FD1-HD

Ganging up to 96 SiPMs

- FD1-HD baseline amplifier
- All SiPMs in parallel (FBK 50um TT)

Signal/Noise

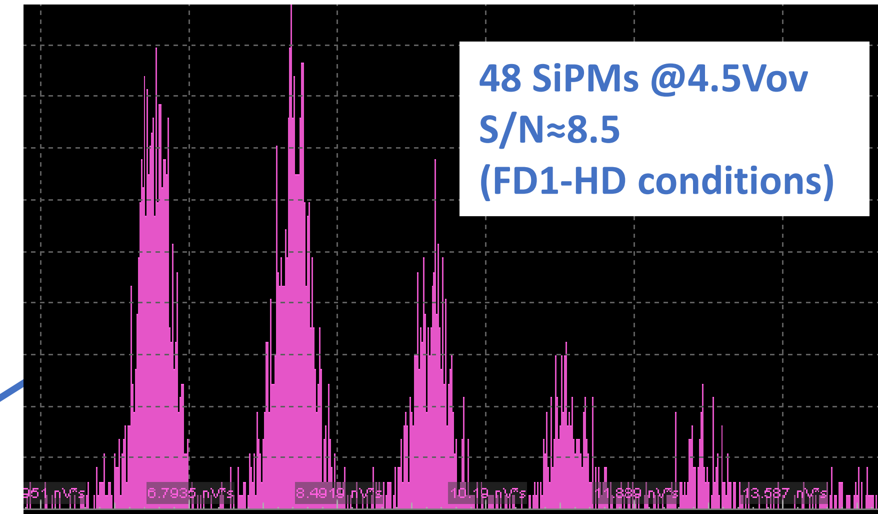
Total number of SiPMs

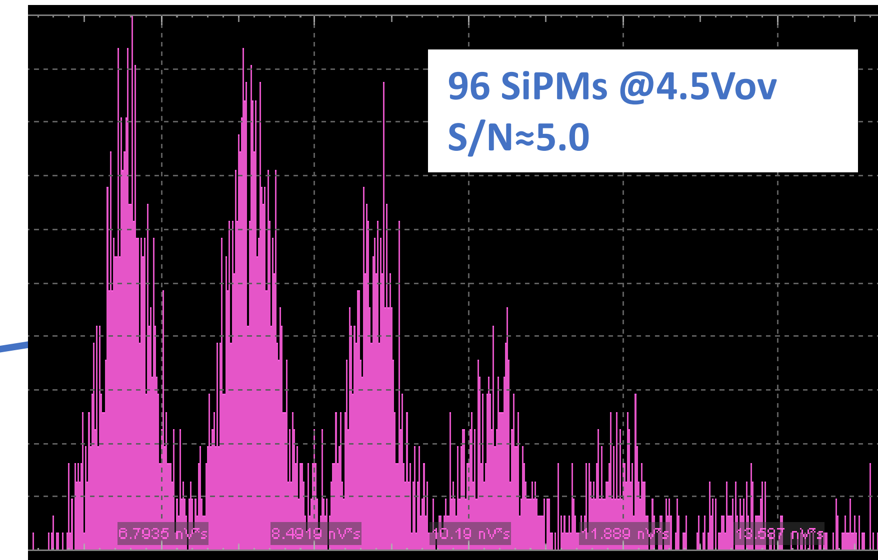
M par amp1 3.5Vov
C par amp1 3.5Vov
M par amp1 4.5Vov
C par amp1 4.5Vov
M par amp1 7.0Vov
C par amp1 7.0Vov

Vov=7.0V
PDE 50%

Vov=4.5V
PDE 45%

Vov=3.5V
PDE 40%

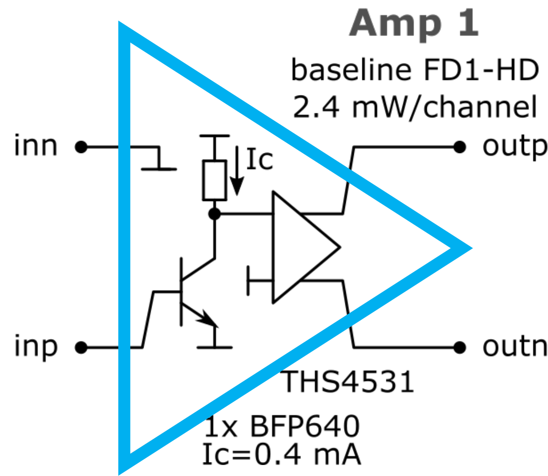


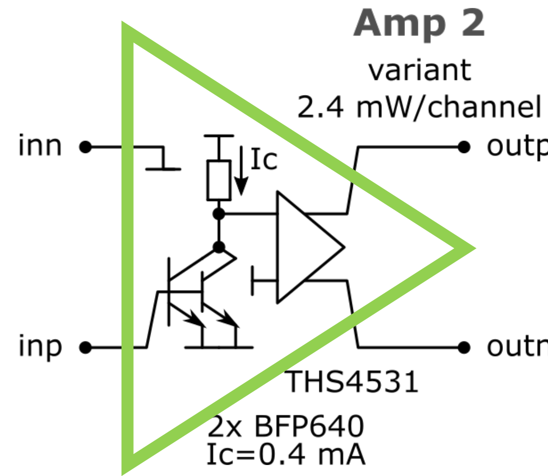


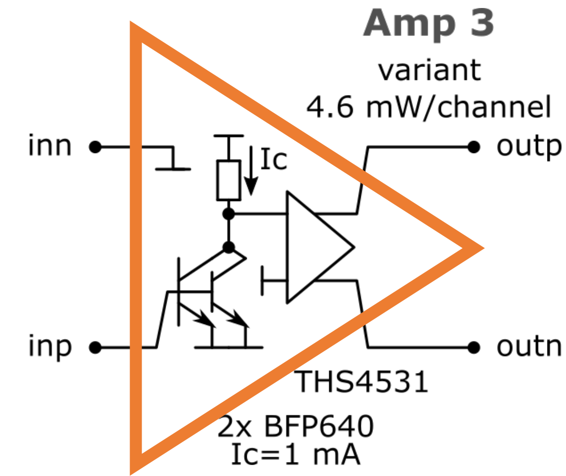
Amplifier variants

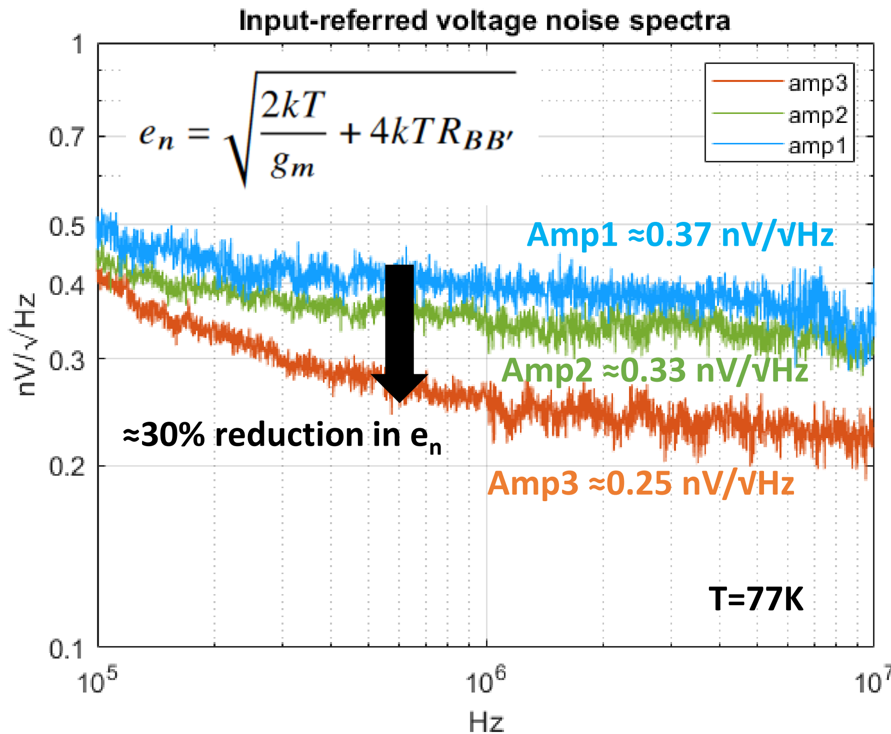
Paralleled BJTs: low mismatch was assumed for these tests.

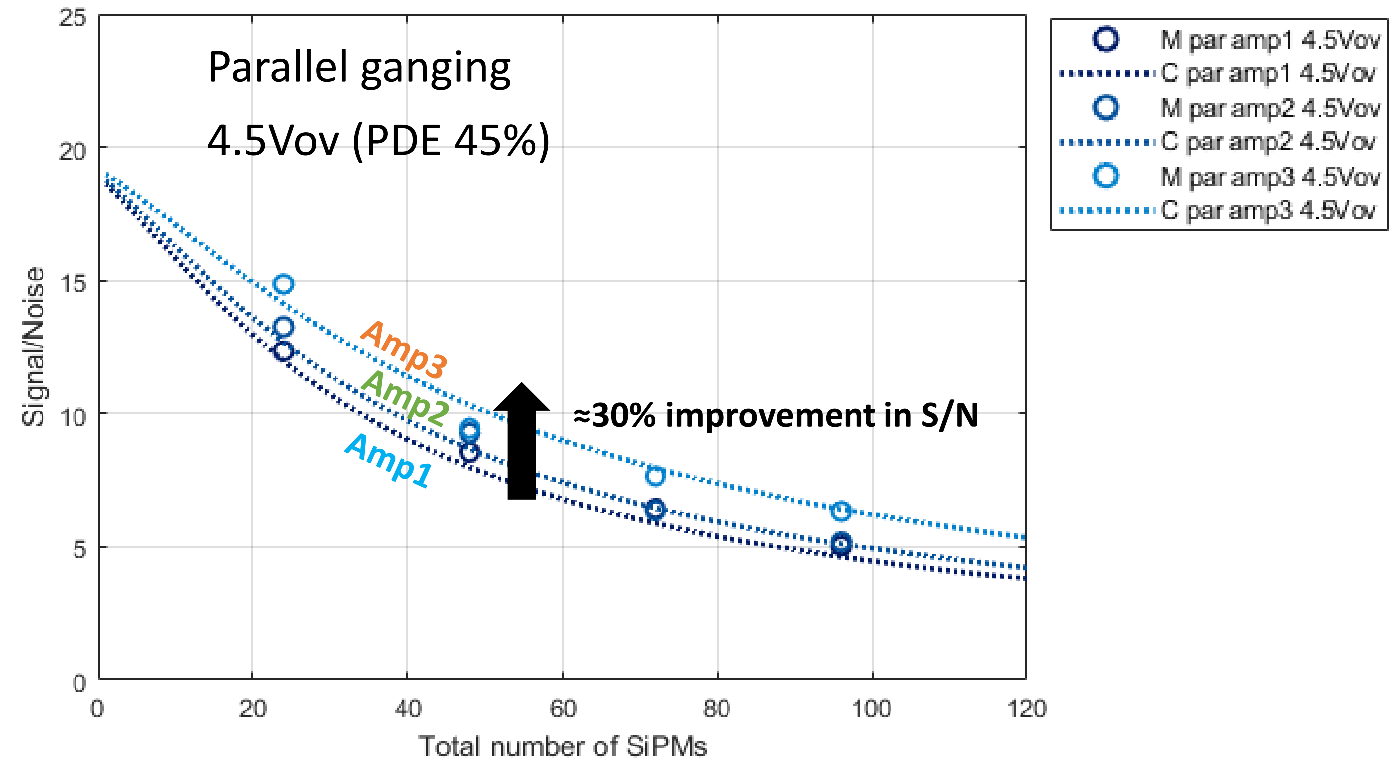
Dedicated tests are foreseen to measure the spread in VBE at a given IC, VCE





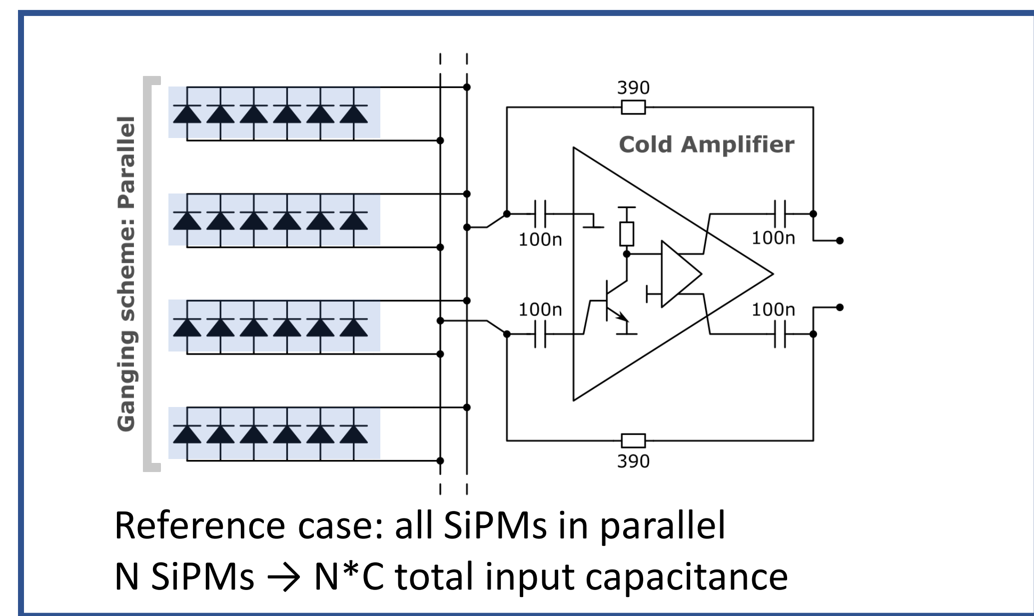




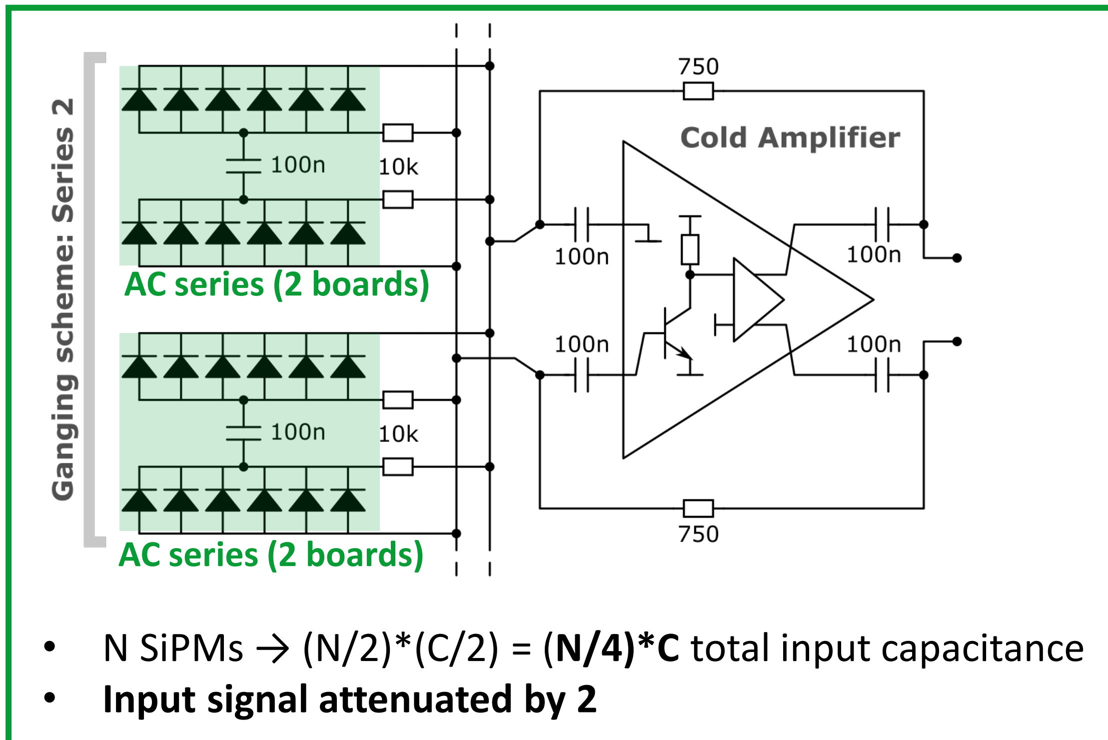


Hybrid ganging schemes

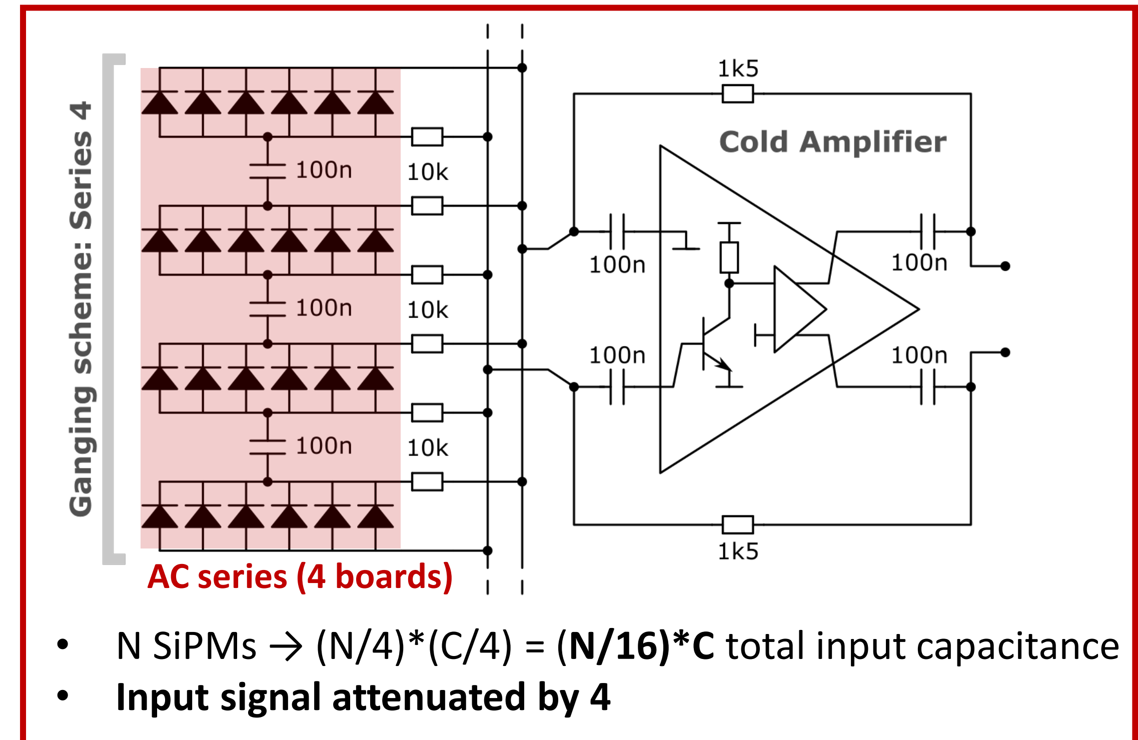
- Scheme developed by the Fermilab group for the FD2 PD
- SiPM boards in series (AC only) in groups of 2 or 4
- Feedback resistor adjusted to compensate input attenuation and keep the output amplitude constant
- Input signal/Capacitance ratio increases by 2 or 4



Reference case: all SiPMs in parallel
N SiPMs → N*C total input capacitance



- N SiPMs → (N/2)*(C/2) = **(N/4)*C** total input capacitance
- **Input signal attenuated by 2**

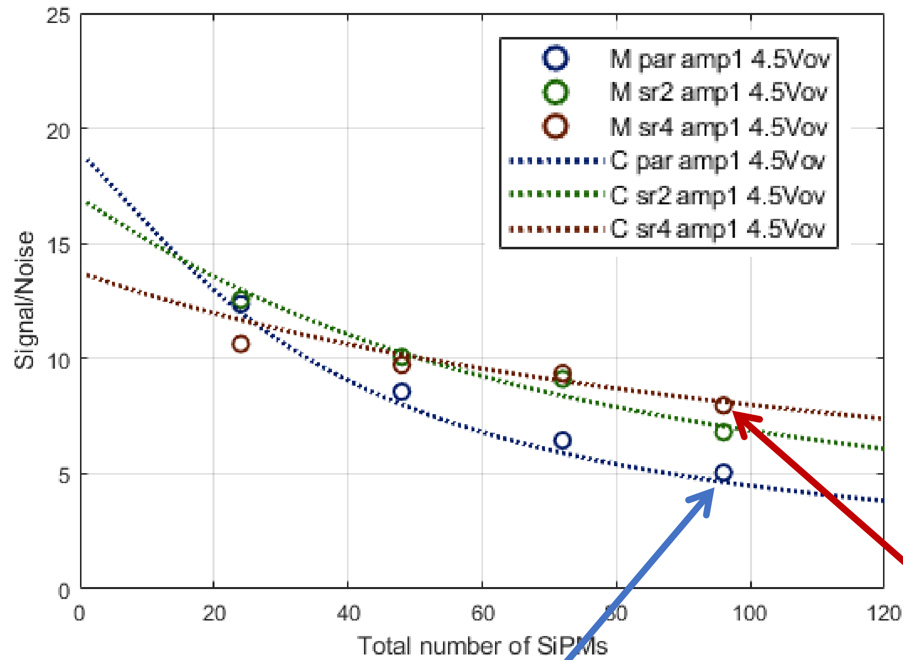


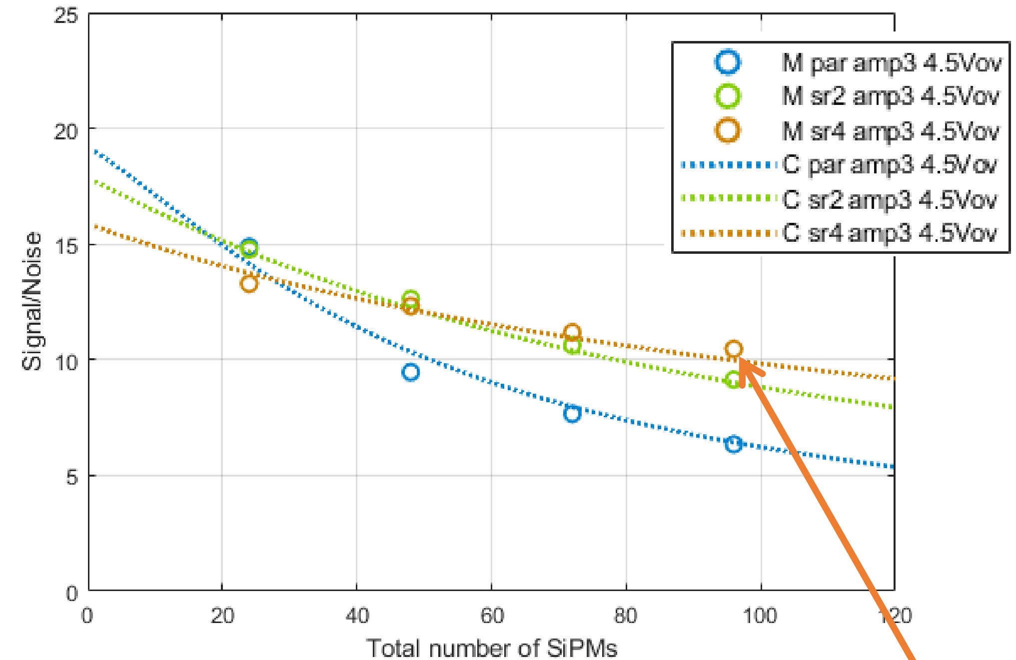
- N SiPMs → (N/4)*(C/4) = **(N/16)*C** total input capacitance
- **Input signal attenuated by 4**

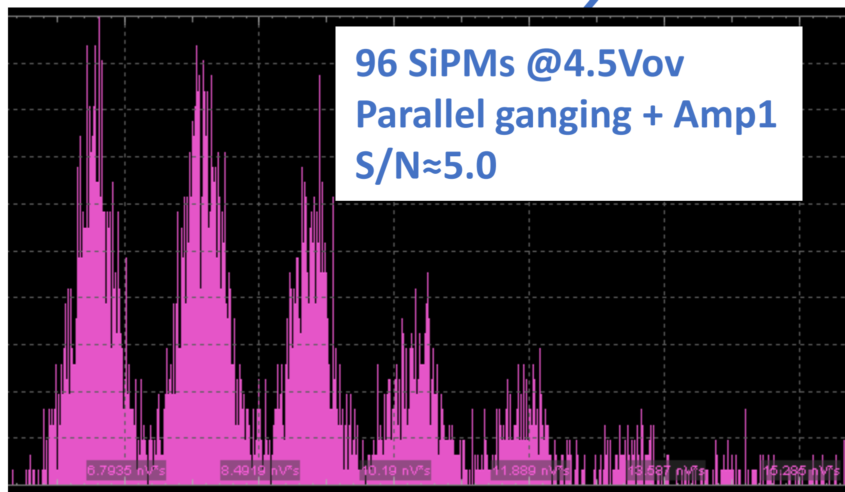
Hybrid ganging results (1)

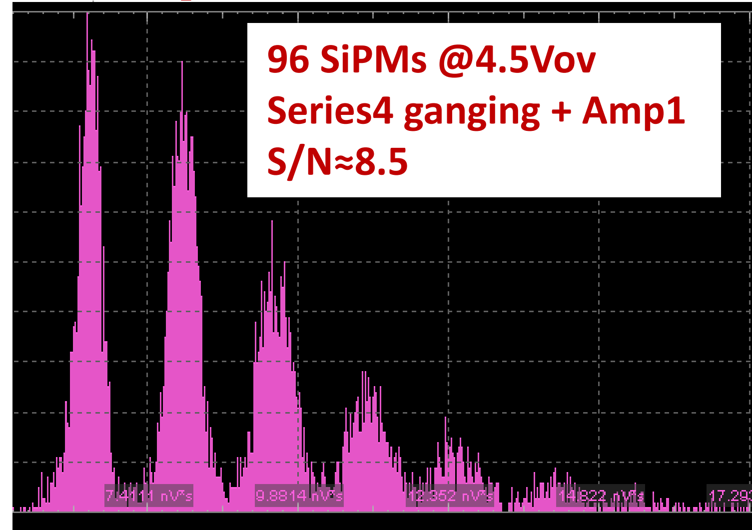
Amp1 (FD1-HD baseline, 2.4 mW/channel)

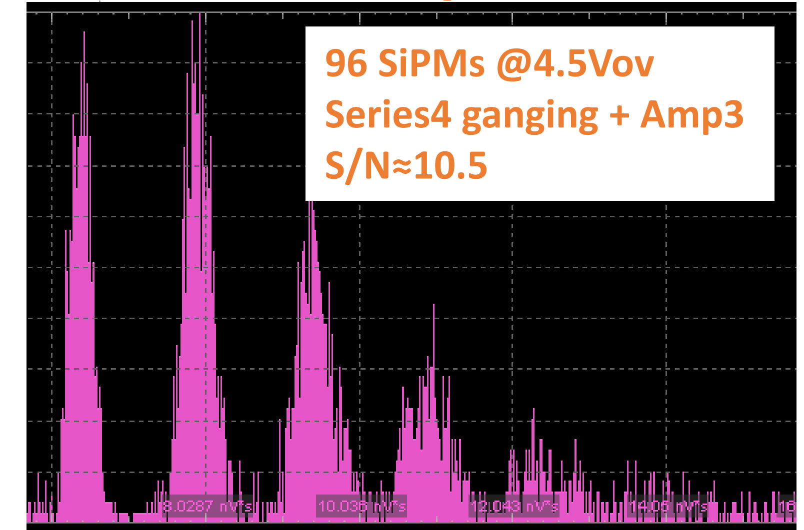
Amp3 (variant, 4.6 mW/channel)







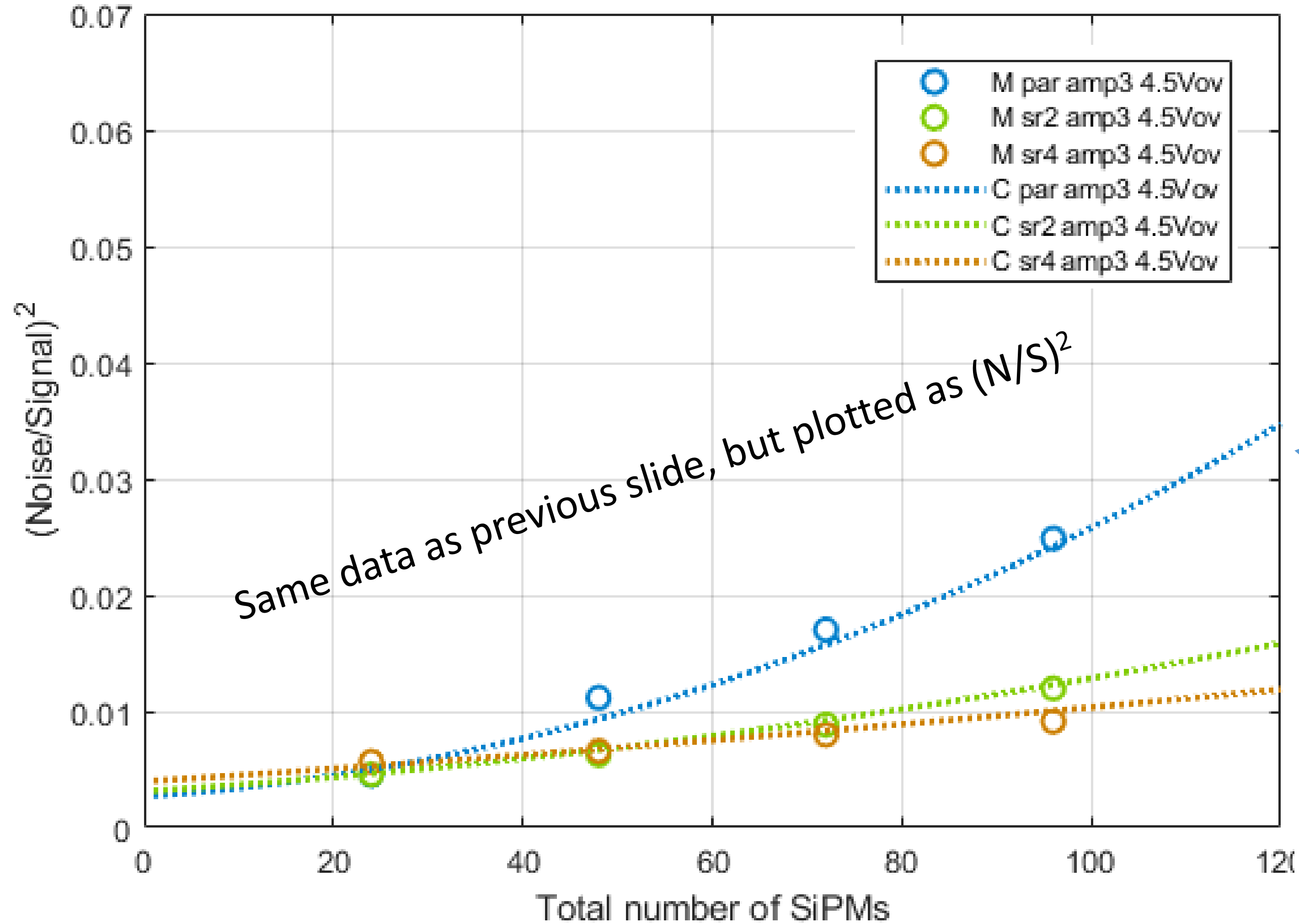




Hybrid ganging results (2)

$$(N/S)^2 = \frac{e^2}{V_{ov}^2 4\tau}\left(\frac{e_n^2 N^2}{G} + 4kTNR_q\right)$$

Amp3 (variant, 4.6 mW/channel)



e_n: white series noise of the amplifier

N: total number of SiPMs

G: ganging configuration
(=1 for parallel, =2 for «series 2», =4 for «series 4»)

Rq: quenching resistance of 1 SiPM
(250 Ω for a 6x6 mm^2 FBK TT)

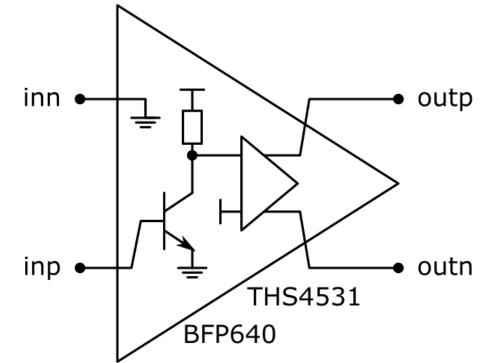
All SiPMS in parallel:

- Amp noise e_n dominates
- $(\text{Noise})^2 \propto (\text{Number of SiPMs})^2$

AC series ganging in groups of 4:

- Thermal noise of R_q dominates
- $(\text{Noise})^2 \propto$ Number of SiPMs

Wrap up



- DUNE FD1-HD PD cold amplifier design based on discrete SiGe BJT + CMOS opamp for low series noise at low power (≈0.4 nV/Hz at 2.4 mW/channel)
- Design satisfies requirements for FD1-HD PD
- Obtained S/N≈8 with 48 Hamamatsu and FBK SiPMs, all in parallel, Vov=4.5V
- Realibility of SiGe transistor tested with success
- Results on estimated lifetime of CMOS opamp expected soon (optimistic feelings due to Vop = 0.6 Vmax)

- Amplifier variants developed for lower noise (down to ≈0.25 nV/Hz at 4.6 mW/channel)
- Successfully tested with hybrid ganging schemes
- Obtained S/N≈10 with 96 SiPMs (FBK 50um TT), AC series in groups of 4, Vov=4.5V