VD PD Digital Readout Breakout Meeting Notes

April 21, 2022

Notes from last week's workshop

- Power is the main issue.
- We can't make a lot of use of the 16 channels.

CURRENT CONSUMPTION WITH JESD INTERFACE ENABLED				
I_{JESD}	Supply currents: JESD204B interface enabled, LVDS interface disabled at 12-bit, 80-MSPS, 4 ADCs per lane mode	AVDD_1P8 current(1)	170	mA
		DVDD_1P2 current(1)	260	
		DVDD_1P8 current(1)	40	
P_{JESD_CH}	Power dissipation in active mode per input channel: f_C = 80 MSPS, 12-bit mode, LVDS interface disabled, JESD interface enabled (4 ADCs per lane mode)	16-channel input mode	43.1	mW/channel
		32-channel input mode	21.6	

Figure 36. Total Power vs Conversion Clock Frequency

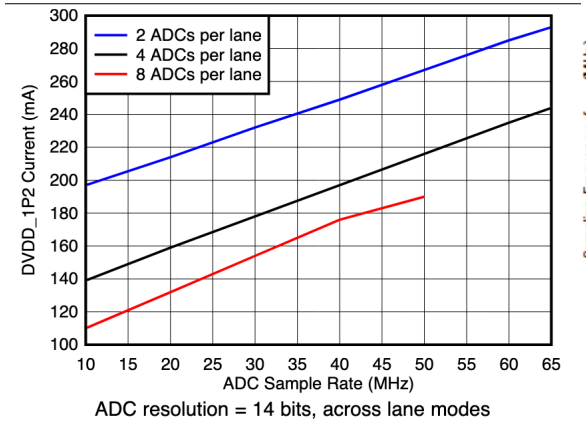

Figure 46. DVDD_1P2 Current vs ADC Sample Rate

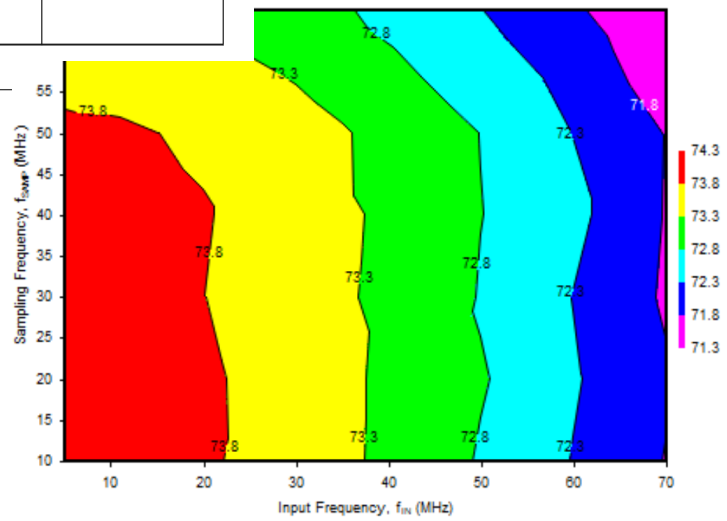

Figure 54. Signal-to-Noise Ratio in 14-Bit, 16-Input Mode

Next steps

- Measure the power draw on the CDR for each voltage.
- Test the power in the cold (we need this number)
- Look at the other parts.
- Ideal, 8 channels (one output) without any control.
  - (target middle Cathode module and membrane)
  - On the boarder, 2 channels max.