

# DUNE timing system (DTS) update

Stoyan Trilov

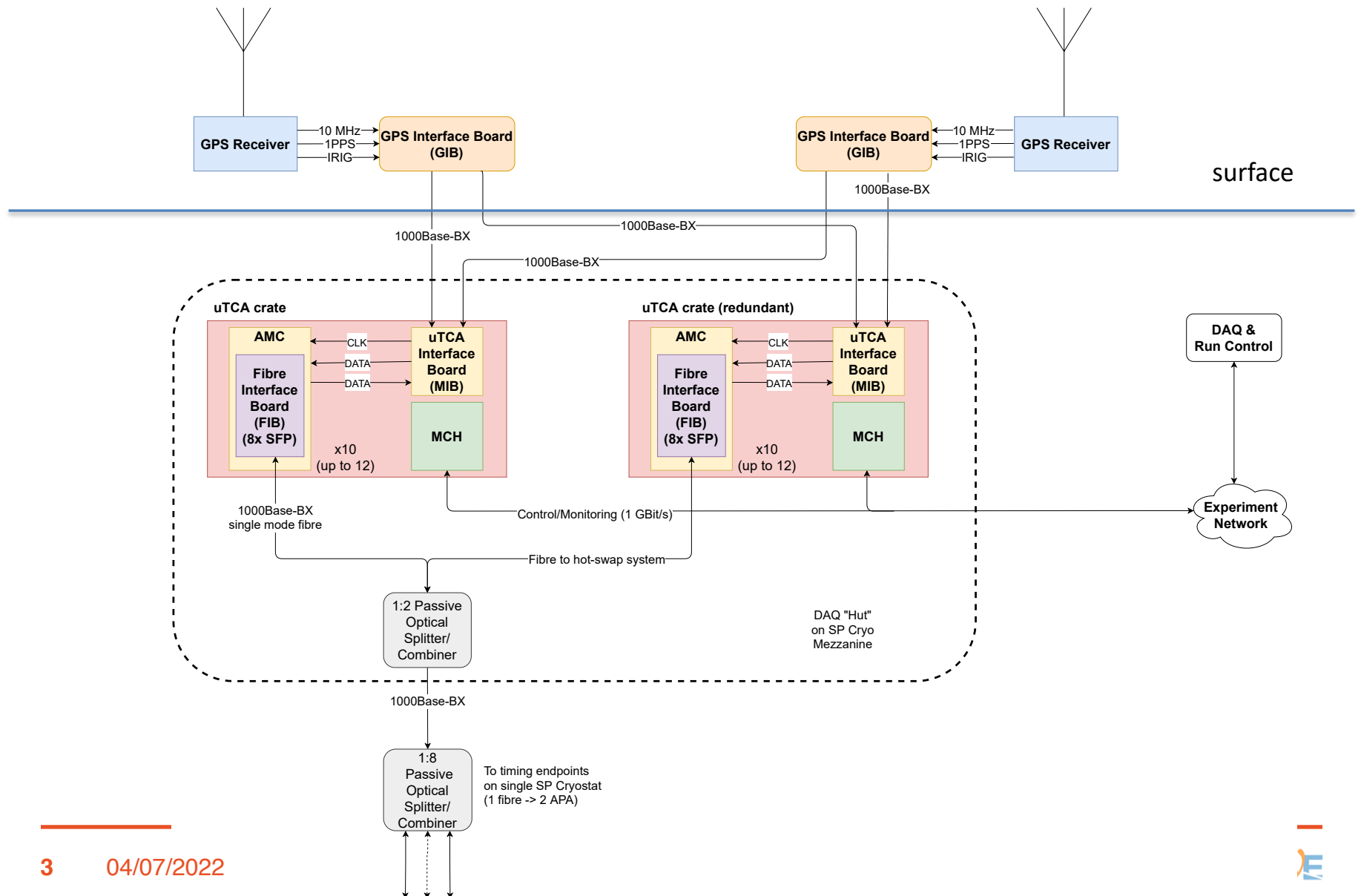
DUNE UK meeting

04/07/2022

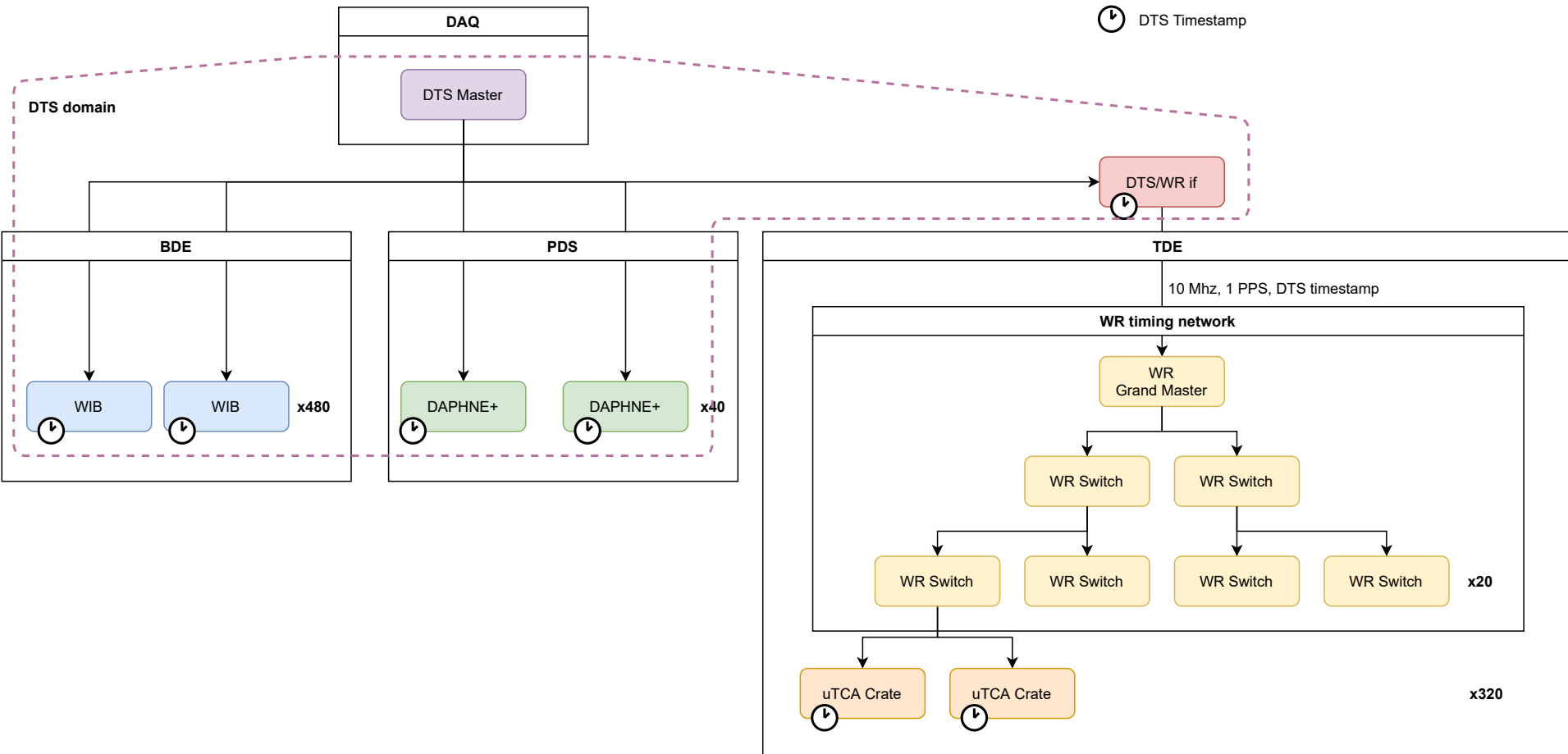
# Content

- DTS design reminder
- Hardware
- New protocol/data-encoding
- Software
- DTS-WR for vertical drift coldbox
- Regression testing
- 2022

# Timing system – HD module



# Timing system – VD module

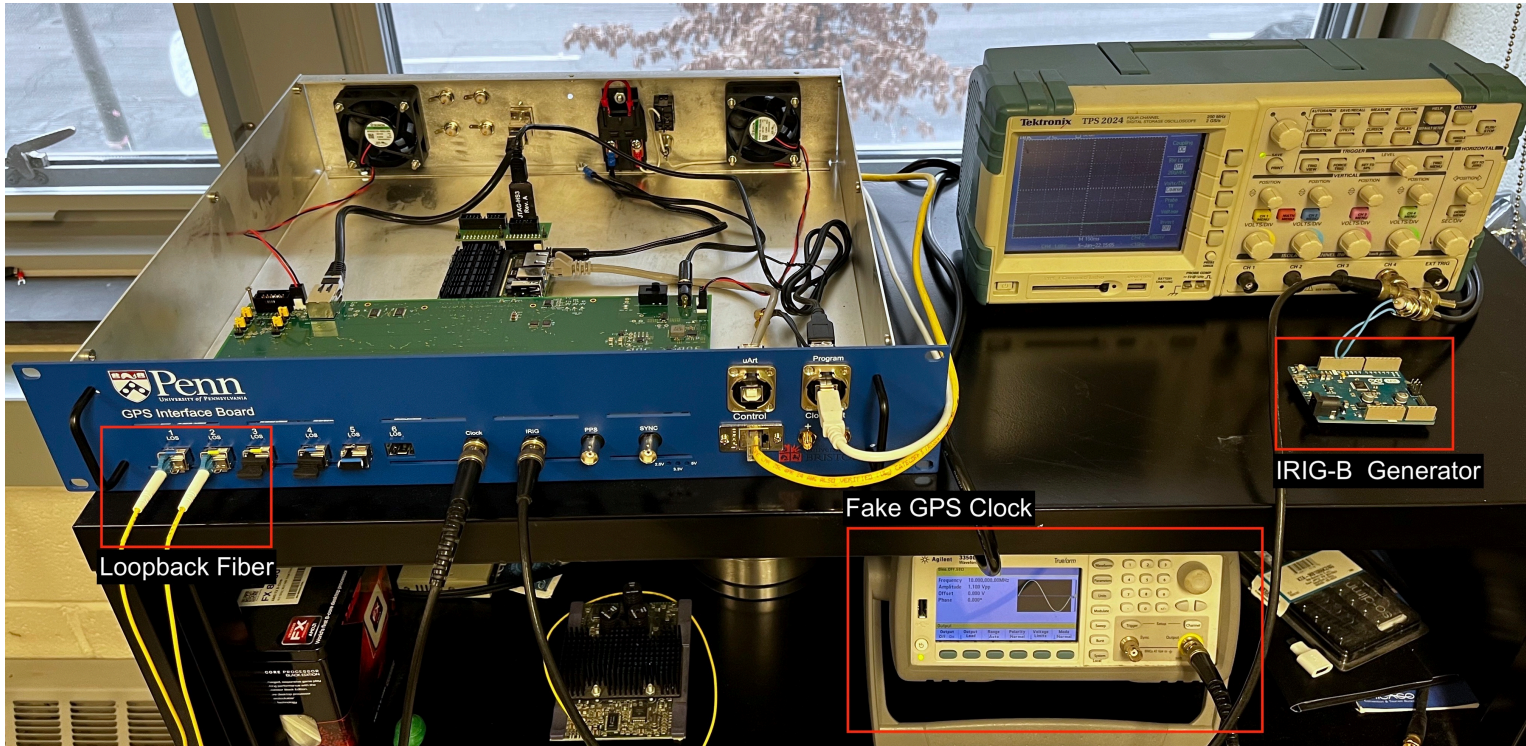


# Timing system custom hardware reminder

- **GPS interface board (GIB):**
  - Receives clock and time from GPS receiver
  - Generates DUNE timing system timestamp
  - Transmit to MIB using the DTS protocol
- **uTCA interface board (MIB):**
  - Receives data-stream from GIB
  - Fan out clock and data to FIBs (via the AMCs)
- **Fibre Interface Board (FIB):**
  - An FMC with 8 SFP modules
  - Hosted by an AMC in a uTCA crate
  - Fans out timing data-stream to timing endpoints

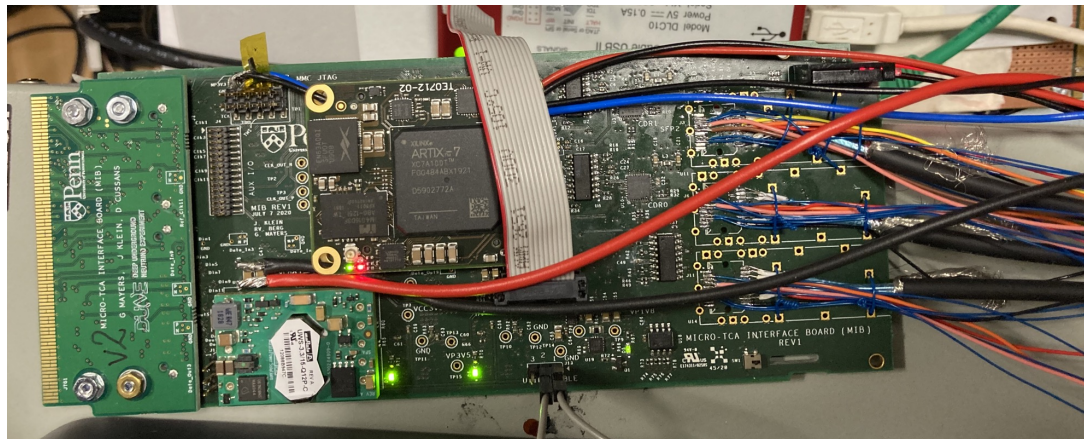
# GIB status

- **Board prototypes fabricated, assembled, and commissioned at Penn**
- **Prototype firmware tested in hardware**
- **IRIG decoder tested in simulation**



# MIB status

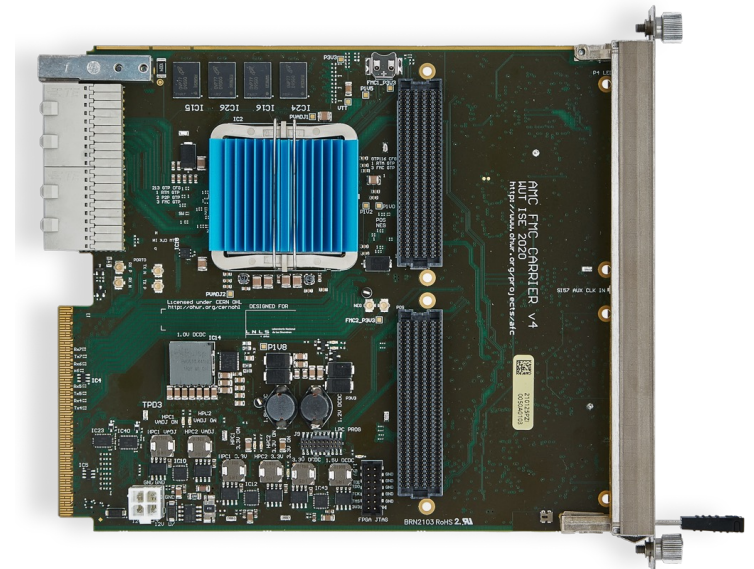
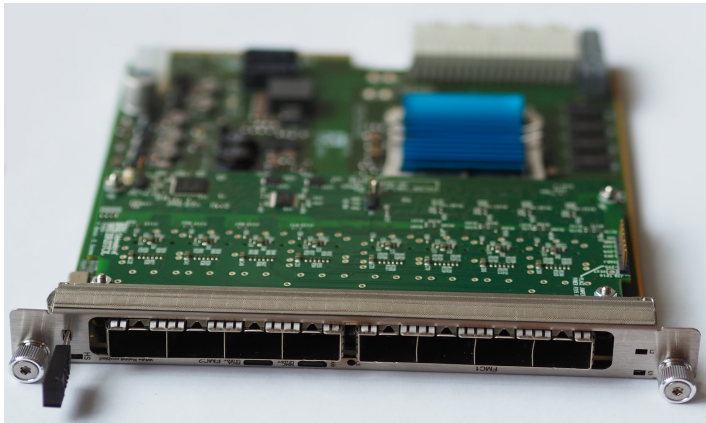
- **Four prototypes fabricated and assembled**
  - Hardware fixes required to allow board operation for PD-II
  - List of changes for next hardware version assembled
- **First firmware version released in DUNE DAQ v3.0.0**
  - Downstream (MIB->FIB+AFC->Endpoint) data and clock path verified
  - GIB -> MIB data and clock path to be debugged
  - AFC+FIB -> MIB (return) data path to be debugged
  - uTCA module management firmware needs testing





# FIB+AFC status

- **Two FIB prototypes fabricated/assembled**
  - Tested and operated at Bristol
    - Some models of SFP do not respond over I2C – to be investigated
    - CDR-less version will need to be produced
  - **Downstream clock+data path of uTCA backplane -> FIB+AFC verified**
    - AFC required hardware modifications to work
    - New AFC version needs testing





# New protocol/data-encoding

- **New Duty Cycle Shift Keying (DCSK) data-encoding firmware developed**
  - No need for physical CDR chip
  - Long term stability of master <-> endpoint demonstrated
  - Backwards compatible with CDR hardware
- **New timing protocol firmware developed**
  - Expand endpoint address to 16b
  - Change partitioning scheme -> more partitions, increased flexibility
    - A “timing partition is now a logical construct, a group of timing endpoints with a particular configuration
  - Enhanced “variable-length” messages/commands
    - Read/write of arbitrary registers in endpoint from master
  - “alpha” release will be made available to electronics firmware developers in coming days
- **New CDR-less “timing FMC” design submitted for fabrication**

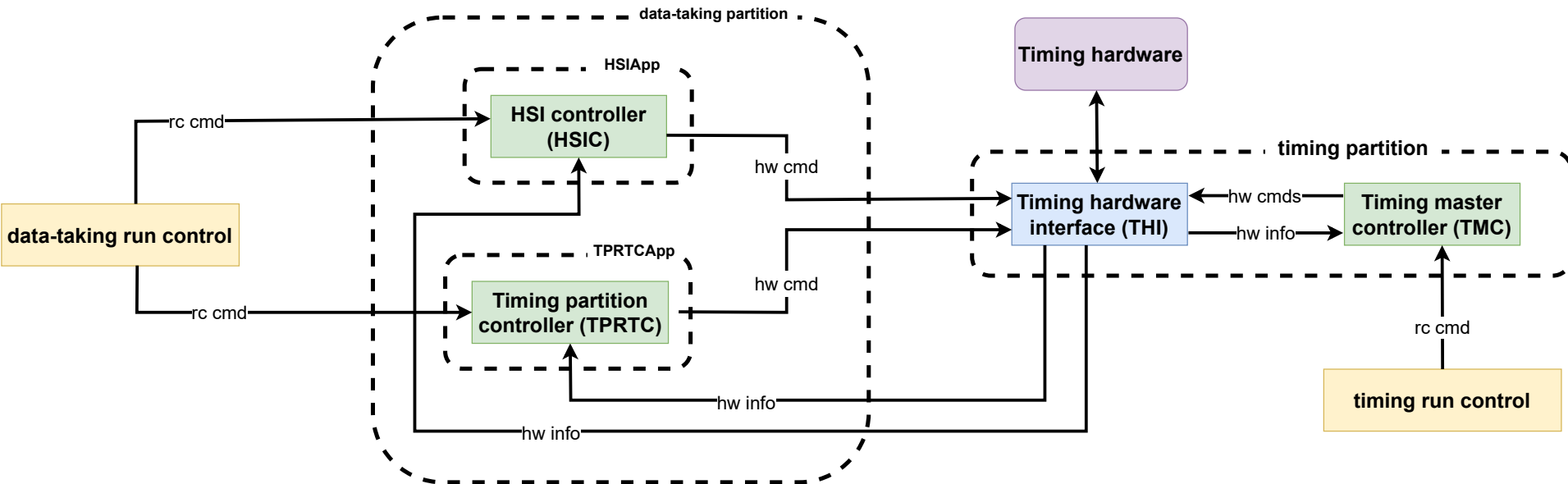
# Software

- **Recent developments (DUNE DAQ v3.0.0)**
  - MIB support
    - low level python tools + higher level application
  - Run control integration
    - Dedicated timing DAQ partition and run control instance
- **Upcoming features (v3.1.0)**
  - New protocol support
    - Low level python tools
- **Upcoming features (v3.2.0)**
  - New protocol support
    - High level applications and run control integration

# High-level timing software RC integration

- Timing master hardware is configured and monitored using applications running in a dedicated “timing” DAQ partition
- Partition specific timing hardware/firmware, e.g. HSI endpoints, timing partitions, are controlled and configured from the data-taking partition via the “timing” partition
- For each timing device, there is a specialised “TimingController” module which accepts higher level commands from run control and translates them into the relevant lower-level software calls
- TimingController modules send the lower-level commands to the TimingHardwareInterface (THI) module
- The THI makes the appropriate calls to the hardware via IPBus
  - Acts as a single gateway for control&configuration of timing hardware

# Timing software and RC information flow



# Timing software – new protocol support

- **New timing firmware will have different master and endpoint interfaces**
  - Plan to support both old and new firmware with the same software version
    - Keep software interfaces exactly the same where possible
      - -> maximum sharing of code
    - Ensure backwards compatibility of new software (C++ classes/python) with old(er) firmware
- **Concept of “timing partitions” will change quite significantly**
  - A “timing partition is now a logical construct, a group of timing endpoints with a particular configuration
  - Old firmware has dedicated partition controllers in master firmware
    - Partition configuration all done in master, endpoints are only assigned a partition
  - In new firmware, no ‘physical’ partition controller in master
    - Partition configuration all done in endpoints
    - Endpoint configuration will be done via commands issued by the master over the DTS data-link
    - New software interfaces between timing and DAQ partitions required

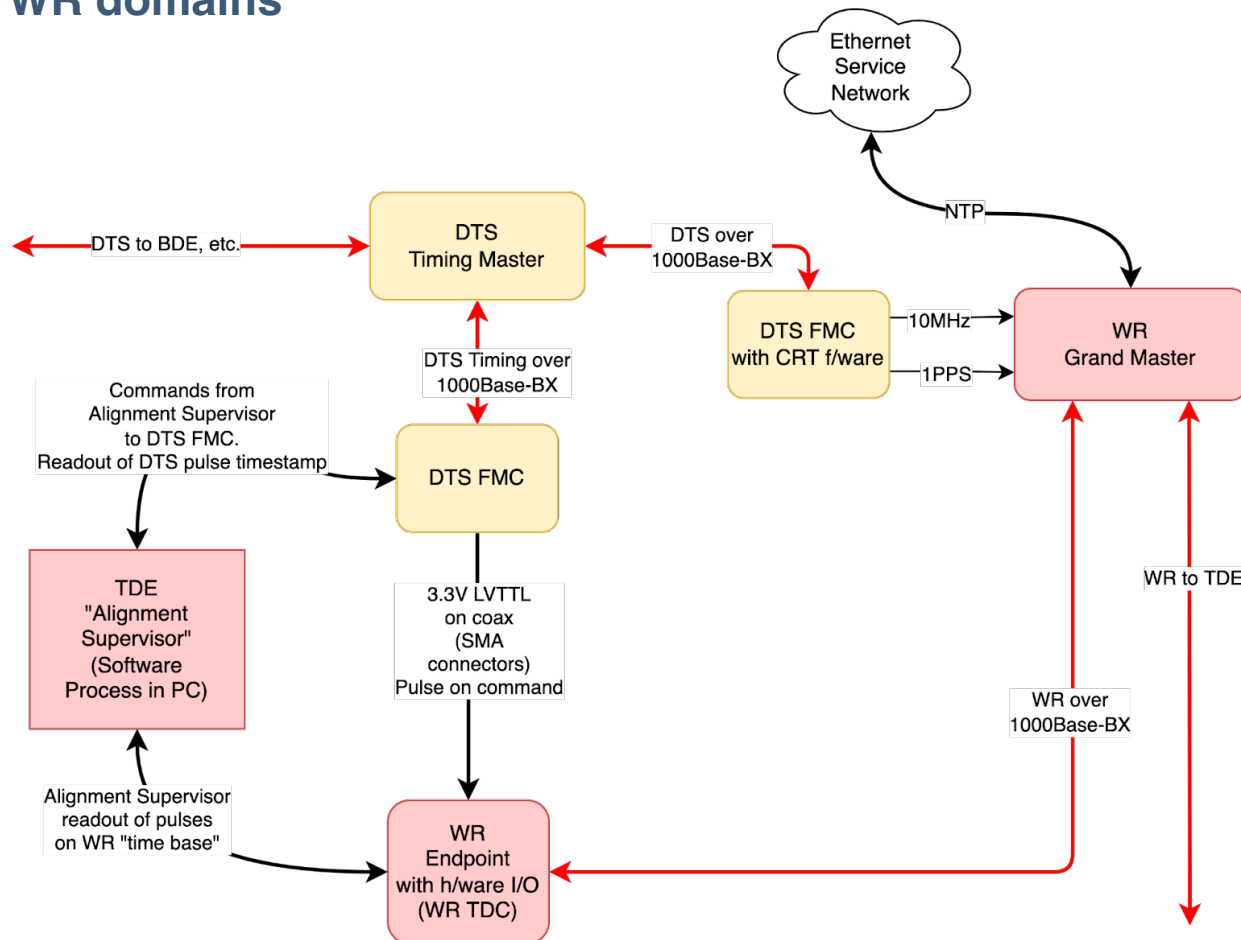
# Timing for Vertical Drift Coldbox

- **DTS provides a uniform interface to readout systems in DUNE**
  - Timing received by readout and transferred to “front ends”
- **Vertical Drift Top Electronics uses White Rabbit (IEEE-1588 2019) for synchronization**
  - Need to derive WR from DTS, and synchronise the two systems
- **DTS→WR interface under design**
  - Proof-of-principle tests conducted to show that WR can be synchronized from DTS (see back-up slides)
  - In discussions with VD TDE



# Possible VDC synchronisation scheme

- Synchronisation based on hardware pulse(s) whose time is sampled in the DTS and WR domains



# Testing of hardware/firmware/software

- **A testing framework developed allowing regression testing**
  - Regression testing ensures nothing has broken when new functionality is added
    - Test new hardware with “known good” firmware + software
    - Test new firmware with “known good” hardware + software
    - Test new software with “known good” hardware + firmware
  - Test point-to-point timing links
    - Master and endpoint
    - Will expand to multi-level ( GIB → MIB → AFC/FIB → Endpoint )
- **Tests that can be performed so far**
  - Clock generation correct (PLL lock, frequency)
  - SFP (optical fibre receiver) is active (Tx/Rx power levels)
  - Master generates timestamps.
  - Endpoint reaches “ready” status
  - HSI enabled devices correctly store signals in the buffer
  - Optical fibre round-trip times are correctly measured

# Testing plans

- **Automatically deploy tests as part of Continuous Integration**
  - Set up dedicated hardware setup
  - Have a CI “runner” at test lab (Bristol) that connects to CI system for timing repositories (firmware = Gitlab )
  - Run through a sequence of set-ups to check for regression introduced by firmware, software changes
- **Develop high level application integration tests**
  - Low level python tools only a small part of DTS functionality/codebase
  - High level DAQ applications sit on top timing low level library
    - These expose interfaces to run control and other DAQ application
    - Require extensive integration tests
  - Work on-going to develop a unified testing framework allowing automation of
    - Low level python tools regression testing
    - Standalone high level application testing
    - Integration testing with DUNE DAQ

# Timing in 2022

- Commission uTCA infrastructure, MIB+FIB at CERN – Q1/~~2~~**3** 2022
  - uTCA crate and FIB+AFC installed at CERN – Q2
  - A 2nd MIB to be commissioned (apply hardware fixes) and shipped to CERN – Q3
- Integrate MIB+FIB with detector electronics – Q~~2~~**3** 2022
- Roll out new protocol (and data encoding) – Q~~2~~**3** 2022
- Prototype and integrate DTS-WR interface at CERN – Q~~2~~**3** 2022
- Commission GIB at CERN – Q3 2022
- Continue to support existing Coldbox timing systems

# Summary

- **Hardware**

- New CDR-less "timing FMC" design submitted for fabrication
- MIB -> FIB+AFC -> Endpoint downstream path demonstrated

- **New protocol+data-encoding**

- Firmware and software in active development
  - In advanced stages of testing
  - Give "preview" version to developers in the coming days
- First release planned for DUNE DAQ v3.1.0
- Full integration planned for v3.2.0

- **DTS-WR interface**

- Interoperability demonstrated at the hardware level
- Discussions on-going

# Back-up

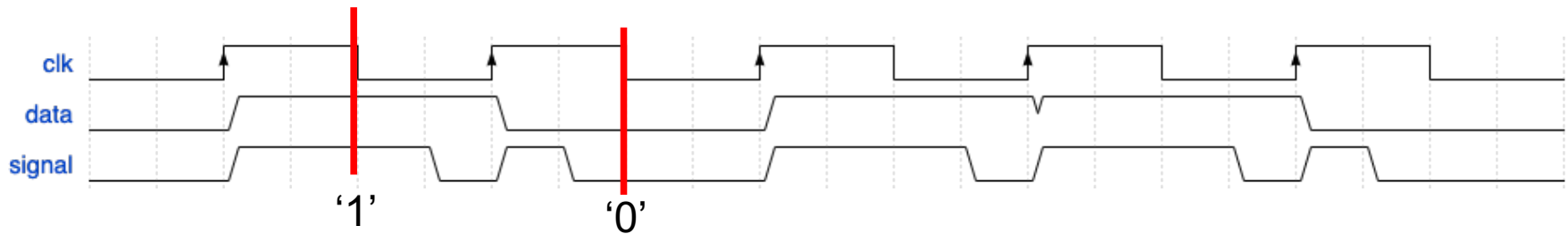


# Timing system current data encoding

- Timing system protocol currently uses 8b10 encoded NRZ data at 312.5 Mbit/s (for 62.5 MHz master clock)
- Clock, data recovered using an ADN2814 CDR chip
- **ADN2814 not available from regular suppliers**
  - No stock promised before 2023
  - Not declared obsolete – victim of global Silicon Chip Shortage
- Only available device with suitable data rate and zero configuration
  - i.e. only component in timing system that can't be replaced by alternative device
  - Would be good to remove this single point of failure even if short term remedy available
  - Want to support DUNE for lifetime of experiment. Including development of ND
- **Introduce data encoding which does not need a CDR chip**

# New timing system data encoding

- Transfer data by modulating duty cycle of a “clock” signal
  - **Duty Cycle Shift Keying**
- Using 25% = 0 , 75% = 1 , 50% = “Z”

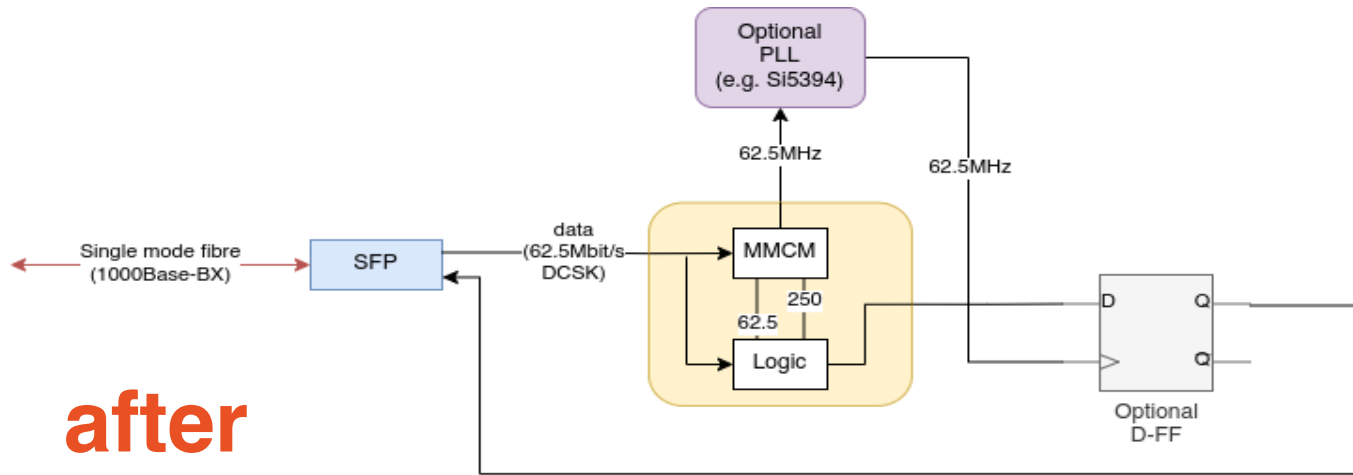
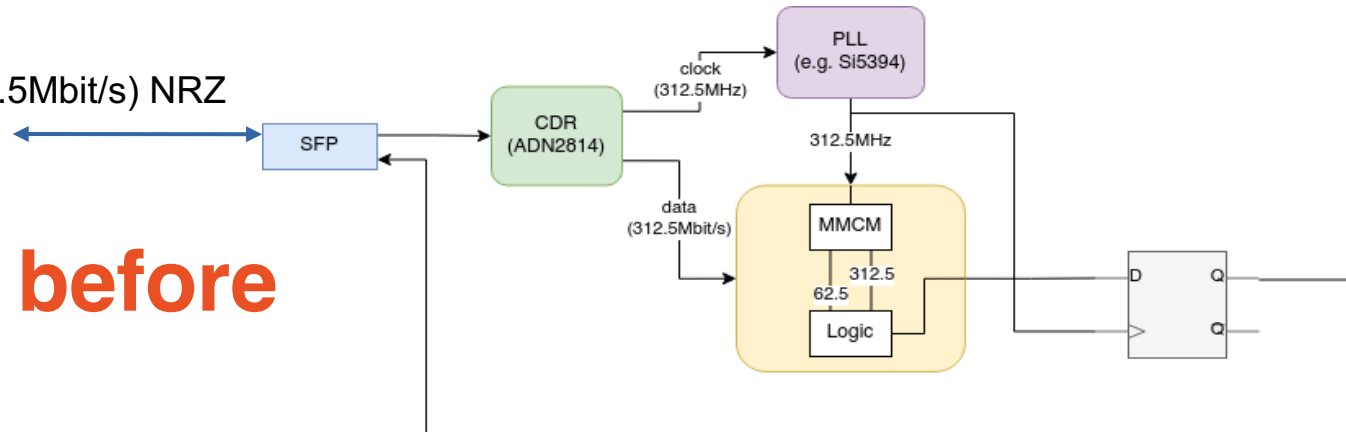


- Not naturally DC-balanced → Use 8b10b encoding
- **No external CDR chip required**
  - Future board designs remove or bypass ADN2814
  - Thought to be backwards compatible (CDR in signal path)
- Discussions between DAQ and other consortia under way

# Proposed data encoding signal paths

Data  
(312.5Mbit/s) NRZ

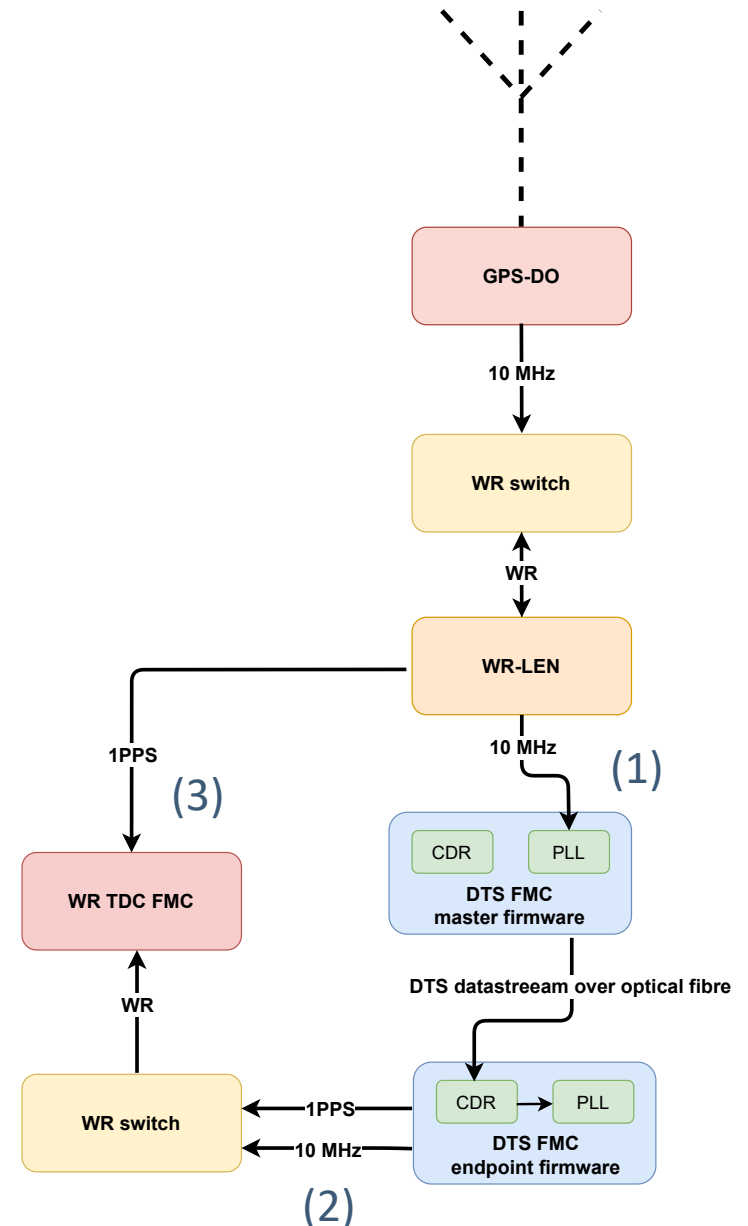
**before**



**after**

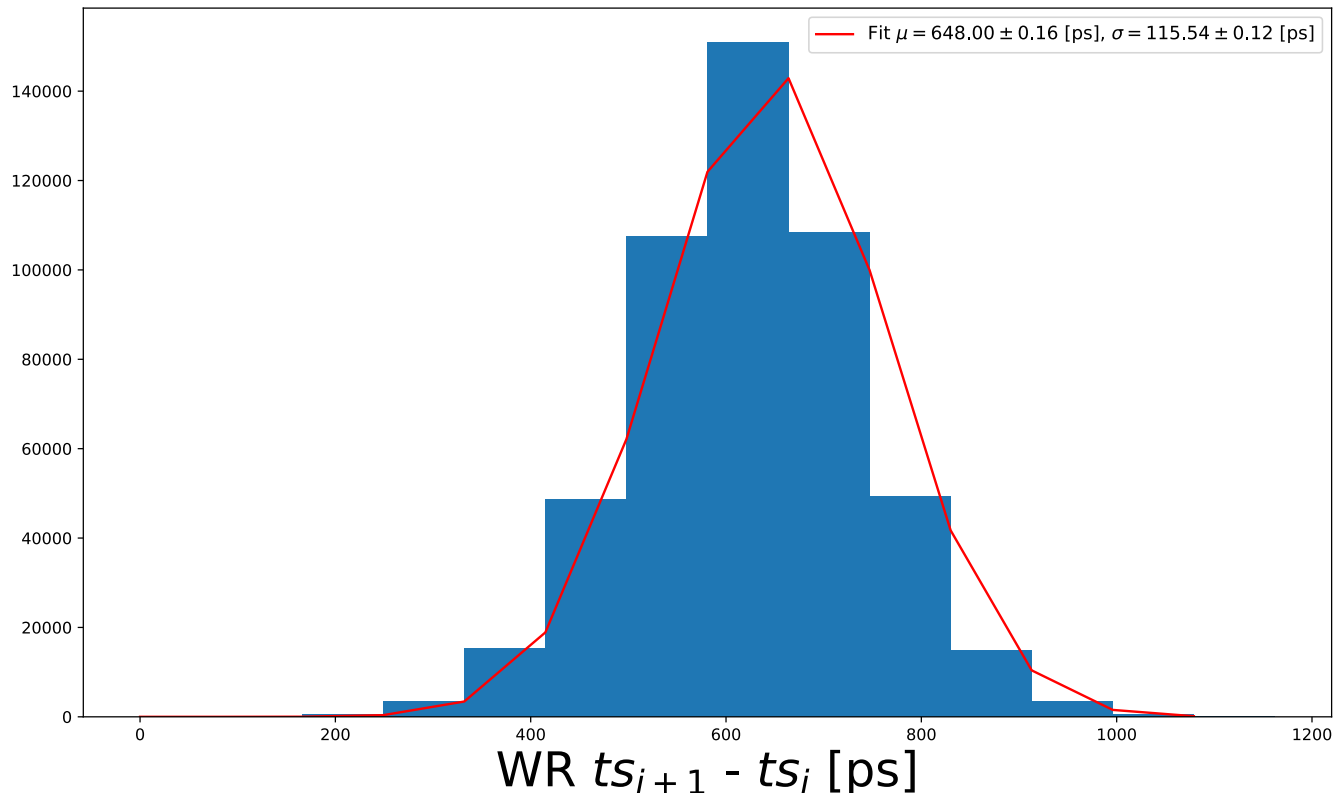
# DTS-WR interface test

- DTS generates its 62.5 MHz clock from 10 MHz clock provided by WR-LEN (1)
- DTS endpoint provides 10 MHz and 1PPS to WR (2)
  - WR switch time of day taken from NTP
  - **Verified WR switch able to lock to 1PPS and 10 MHz coming from DTS endpoint**
- 1PPS from WR-LEN timestamped by WR-TDC connected to DTS driven WR switch (3)
  - Distribution of 1PPS timestamps gives an indication of jitter introduced by whole DTS->WR chain
  - WR-TDC: <https://ohwr.org/project/fmc-tdc/wikis/home>



# DTS-WR interface test - 1PPS timestamps

- 1PPS timestamps appear stable over 6 days \*
  - Demonstrated by plot below of consecutive WR timestamp differences (1s offset subtracted)
  - \* Timestamp anomaly observed near start of data-taking (see next slide)



# DTS-WR interface test - 1PPS timestamps

\*Around 8 minutes into data taking the DTS driven WR switch appears to lose synchronisation for ~30s

- Causes WR-TDC timestamps to reset to ~01/01/1970
- Stable operation after (see previous plot)
- Exact cause unclear, possible external interference due to lab environment
- Longer stability tests foreseen in a more controlled environment planned



# Regression test structure

- Tests performed based on configuration files
  - Specifies the hardware and firmware to use
- A series of commands based on the firmware are run via timing system s/ware (currently pdtbutler tool)
- Text output from commands executed saved in a log file
- Log file is analysed using a python script to determine whether the tests successfully passed.
  - Gives a simple Go / No-go decision , together with detailed logfiles.
- For QA/QC of hardware store go/no-go decision in web-accessible spread-sheet, detailed logfiles in electronic logbook