High-pressure gas TPC test at Fermilab this Autumn (TOAD)

Patrick Dunne for the TOAD group

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Introduction

- Why ND-GAr?
- What are the goals of our test beam program?
- Progress so far
- Opportunities for hands-on hardware experience

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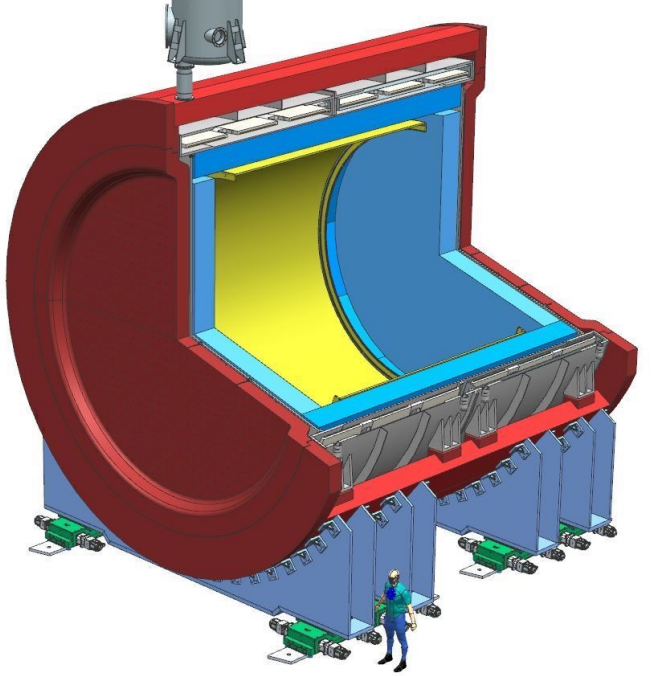
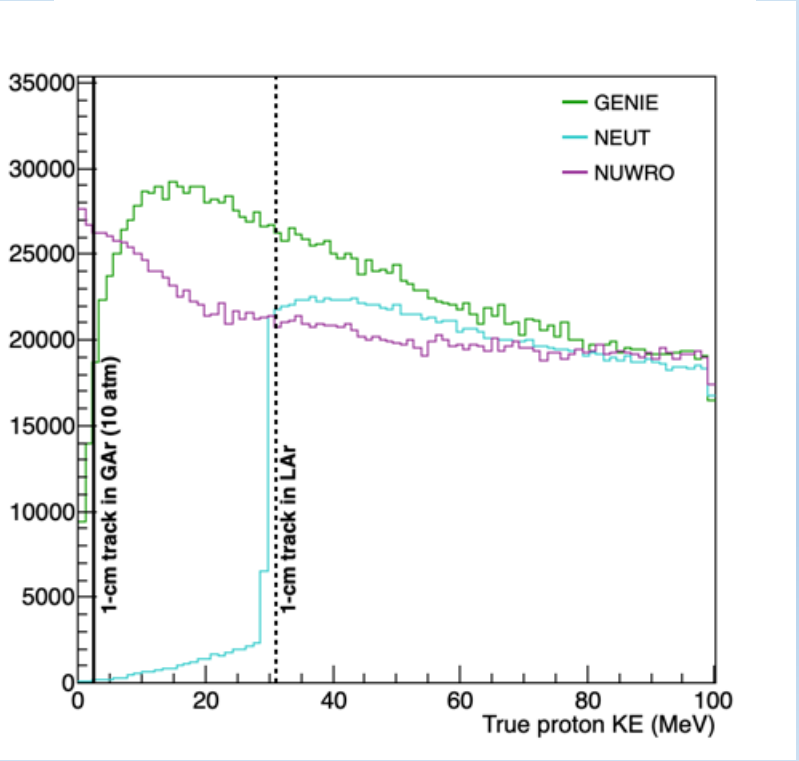
ND-GAr: Gaseous Argon

- 1 ton fiducial mass gas target TPC surrounded by ECAL and superconducting magnet
- Reusing ALICE TPC wire chambers
- Not all muons are contained in upstream ND-LAr so ND-GAr also acts as spectrometer for these
- Gas target has lower energy threshold than liquid
  - Models that are easily distinguishable in GAr but not LAr can lead to biases in oscillation parameters
- Key for hadronic final states which are hard to distinguish in ND-LAr and far detector that contribute to visible energy differently e.g. multi-π
- Impact on LBL shown by Stefan and Gary yesterday





TOAD

- The Teststand of an Overpressure Argon Detector (TOAD) will operate a slice of the detector and its electronics at FNAL in the 2022/23 beam year
- TOAD is based on the detector used for the 2018 CERN HPTPC beam test
- Two primary goals:
  1. Tune operating point and demonstrate long term operation of ALICE readout chambers and new UK designed electronics at high pressure for long time period
  2. Obtain a large sample of proton-argon interaction data with this low energy threshold detector
- Significant UK involvement and opportunities for students to get hands-on hardware experience

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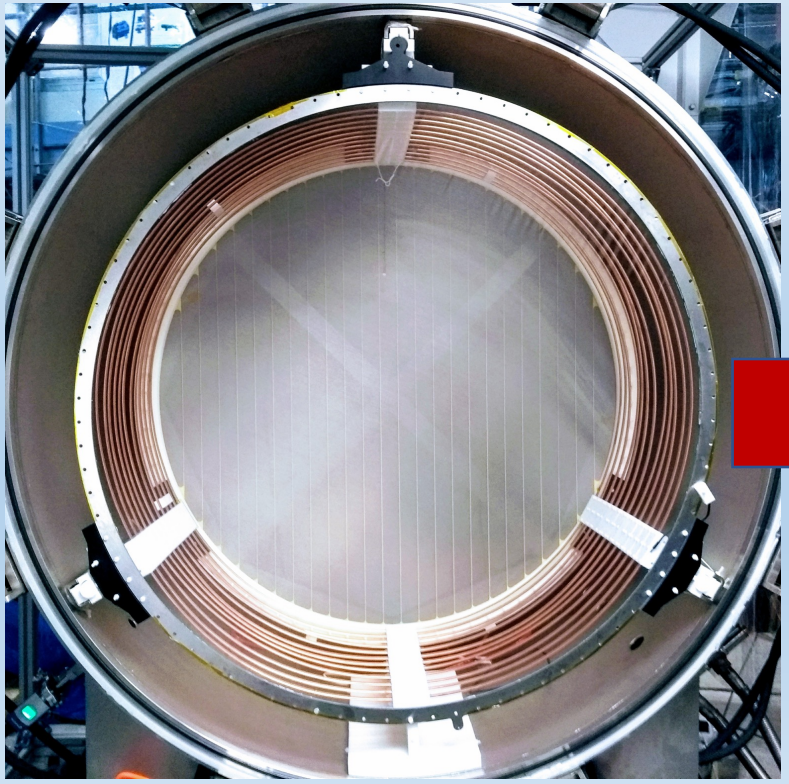
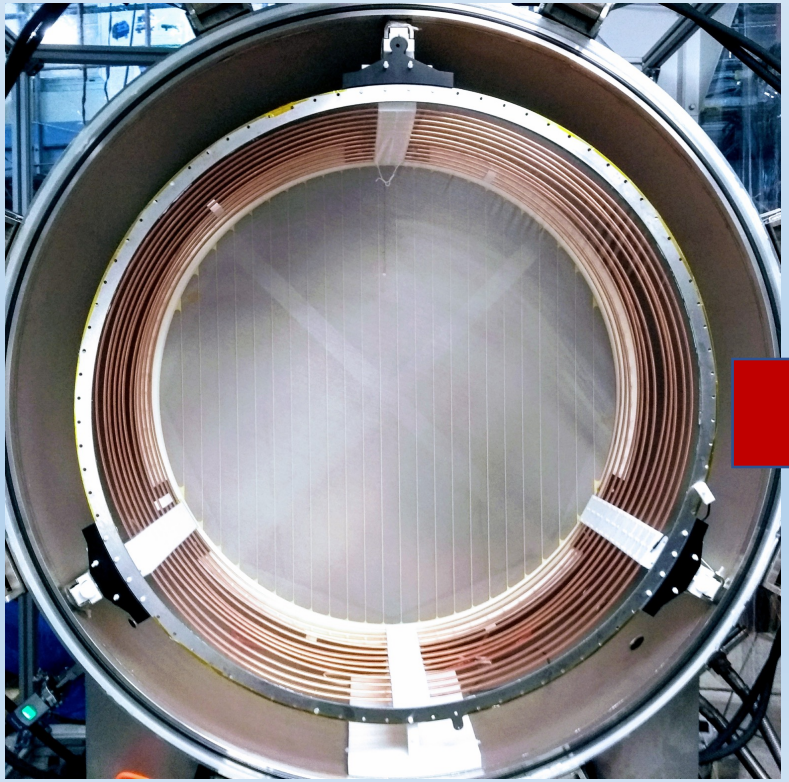
Upgrades to detector since CERN beam test

- Test stand is keeping the ~1m^3 5 bar pressure vessel and field cage used for the CERN HPgTPC test beam (built with STFC PRD funding)
- Detector has undergone significant refurbishment with funding from UKRI, STFC, Royal Society and US partners



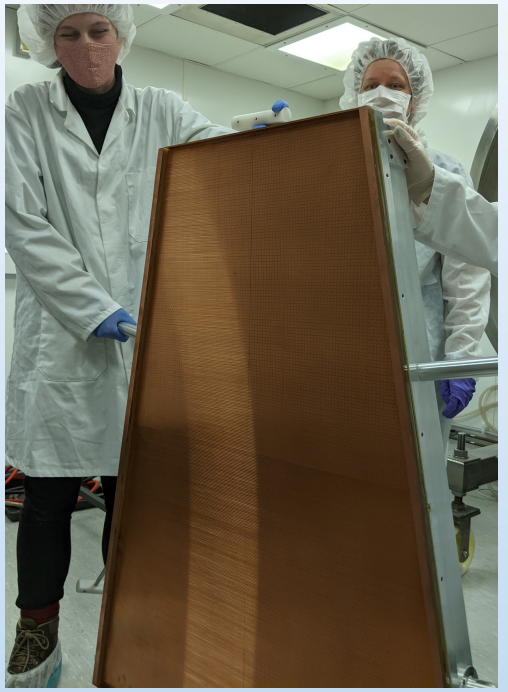
Upgrades to detector since CERN beam test

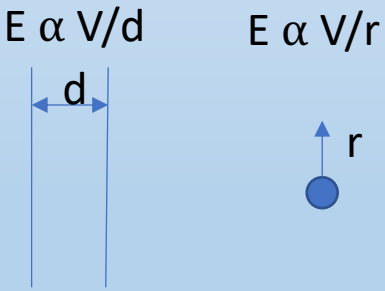
- New OROC amplification region
- Renovated high voltage path inside vessel
- New readout electronics and computing
- New vacuum pumping system



Wire chamber upgrade

- ALICE wire chambers come in two types
  - Outer and Inner ReadOut Chambers (OROCs and IROCs)
- We have put an ALICE OROC into the pressure vessel as it is the only vessel easily available that can accommodate this larger chamber
- Wire amplification achieves similar gain with much lower voltage than CERN beam test mesh amplification system
- Gain demonstrated using radioactive sources at 5 bar
  - Can see Fe55 source well in charge data at these pressures





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Wire chamber upgrade

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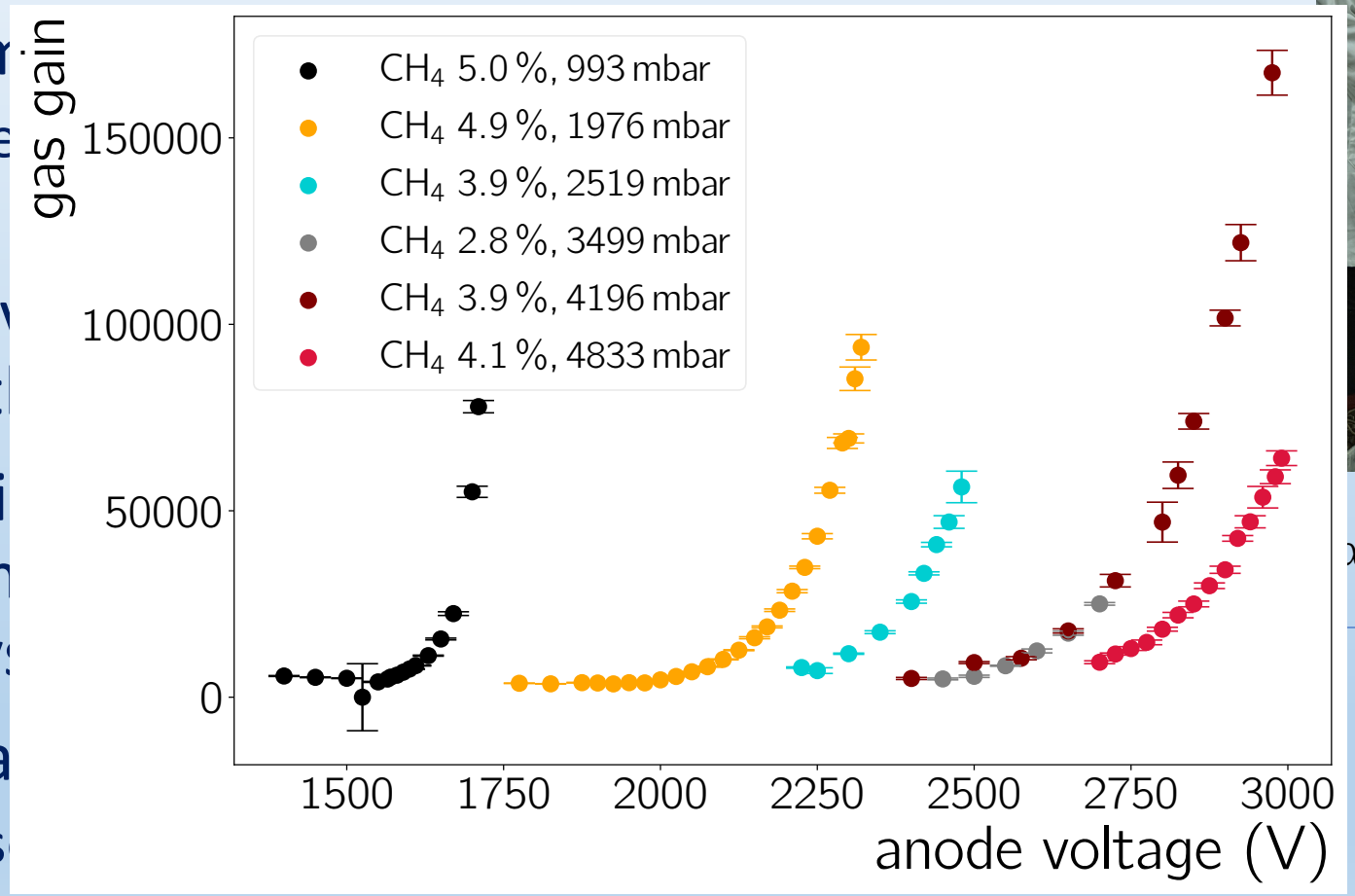

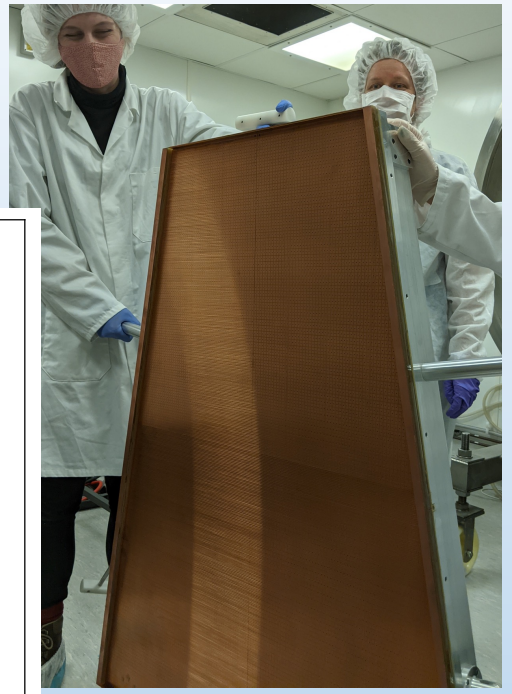

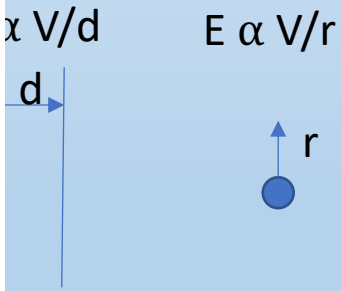

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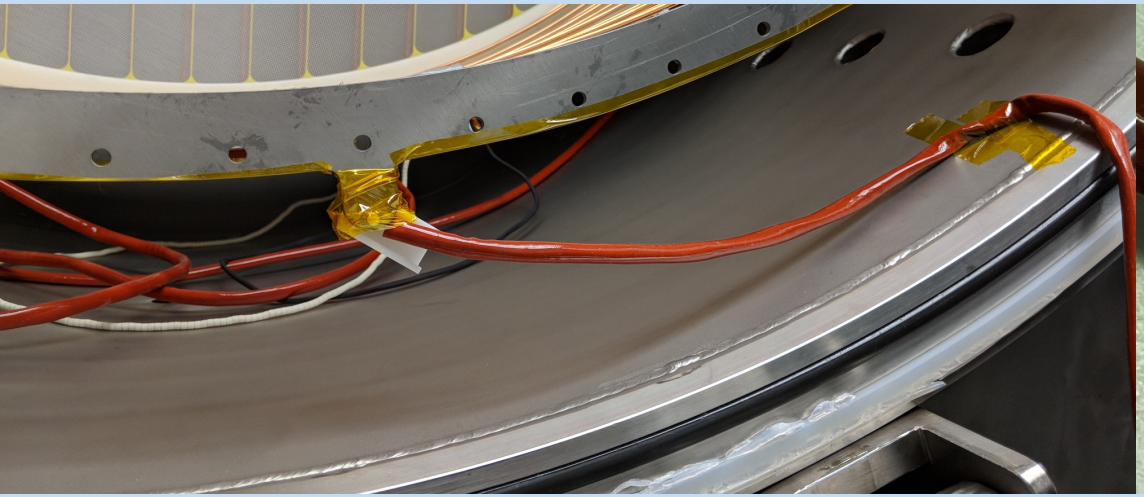
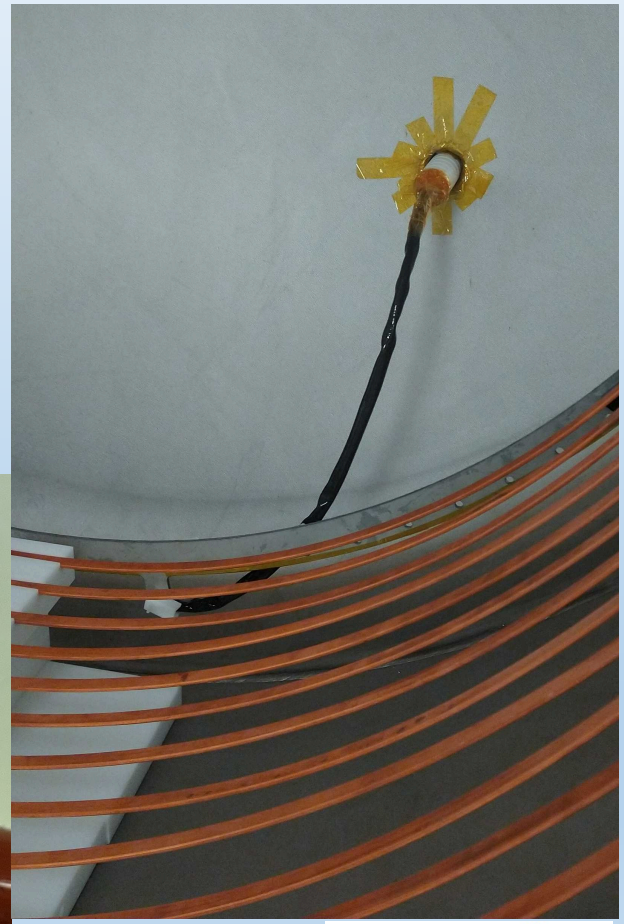
High voltage cabling upgrade

- In CERN test shorting through cathode cable fiberglass sheath was limiting our cathode voltage and therefore increasing diffusion during drift
- Feedthrough was on door so cable hung down in contact with vessel when closed making the problem worse
- We upgraded the fiberglass sheath, plus use a new shorter cable path increasing maximum voltage from 8 kV to 17 kV





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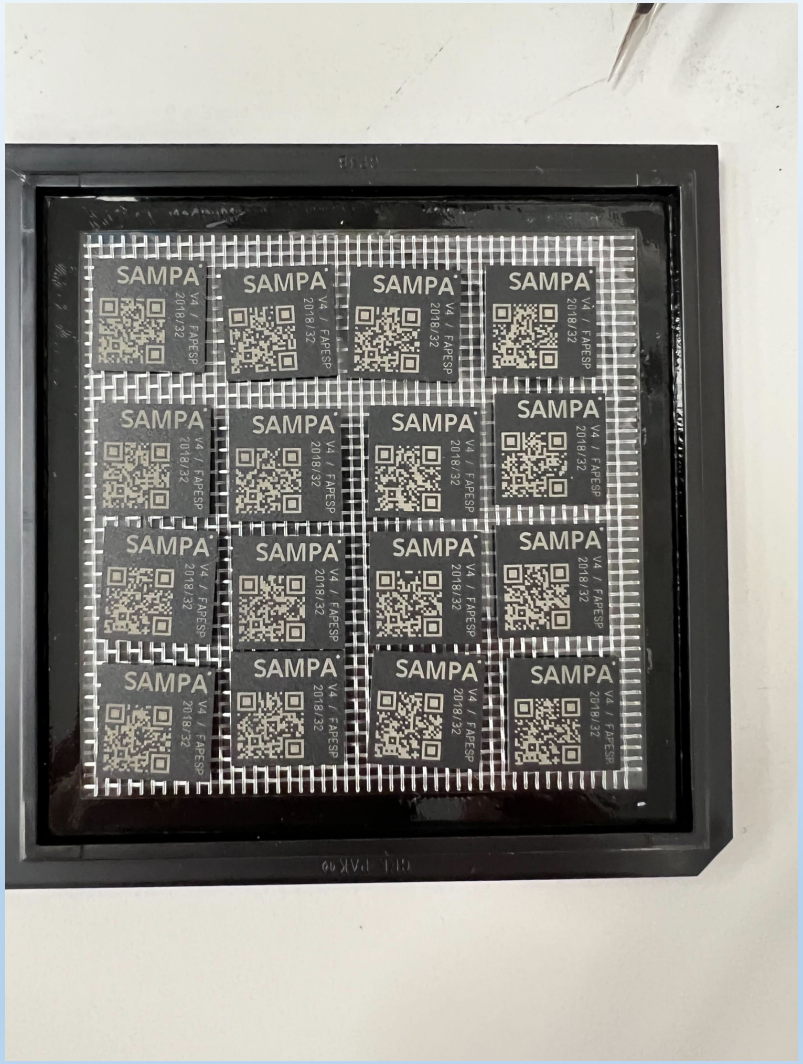
Electronics

- CERN detector primary readout was light based so charge readout was unpixellated. Also had a long analogue signal path to preamplifiers and digitiser outside vessel
- ND-GAr electronics will have ~700k channels, must work at pressure in ~0.5T field and will need lower noise than CERN detector system
- New system based on ALICE SAMPA digitizer and FPGAs is being developed at Imperial, FNAL and Pittsburgh to these requirements
  - Step change in detector readout capability
- A full slice of this system will be used for TOAD



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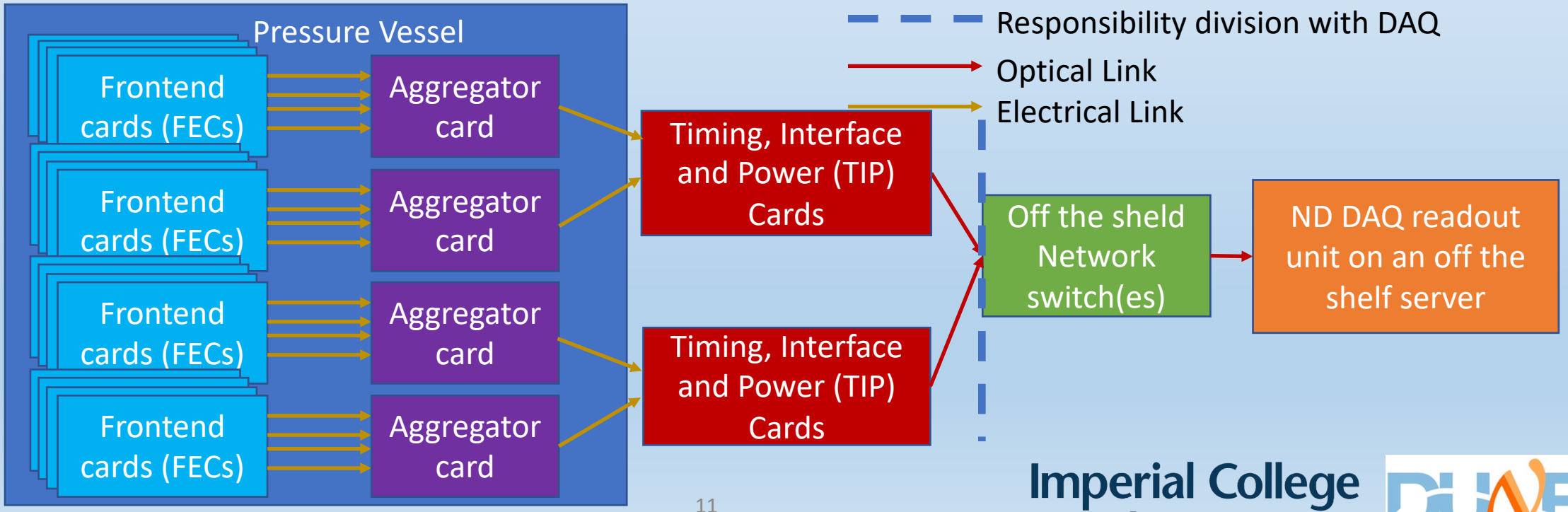
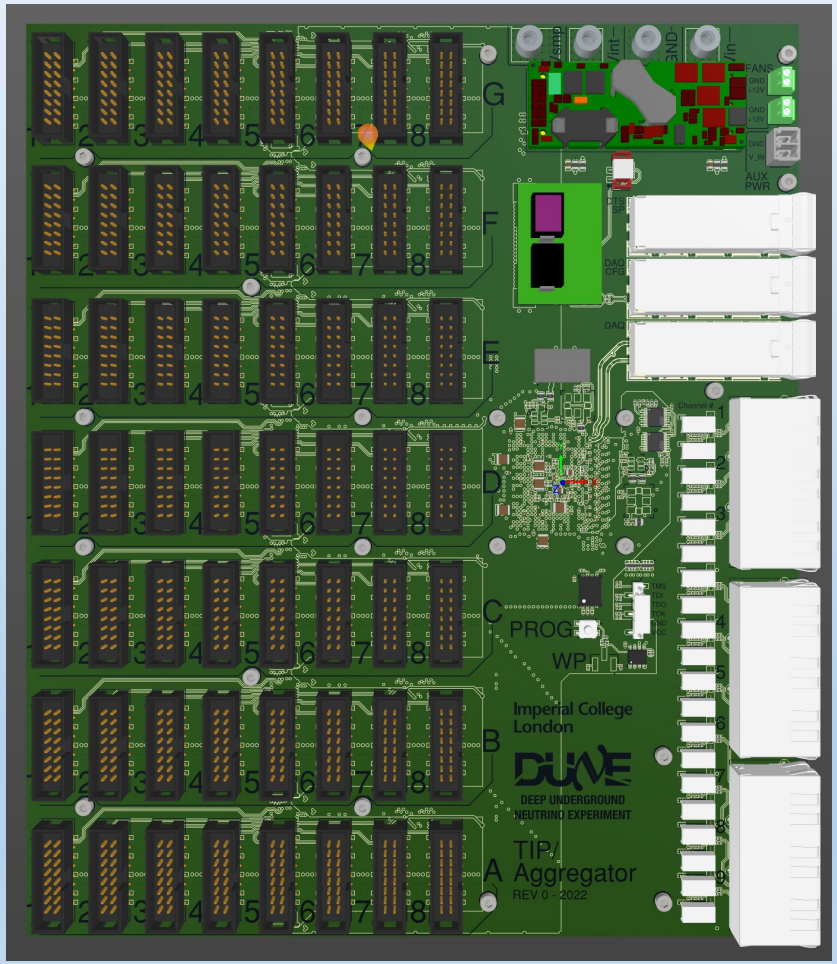
Electronics and DAQ

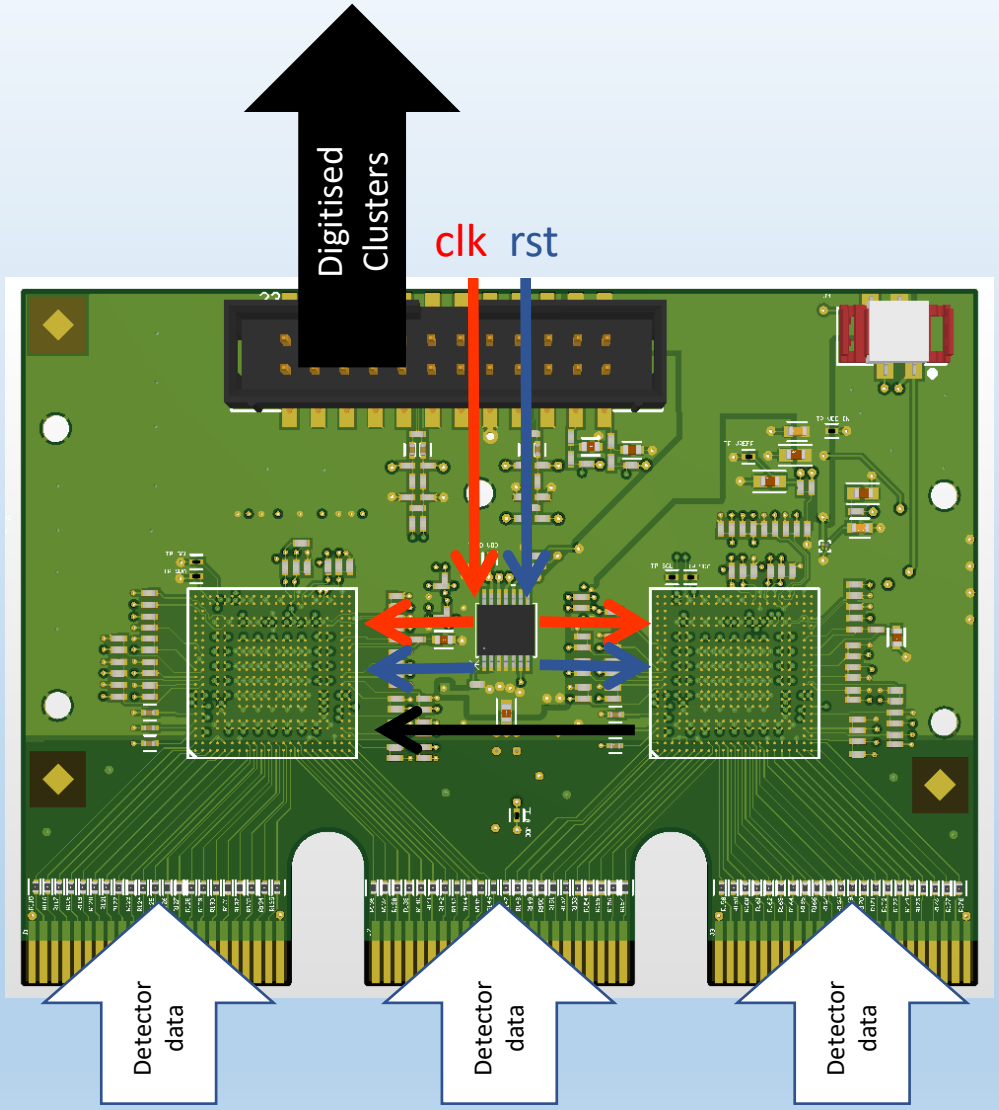
- Digitisation occurs at the wire chamber reducing analogue signal path
- FPGA based aggregator boards (Imperial) minimize number of feedthroughs in vessel
- TIP cards (Imperial) aggregate further, control system and provide timing and power
- Will interface with DUNE DAQ group software via off the shelf networking
- First versions of all of these boards are being assembled this week



Electronics and DAQ

- Pictures of TIP, AGG, FEC





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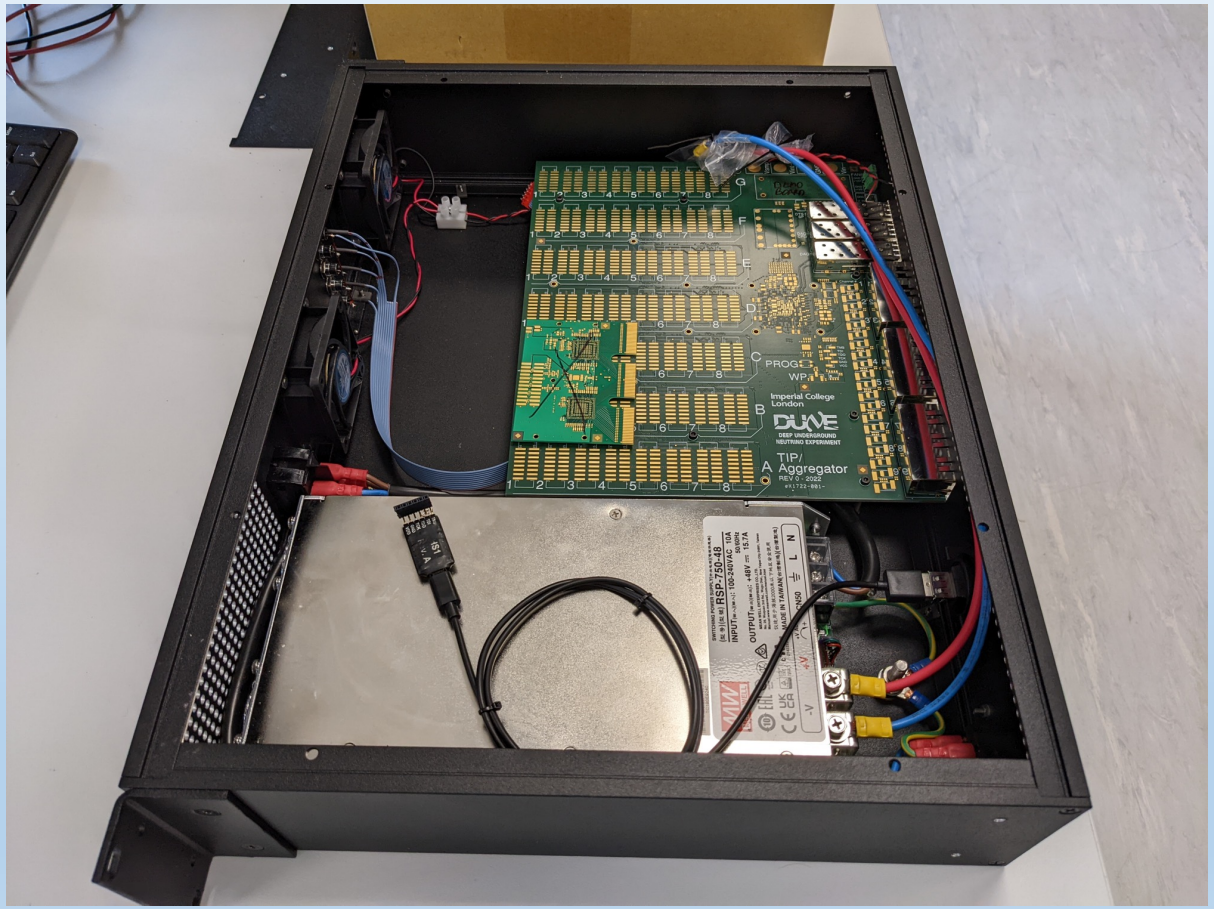

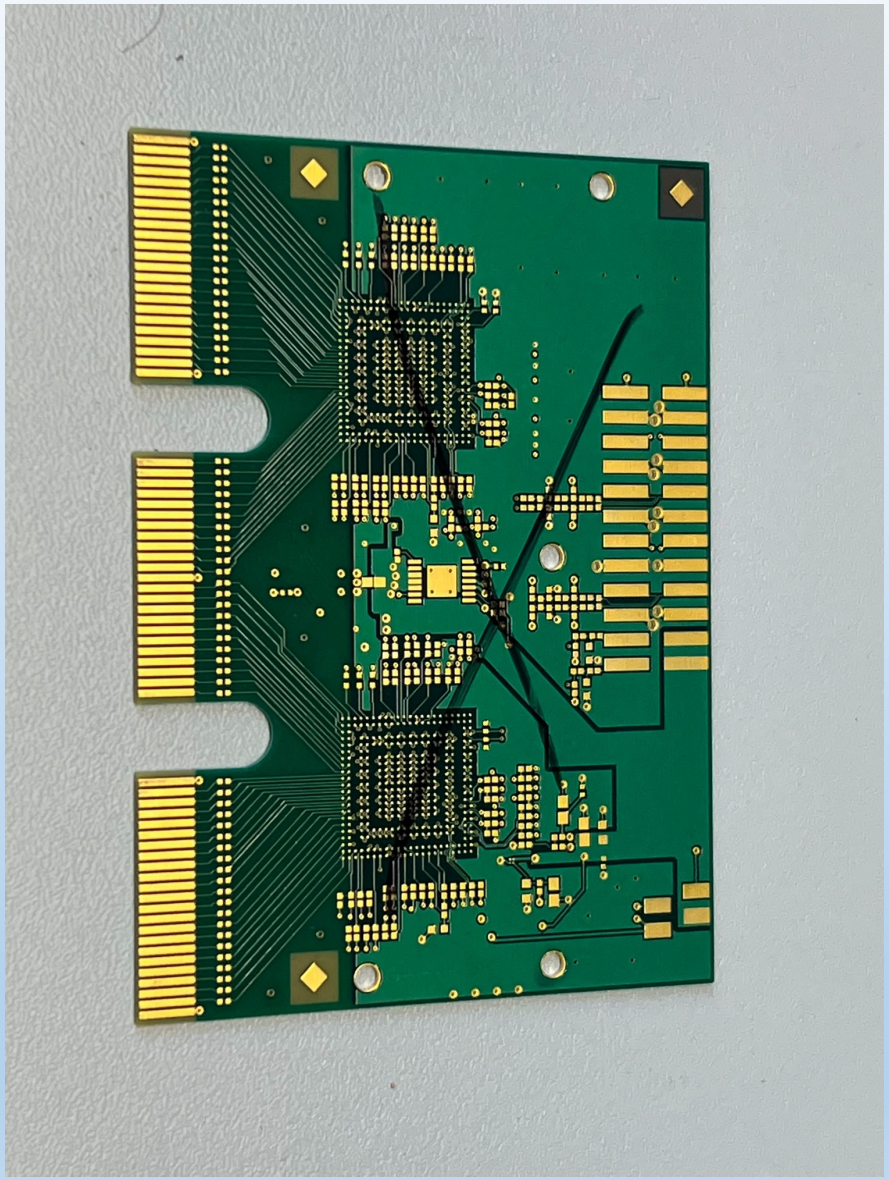

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Fermilab test beam

- Detector shipping to FNAL 2nd week of August
- Assembly and commissioning at D0 assembly building (DAB) through Autumn
- Moving to MCenter beamline at Fermilab Test Beam Facility (FTBF) where LArIAT was in time for beam start November/December this year
- We will be in the beamline for the full beam year ending ~July 2023
- Long run lets us:
    1. Demonstrate operation of full slice of ND-GAr in a low energy hadron beam from hardware through to real event reconstruction
    2. Collect a sample of proton-argon interactions with low energy hadron information for use in cross-section model tuning

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Summary

- Beam test with large UK involvement happening at FNAL from September 2022 to July 2023
- Will demonstrate long-term operation of ALICE wire chambers and UK designed and built electronics at high pressure in a beam
- Hardware is fully funded and core team of detector experts is already identified but we need more people to come to FNAL to commission and operate the detector
  - Great opportunity for people to get hands-on hardware experience

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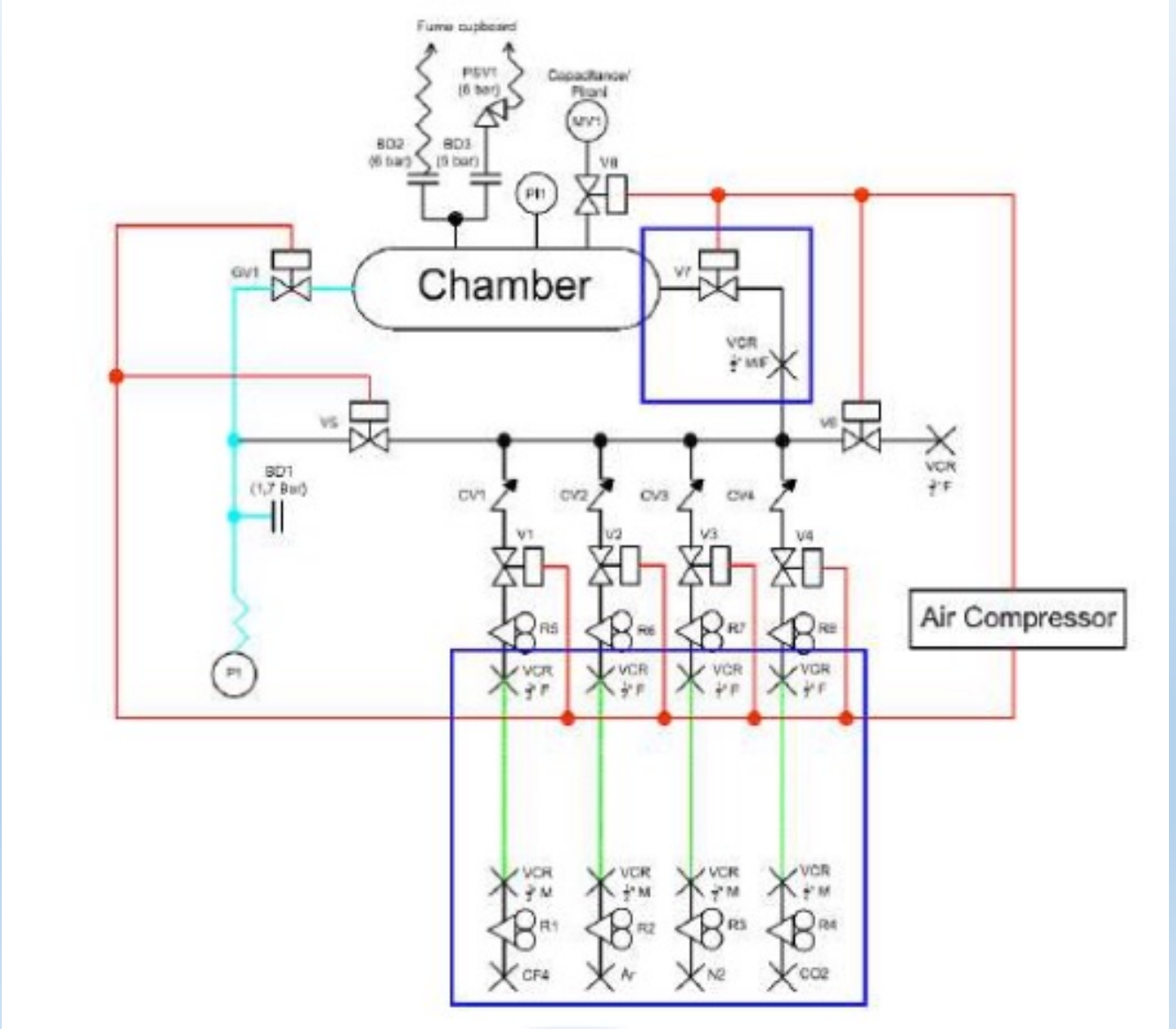
Backup

Pressure vessel

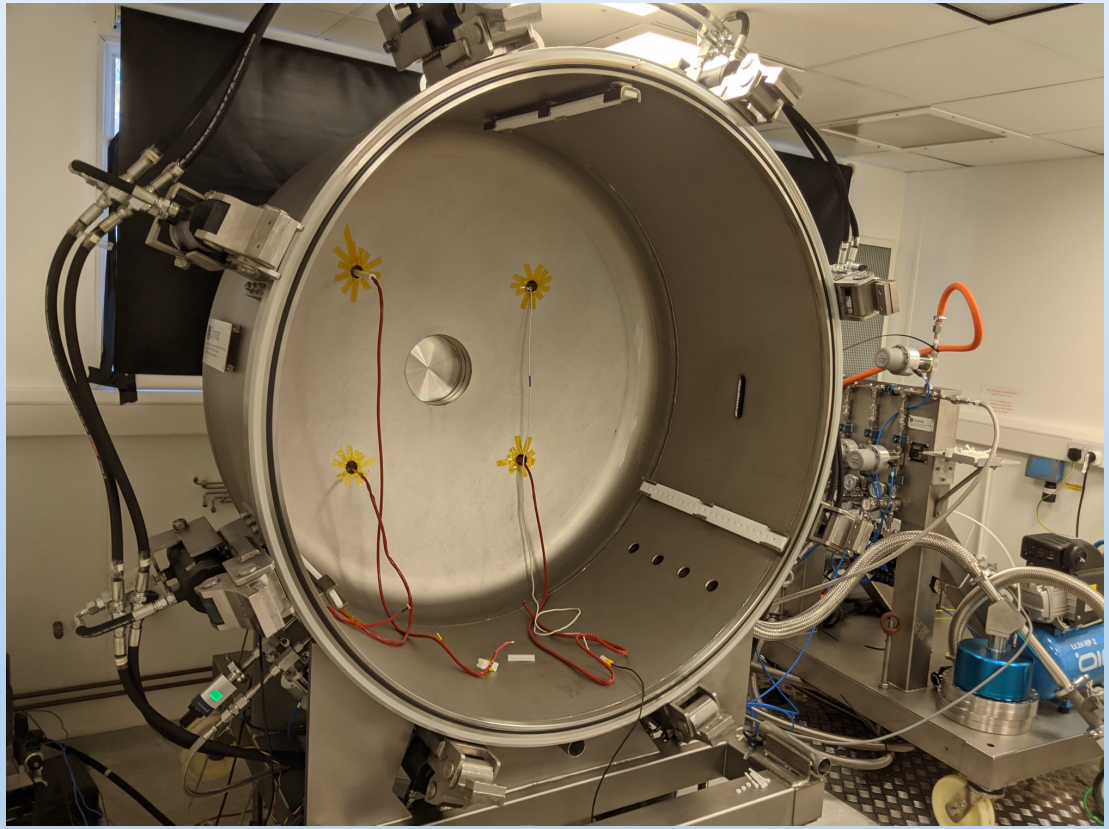
- Vessel is CE stamped for operation at 5 Bar (see Evan's email for details)
- Accesses are several ports (6 DN200, 13 KF40, 4 KF25, 1 custom), plus a large door
  - KF flanges are operated using overpressure retaining rings (fine up to 75psig according to standard)
  - Large door is a DN1500 flange held shut with 8 hydraulic rams and 8 manually tightened clamps
  - Custom flange was certified as part of the vessel's CE stamp

Pressure vessel operation

- Main vessel overpressure protection provided by burst disks:
  - 5 bar burst disk with safety valve calibrated to 5 bar
  - 6 bar burst disk
- Design complies with CE requirements
- Vessel is evacuated then filled to required pressure (no continuous flushing)
- Gas mixes achieved by filling from 4 separate lines to desired partial pressures



Pressure vessel pictures



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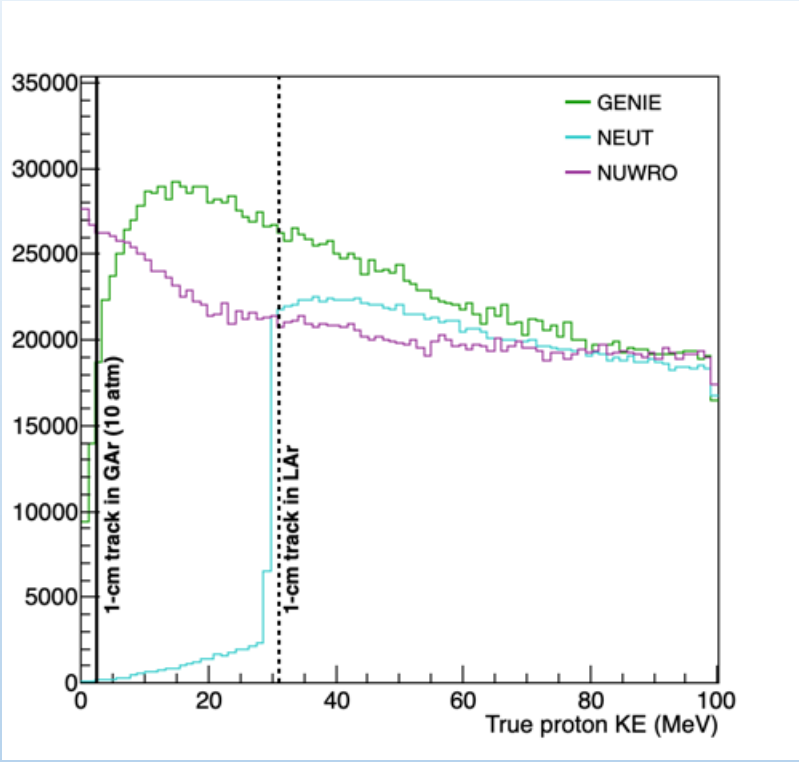
Facility Requirements

- Looking to study low energy proton interactions with argon so need MCenter tertiary beam for a long beam run
- Center of detector is ~1-2m from the ground so we will need a platform to raise it to beam height
- In discussions already re power, gas, computing etc. requirements
- Aiming to arrive early Autumn to assemble and commission detector ready for beam start



Funding and personpower

- UK funding secured to update pressure vessel, ship it to FNAL and provide operating consumables (e.g. gas)
- Electronics being jointly built and funded by UK (Imperial) and US (FNAL/Pittsburgh) groups
- ~20 people have currently expressed interest in assisting with shifts
  - Includes ~2 FTE years of funded UK students to provide expert shifters for electronics system and several experienced postdocs/fellows coming for 6 week to few month stays
  - We are welcoming new effort from anyone who will be around at DUNE during the running period

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Summary

- Aiming to operate ~1m3 high-pressure gas TPC test stand for several months in the Mcenter tertiary beam
- As well as long-term operations experience we will collect large sample of proton-argon interactions which will provide new dataset for tuning models of final state interactions in neutrino-argon interactions
- Program is fully funded, main remaining item is recruiting more on site PhD student help to insure we can achieve 24 hour operation through full run period

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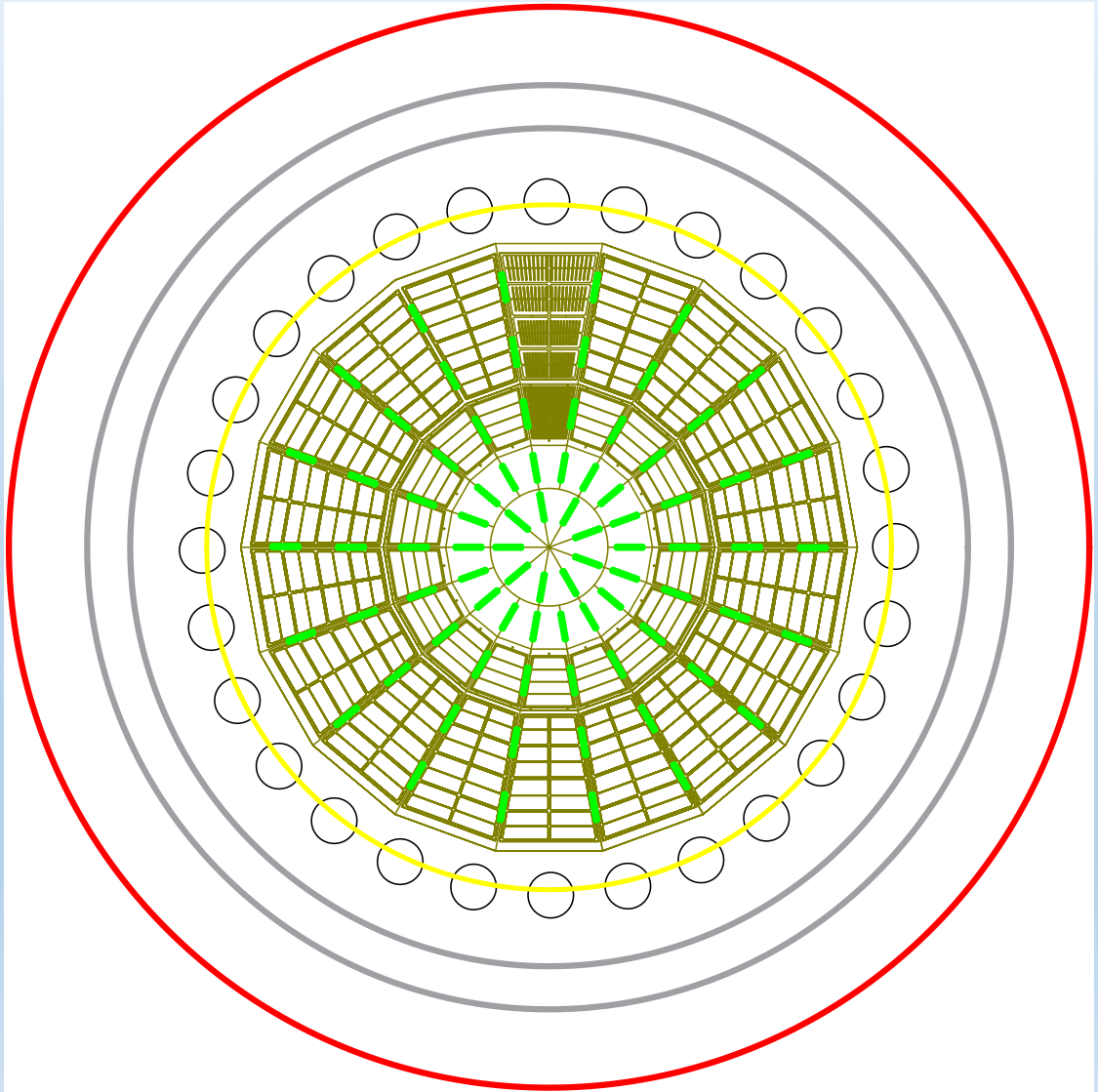
Electronics Requirements

Front end

- Single hit resolution in drift direction: aiming for 1.5mm
- Number of channels: ~700,000 (570k from ALICE ROCs + 130k central region)
- ND DAQ requirement likely to be that we stream all data into DAQ after zero-suppression
- Dynamic range must be sufficient for signals from both protons and MIPs in 10 bar of Argon
- Heat output into the detector volume should not affect temperature stability of TPC active region



Interfaces, constraints: upstream

- Readout will connect to repurposed ALICE readout chambers (ROCs)
- Interface consists of pads arranged in lines of 23 pads/grounds (21-2 or 22-1) per connector slot
  - Blocks of 3 connector slots always contain 64 signal channels and 5 grounds

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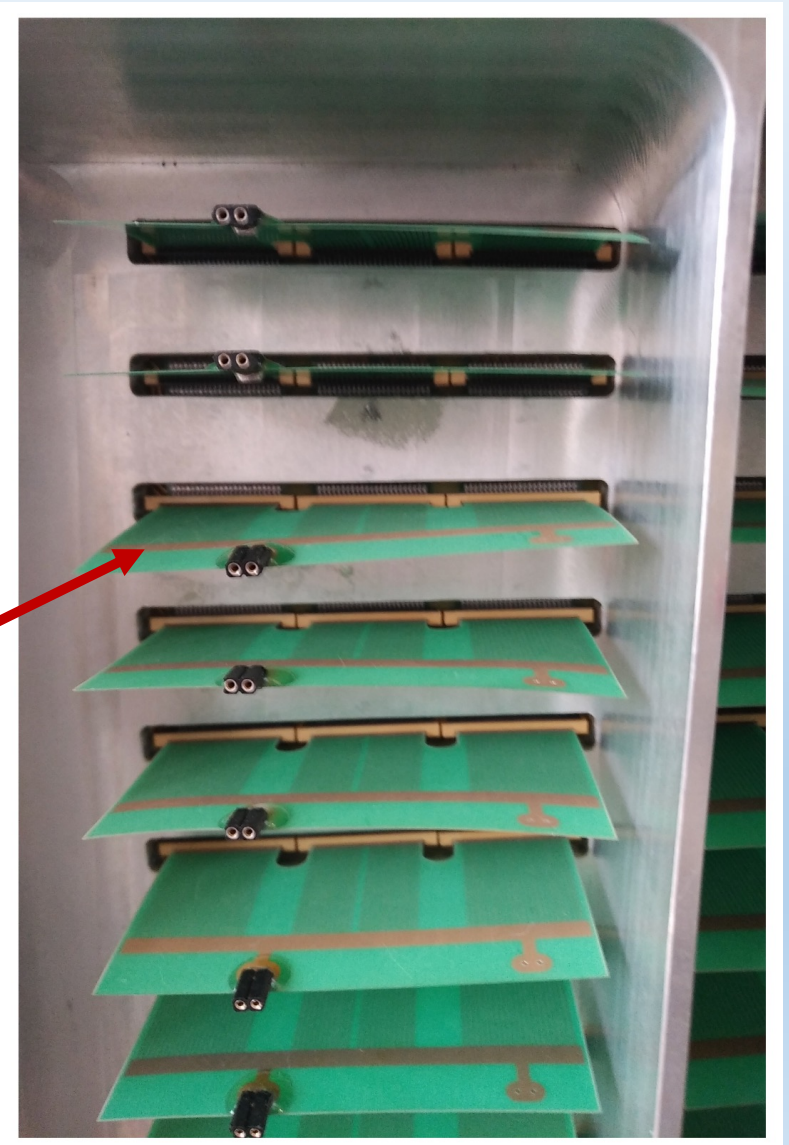
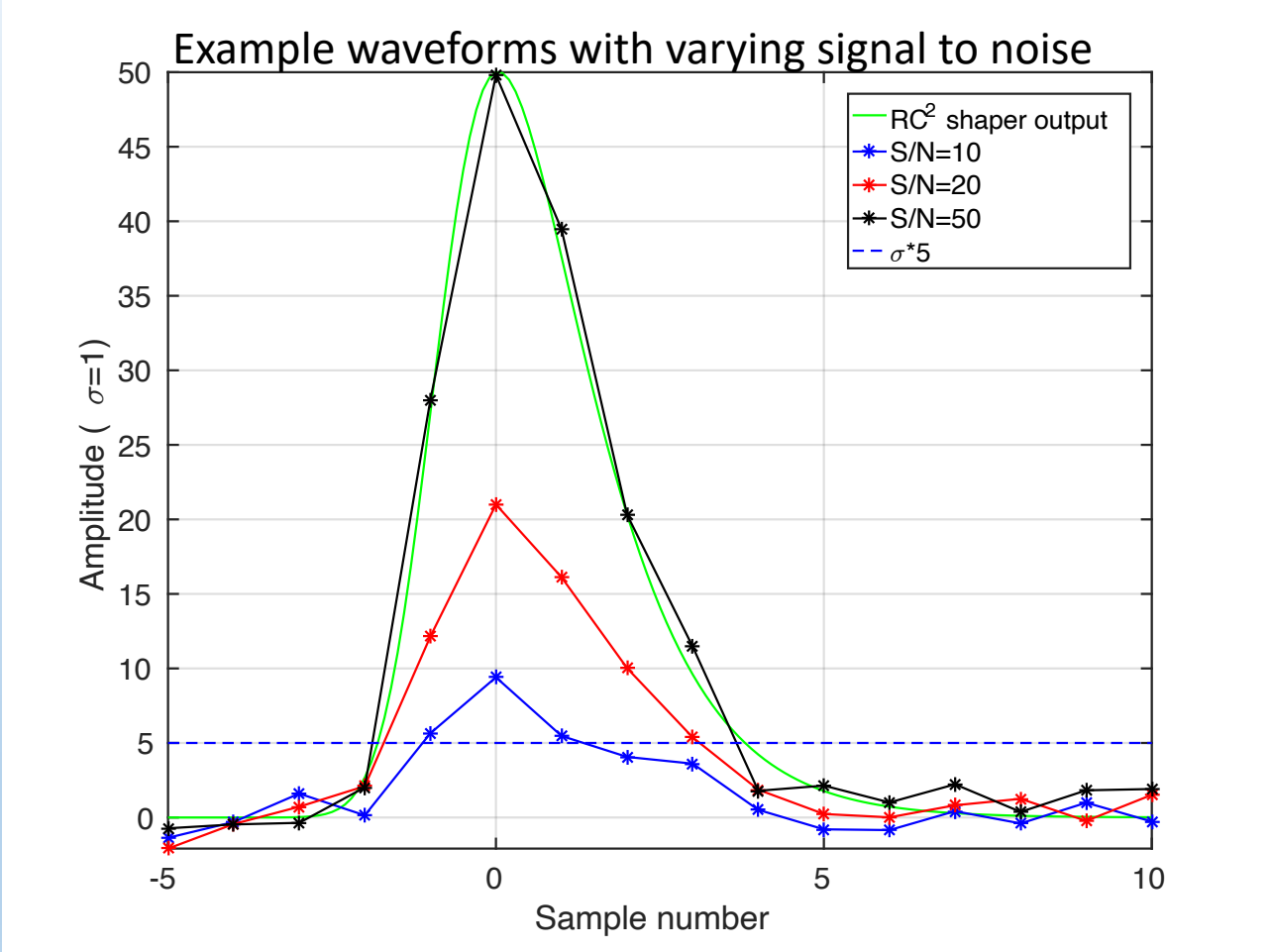
- Interface consists of pads arranged in lines of 23 pads/grounds (21-2 or 22-1) per connector slot
  - Blocks of 3 connector slots always contain 64 signal channels and 5 grounds
- Initial tests using PCBs that short 64 channels into one
- Long term will be replaced by ASIC host cards described later



Interfaces, constraints: upstream

- No on-board triggering so hardware level zero suppression will be needed to reduce data rate to an acceptable level
- Common industry standards are to zero suppress at ~5xRMS of noise and aim for signal to noise of at least 20
  - ALICE's design goal was a S/N of 30 for MIPs so this should be achievable



Interfaces, constraints: downstream

- System will interface with ND DAQ
- Interface is optical fibers into a network switch using TCP/IP
- Data rate studies underway but initial results imply we can stream all data passing zero-suppression from detector out into DAQ
- System will also need to receive and distribute information from central timing system

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Longitudinal single sample resolution

- Choice of digitizer ASIC must have sufficient sampling frequency
- Argon gas has drift velocities O(10cm/us)

Required resolution	Implied Sampling Frequency
1cm	10 MHz
1mm	100 MHz
100um	1 GHz

- Does not take into account longitudinal diffusion
- However, these are single sample resolutions so significant improvement from fitting sequential samples from adjacent pixels
  - ALICE achieve 1300um precision with 5-10 MHz sampling

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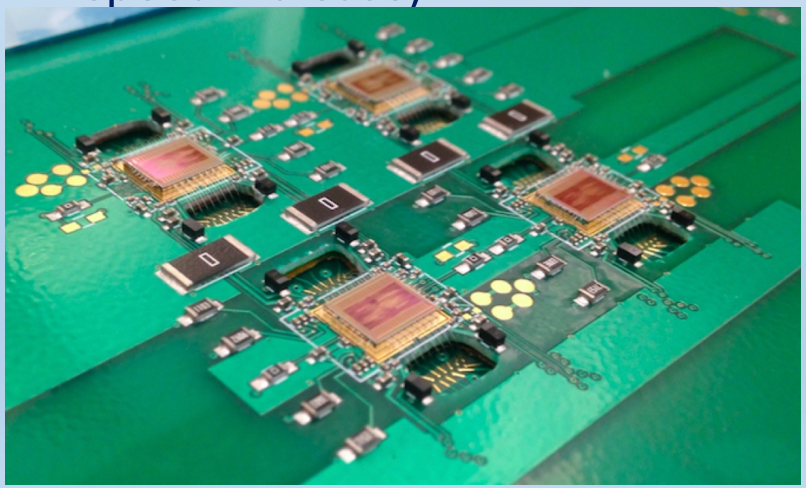
Digitiser ASIC options

- LArPix is clear front runner, but here are some other options for comparison
- Host and aggregator boards will also contribute to thermal budget

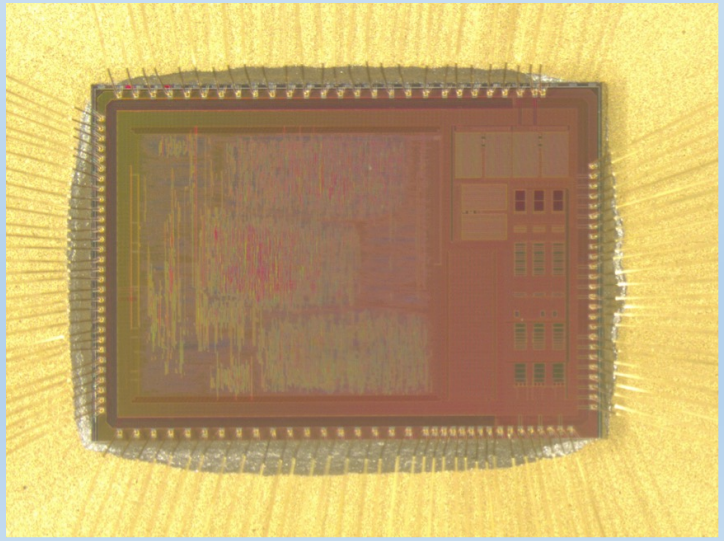
LArPix v2 chip

- 64 channels at 500kHz (but can be upgraded (interest in doing this in Rutgers, FNAL, UC Santa Barbara
- ~100 uW/channel (will go up with speed increase)



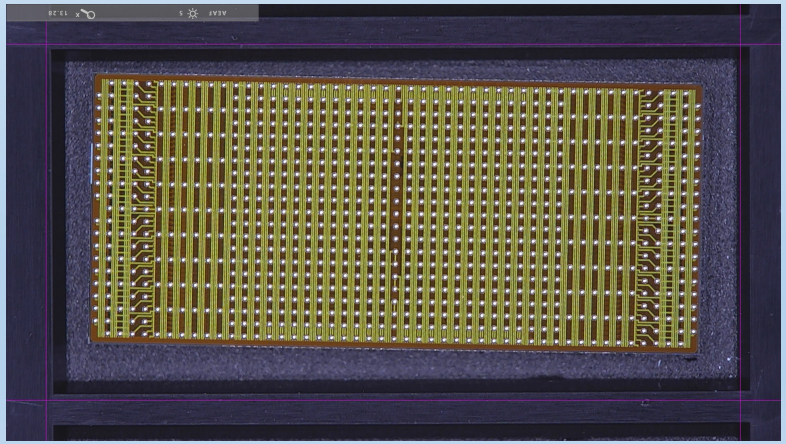
SAMPA chip develop for ALICE TPC upgrade

- 32 channels at 5 or 10 MHz
- ~35 mW/channel



HGROC chip developed for CMS HGCAL

- 72 channels at 40 MHz
- ~15 mW/channel



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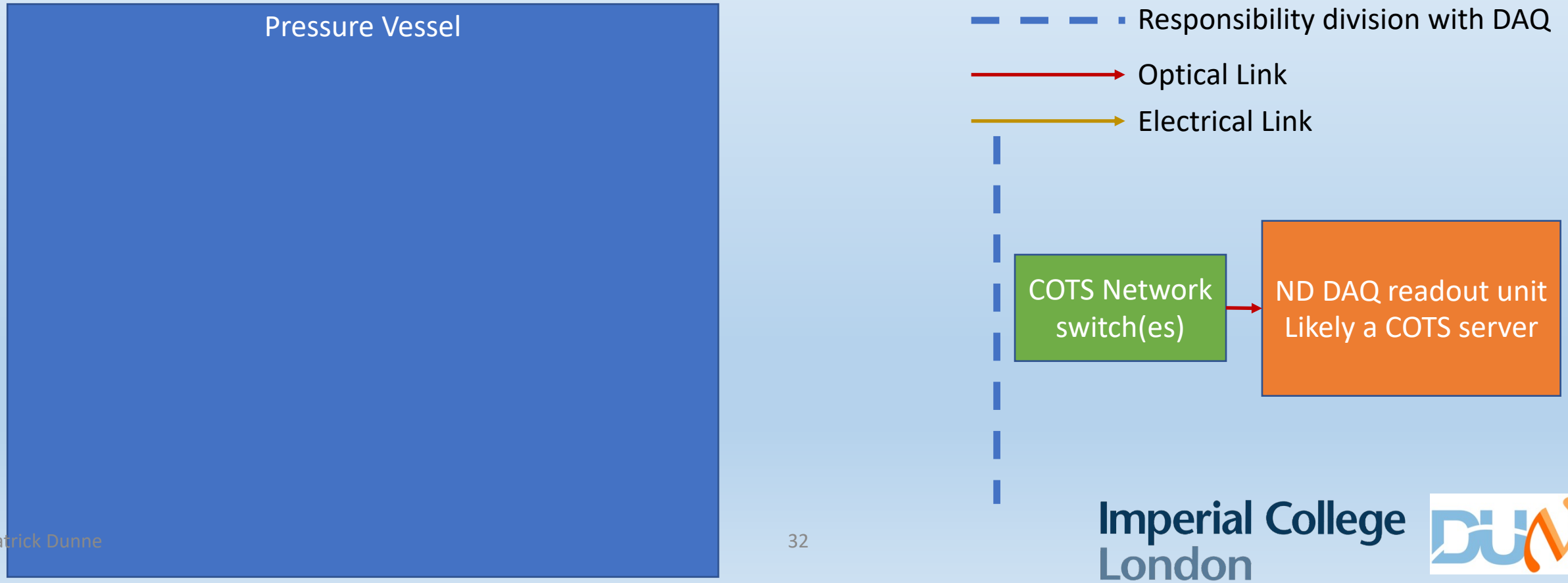
System Design

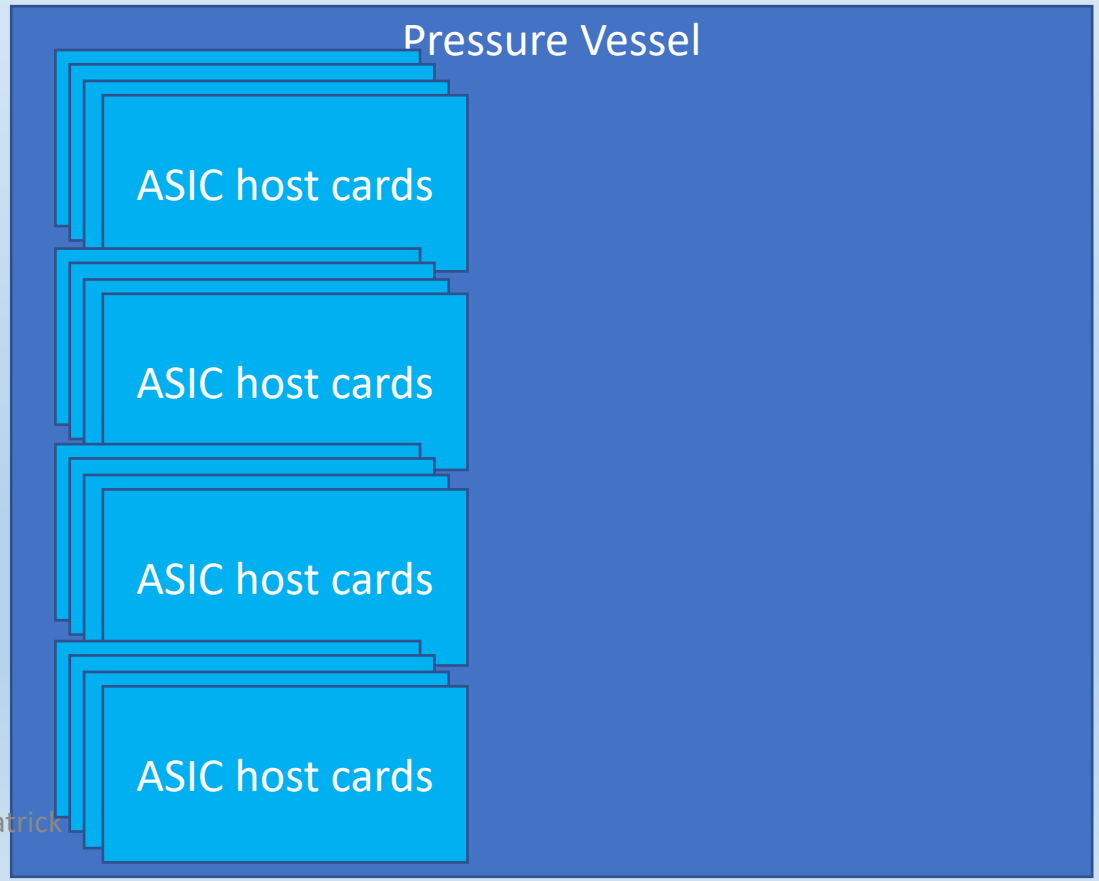
System Design – 1) Digitisation

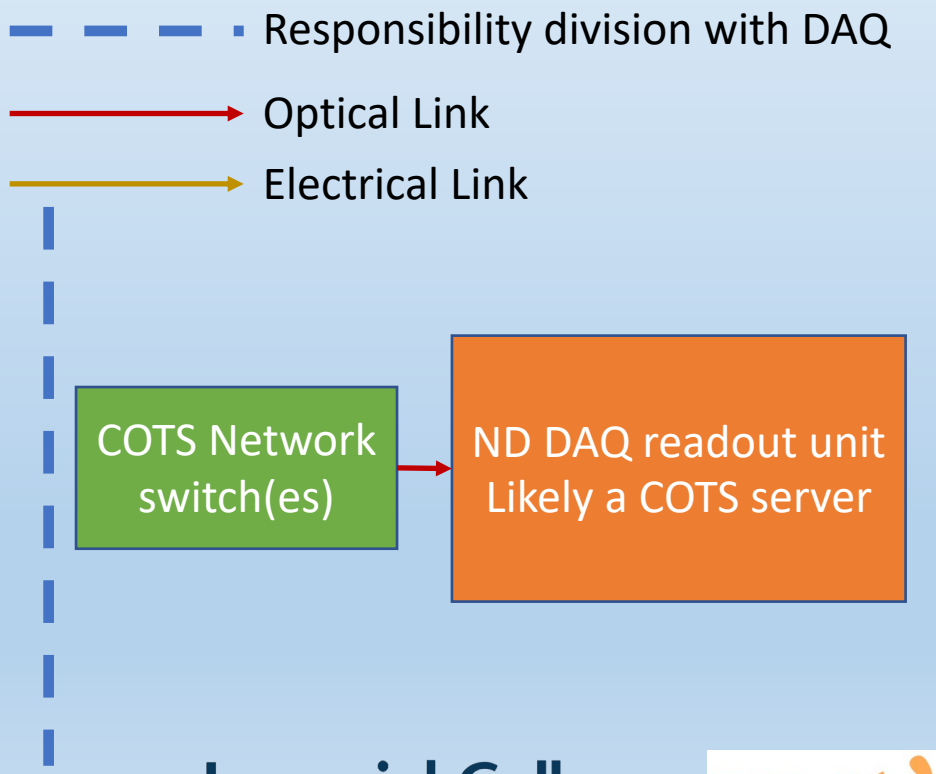
- 700k channels will need significant aggregation to have an acceptable number of links out of the vessel. We also want to limit the analogue signal path length



System Design – 1) Digitisation

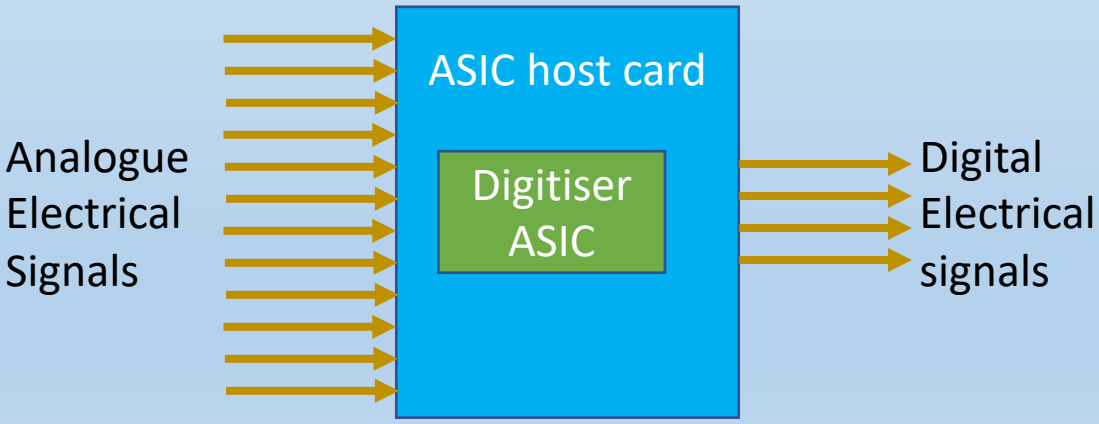
- 700k channels will need significant aggregation to have an acceptable number of links out of the vessel. We also want to limit the analogue signal path length
- Therefore, must digitize and zero-suppress inside vessel before sending out of vessel

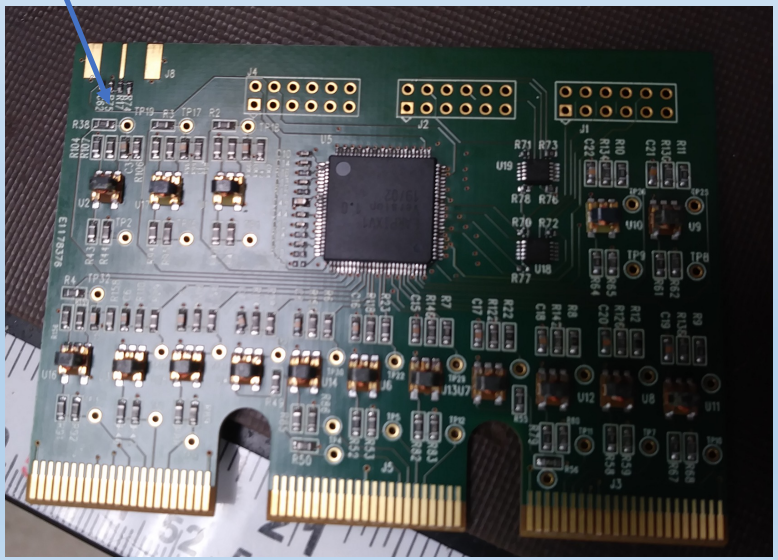




ASIC host cards

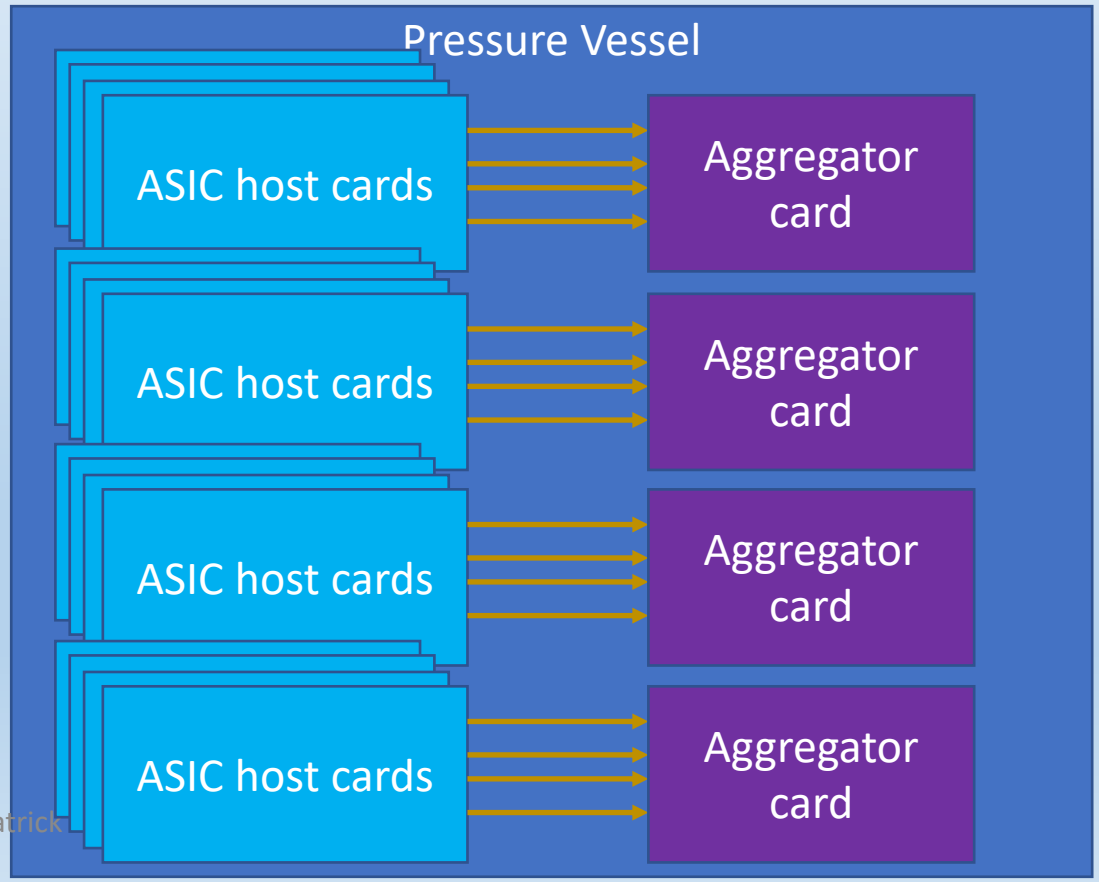
- Input is analogue electrical signals from detector
  - Each one will be positioned in a block of 3 ALICE ROC slots using an edge connector as 64 channels matches number channels a single LArPix v2 can read: implies ~11,000 of these cards
- Primary role is digitization of signals and zero-suppression
- Version with LArPix v1 has been designed by Pittsburgh and will be tested at FNAL
  - LArPix v2 will be easier as signal inversion can be done on LArPix with v2

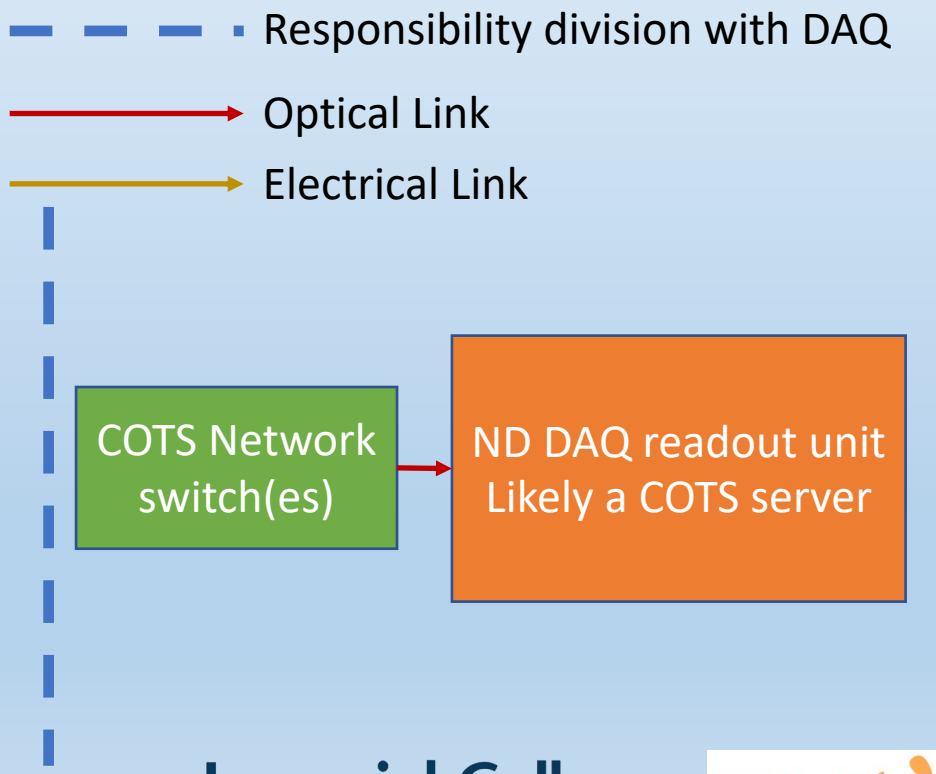




System design – 2) Aggregation

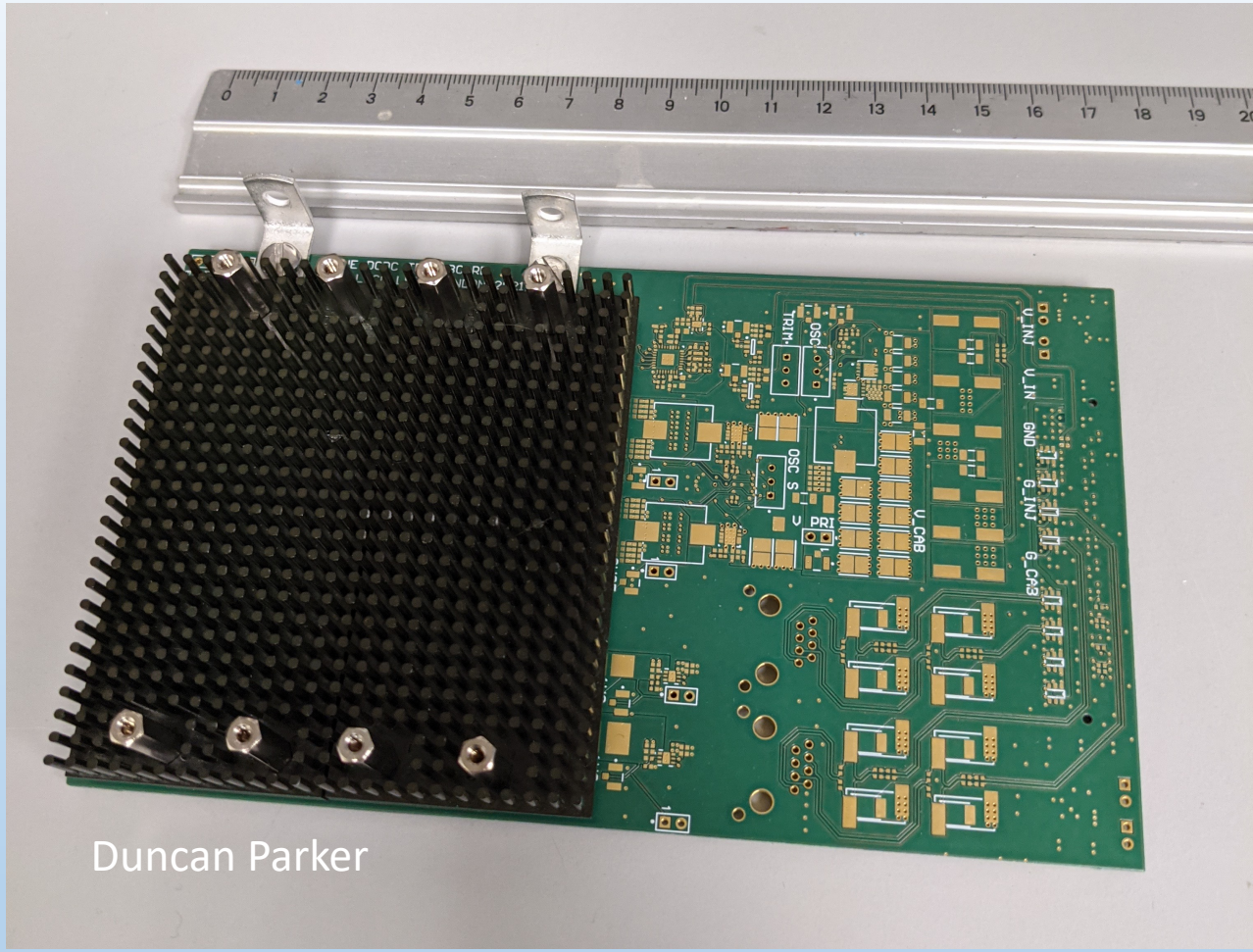
- Each ASIC host card hosts one LArPix digitizer which accepts 64 channels
  - ~11,000 ASIC host cards is still too many to read out of detector at one link per card
- FPGA based (Xilinx Kintex Ultrascale) aggregator cards concentrate data from up to 90 ASIC host cards each





Power test board

- Aggregator must power ASIC host cards and must be inside vessel
  - Implies high magnetic field and pressure
- This part of aggregator board has been designed at Imperial for early tests
- This is also one of the most power-hungry parts of the system so designing it allowed us to deliver accurate heat estimates to facilities



Duncan Parker

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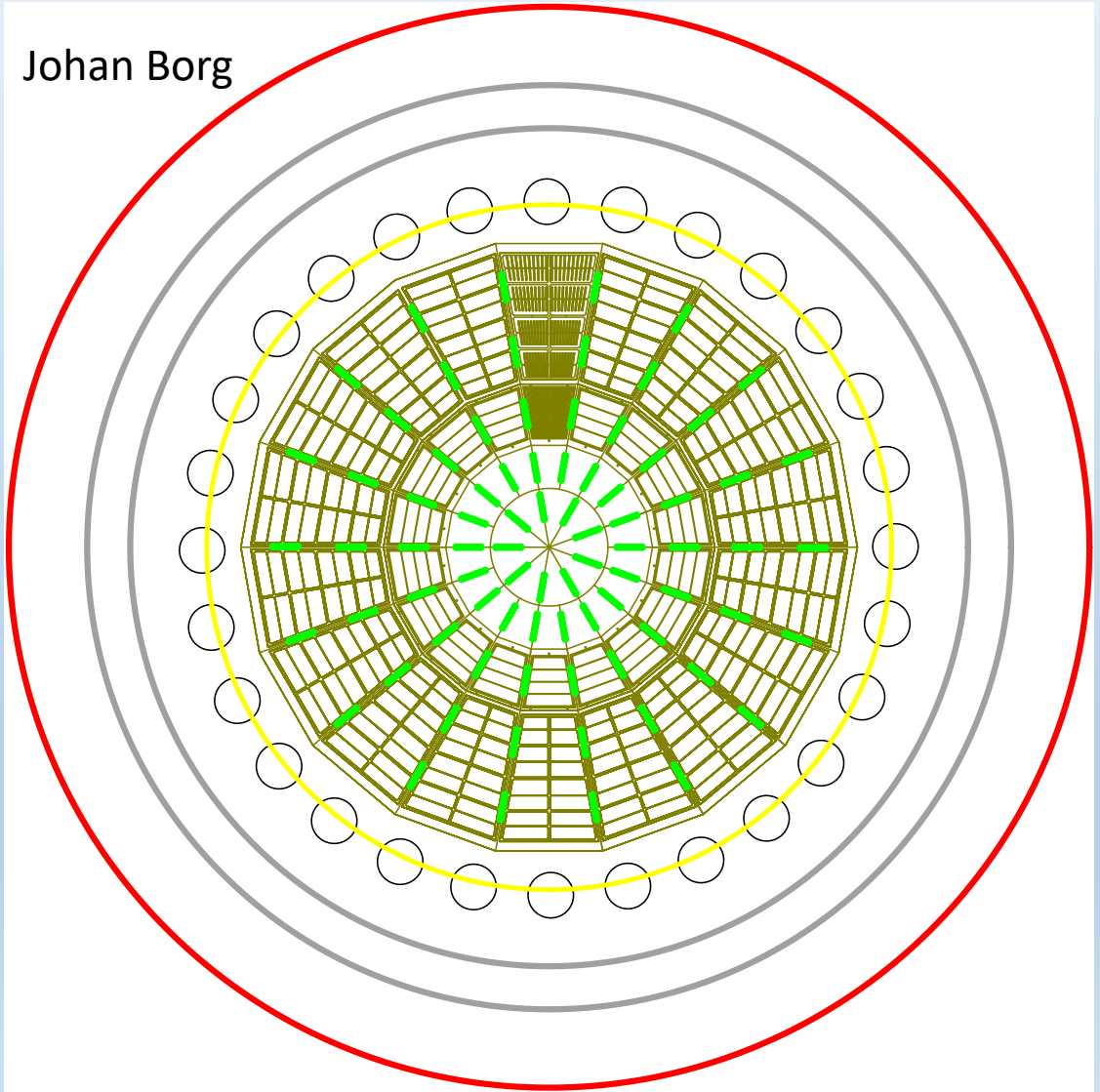
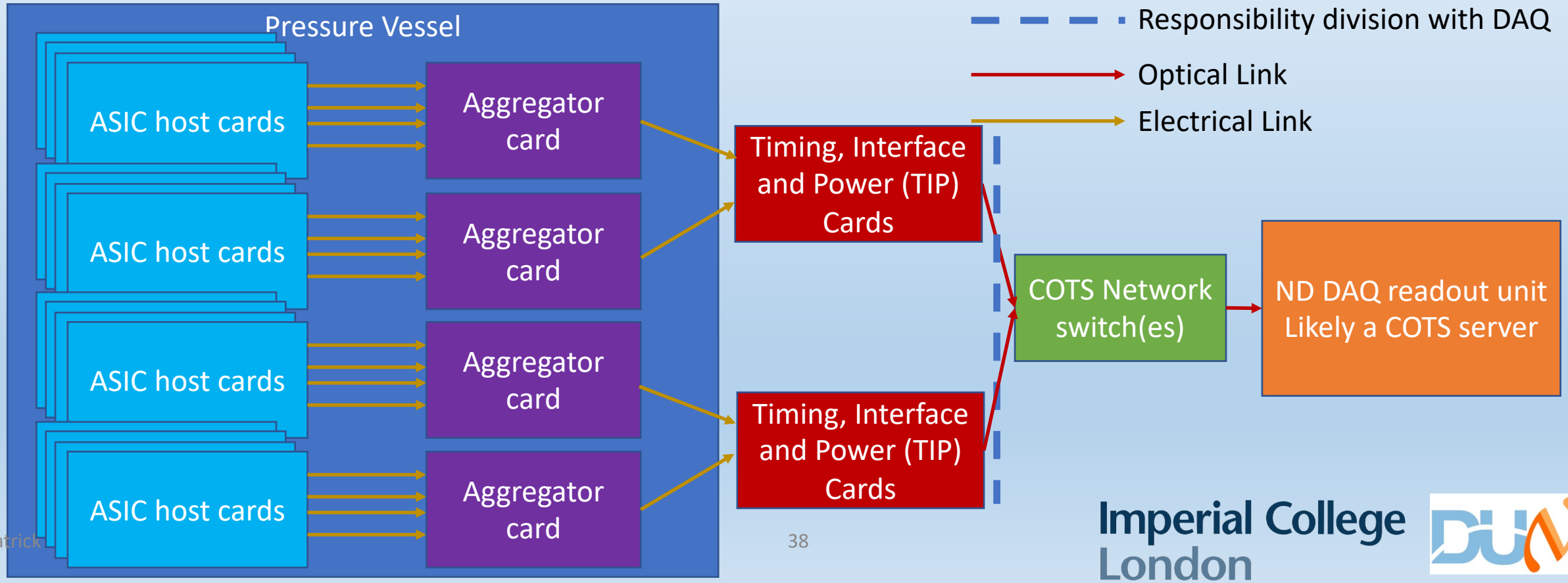
Mechanical Design inside vessel

- ALICE ROCs have slots that each correspond to 64 channels
  - 156 slots per OROC and 90 per IROC
- Plan on 2 aggregators per OROC, 1 per IROC allowing cable lengths to be short
- Assuming a conservative density for central region gives 81 aggregators per end for 162 total (green lines to right)



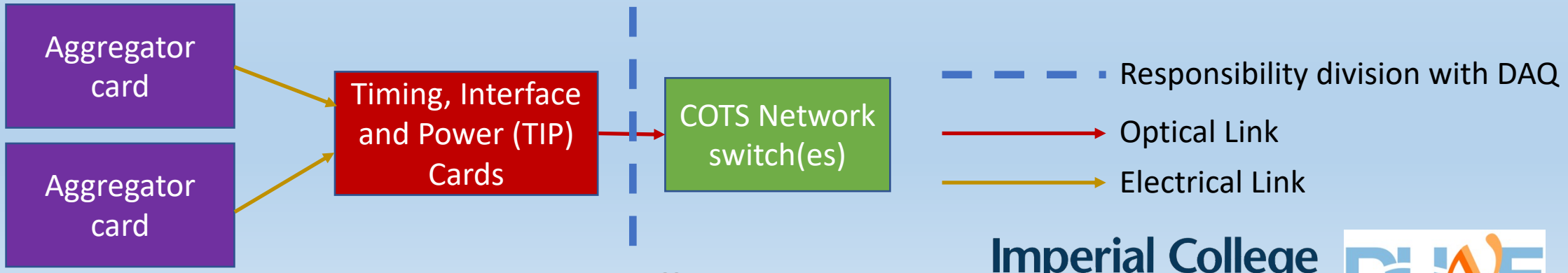
System design – 3) Power DAQ Interface and Timing

- Previously planning to connect aggregator cards direct to DAQ switch
- However, power and timing information must also be sent into vessel and distributed to ASIC host cards. Timing Interface and Power (TIP) cards will do this as well as further data concentration



Timing Interface and Power (TIP) Cards

- TIP cards will use same FPGA based design as aggregator card design with different interface to power and provide timing to aggregators
- Each TIP card controls 9 aggregator cards so there will be 18 of them
- Baseline timing system is that used by far detector Single Phase to reuse existing work
- Previous plan had been to send data out of vessel via optical links however power delivery necessitates electrical feedthroughs into vessel
- If we have electrical links anyway, can we send data over them?



Data and power on same cable

- Data will be sent from aggregators to TIP cards over differential pair
  - Signals encoded by one line voltage increasing and the other dropping
  - These pairs have an average DC voltage that can be used to power electronics
- Tested for data rates similar to ours using CAT6A cables
  - Heating acceptable at 1A current draw
  - Data integrity also looks good
- Will also test this using the power test board
- Takes us from 2 optical cables for data plus connections for power and timing for each aggregator to 8 electrical links per aggregator over standard CAT6A, also means we can use off the shelf RJ45 feedthroughs

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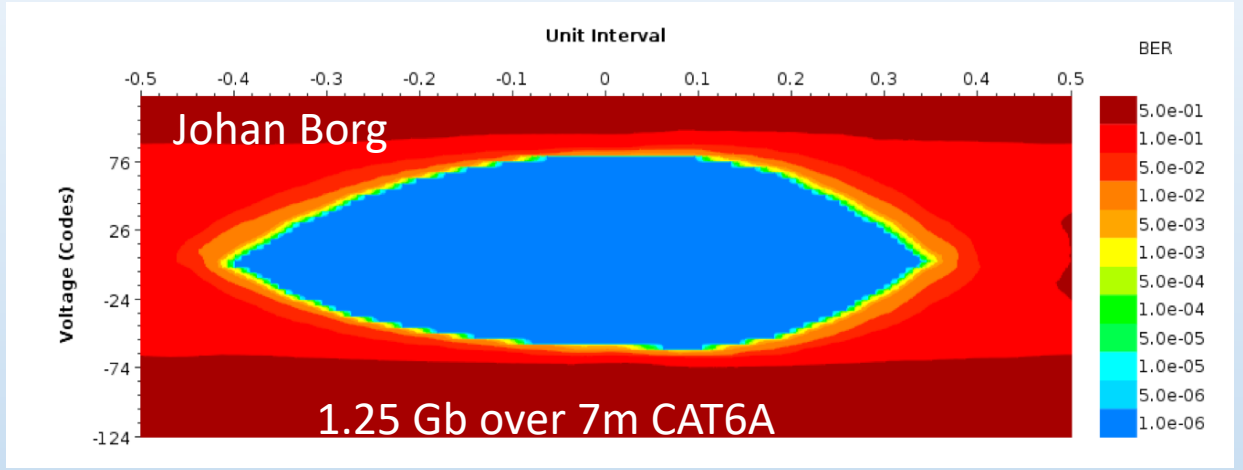

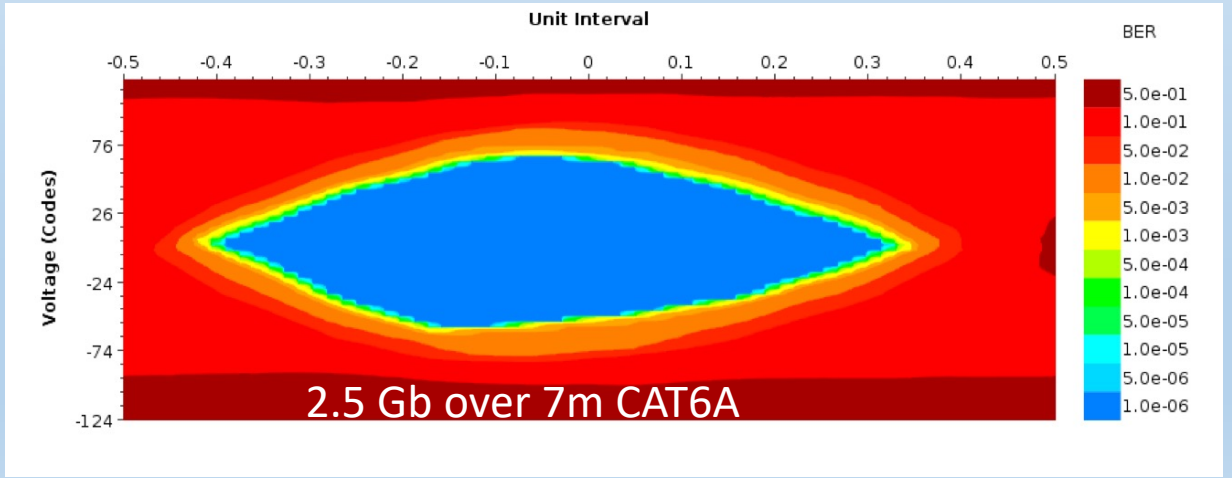

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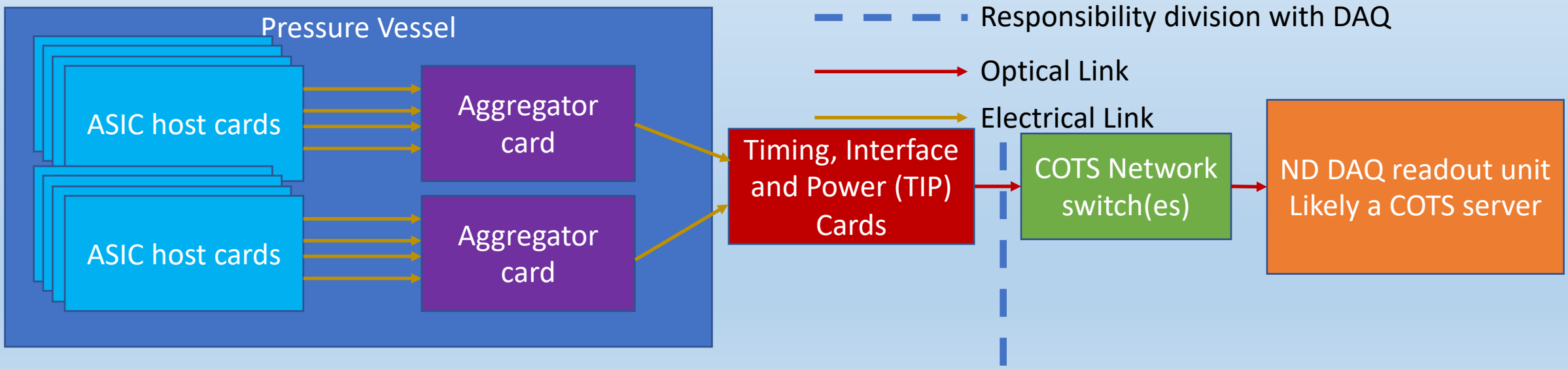
Interface to DAQ

- DAQ group will have ownership of network switch so they can configure it to work with the downstream network and troubleshoot when problems occur
- We have also agreed data will be output over TCP/IP to minimize DAQ effort
  - This is often tricky in an FPGA, but we have identified SiTCP firmware core (used by JPARC main ring) that can do this



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Schedule and beam tests

- Current schedule driven by OROC beam test at FNAL starting in Autumn 2022
- Aim is to have a prototype system ready for this beam test
- We want to have carried out the following before this point:
  - Bench slice test with all three boards (ASIC host, aggregator and TIP) integrated with DAQ system
  - Cosmic ray running at FNAL or London vessel for some time before test beam
  - 2 aggregator cards and 1 TIP card should be able to control a full OROC of ASIC host cards

Summary

- Electronics design is advancing fast with all components in prototyping
- We are working towards providing a first prototype of the full system by the end of the year
- Aiming to use this system for the OROC beam test in the 2022/23 beam time at FNAL test beam facility