131.ND.02.05 Charge Readout: Overview

Brooke Russell, L3 Charge Readout Subsystem Lead

ND-LAr Preliminary Design Review

27 June 2022

Schweizerische Eidgenossenschaft
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U.S. DEPARTMENT OF ENERGY | Office of Science

Who am I

- Brooke Russell
  - Chamberlain Postdoctoral Fellow at Lawrence Berkeley Lab since January 2020
  - Background in accelerator ν physics with LArTPCs from MicroBooNE experiment

Outline

- Scope
- Requirements
- Interfaces
- Procurement, Manufacturing, QA/QC
- Risks and Prototyping
- Recommendations from Previous Reviews
- Cost and Schedule
- Summary

Context

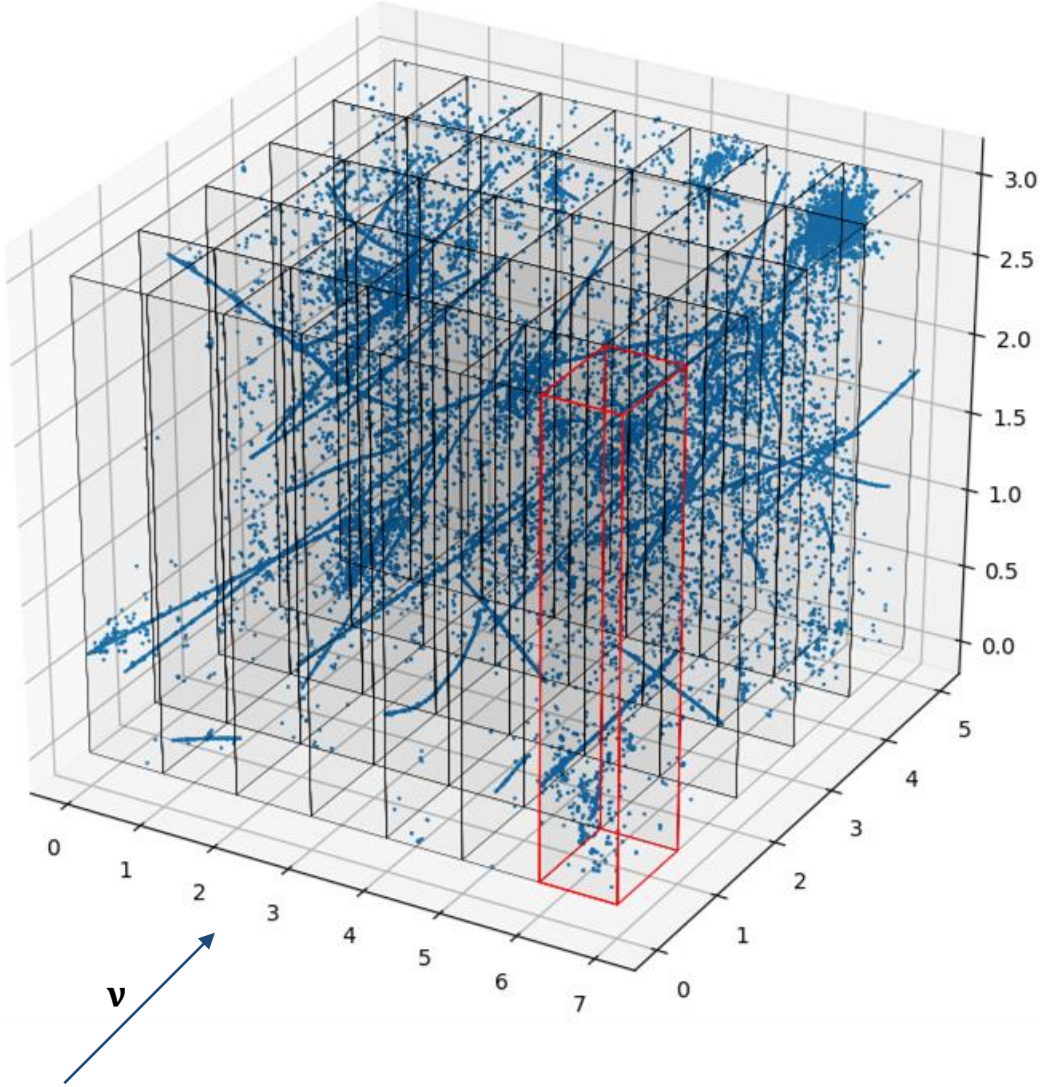
ND-LAr custom design for high-rate LBNF beam

1. Modularity: 35 low-profile TPC modules, 70 optically-isolated drift regions
2. High photodetector coverage: 40% photocoverage
3. Unambiguous 3D charge: low-power, pixelated charge readout

The ND-LAr charge readout system provides unambiguous ν interaction 3D imaging

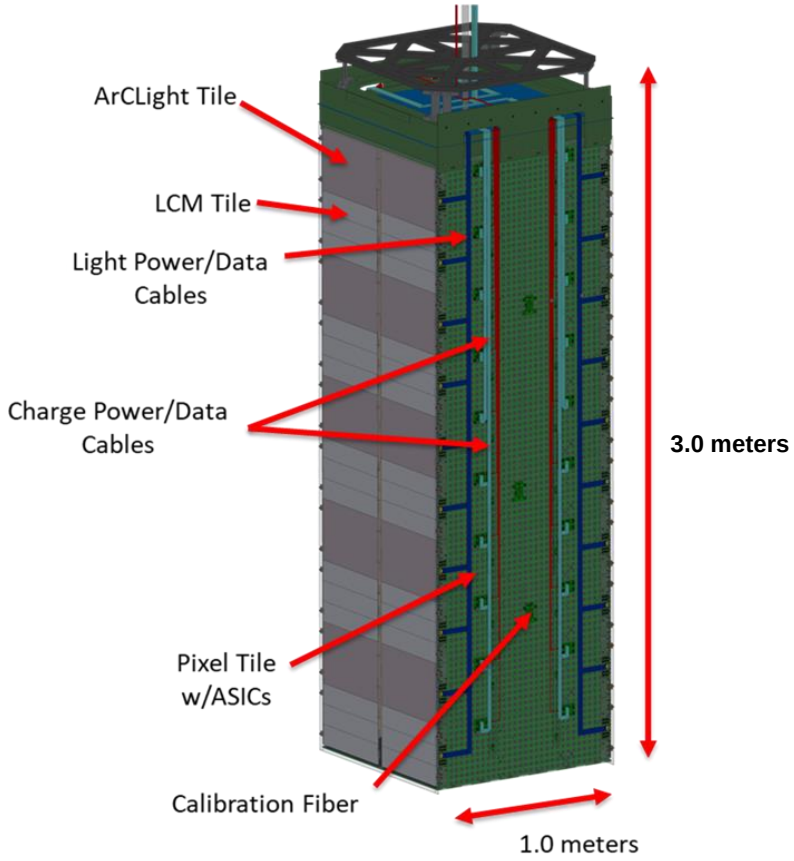
- High-fidelity imaging of large multiplicity neutrino topologies
- Overcome beam neutrino pile-up at high-rate DUNE Near Detector Complex

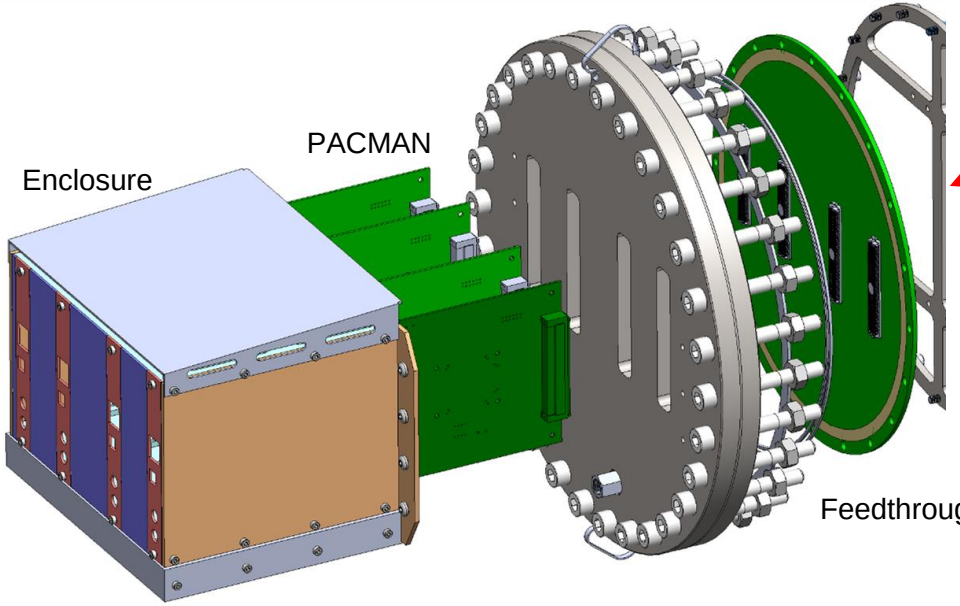
The charge readout system leverages industry for quick-turn prototyping & production at competitive cost



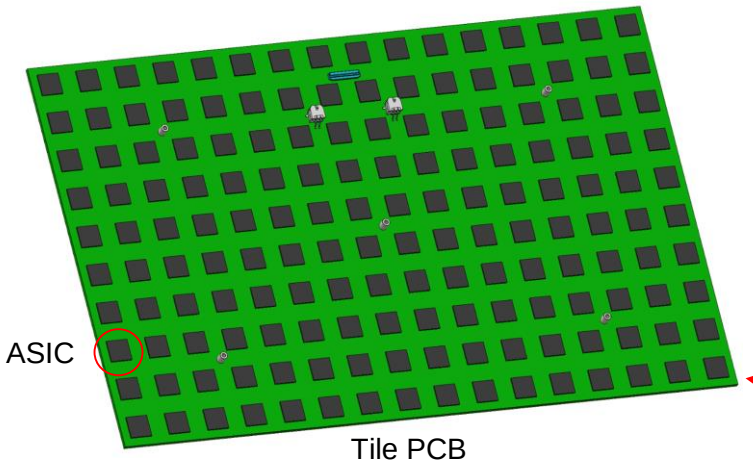
ND LArTPC Module Design

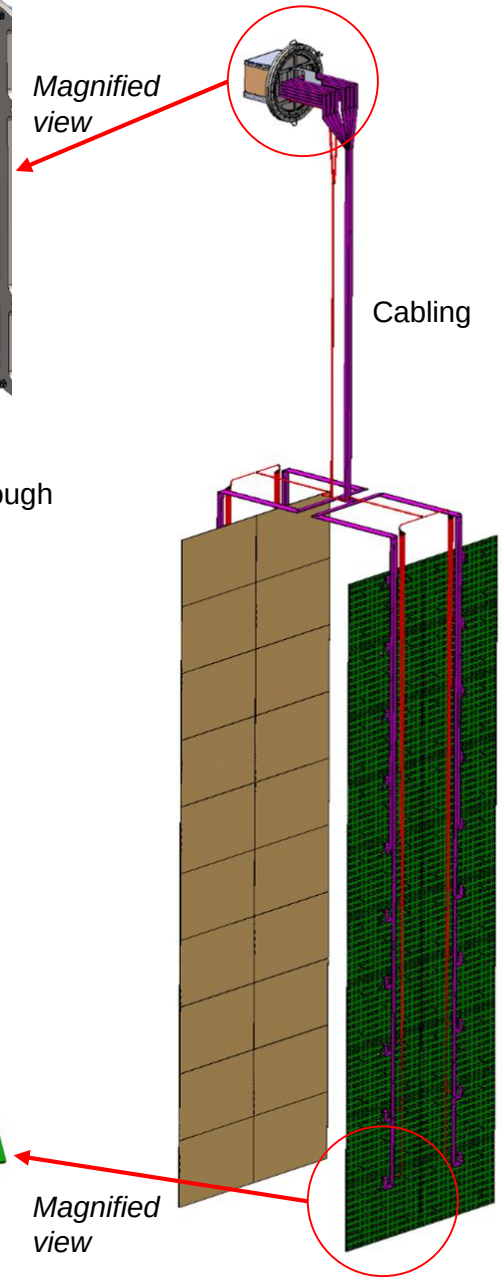
Integrated Module





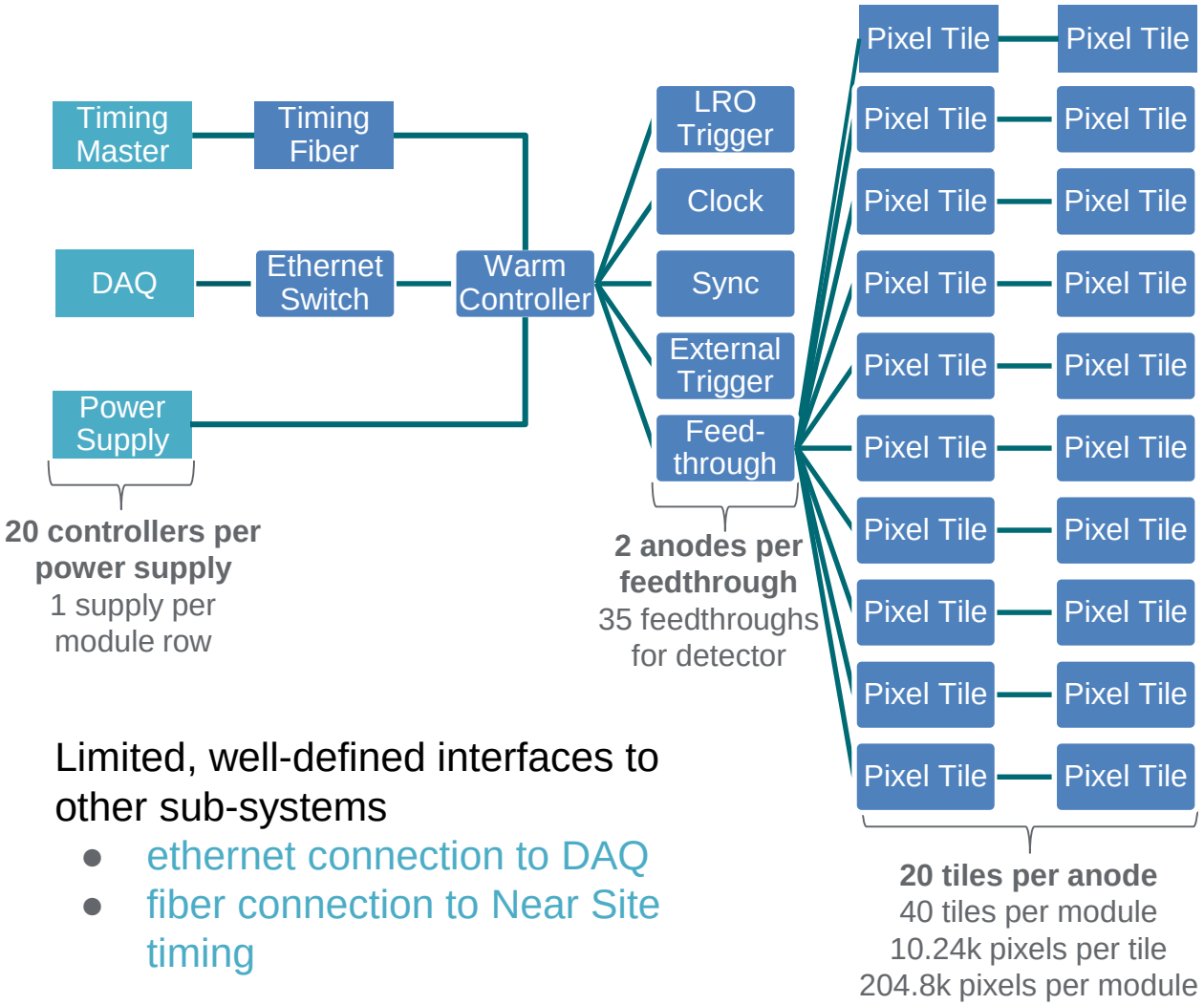
Charge Readout Subsystem





Charge Readout Architecture

A contained, end-to-end system



Limited, well-defined interfaces to other sub-systems

- ethernet connection to DAQ
- fiber connection to Near Site timing

ND-LAr Charge Readout System Institutional Responsibilities

Task	Institutions
ASIC design and production	LBL
ASIC test boards	UPenn
ASIC testing	Caltech
Tile design and production	LBL
Tile testing	UTA
Cables and feedthroughs	Rutgers
PACMAN hardware	UC Davis
PACMAN firmware	UC Irvine
Clock and power	LBL
DAQ interface software	LBL

https://edms.cern.ch/document/2619608

131.ND.02.05 Charge Readout: Scope

Detailed subsystem scope per WBS dictionary

Delineates deliverables, quantities, responsible institutions, and funding source during design, prototyping, production and installation phases

Informed by 2x2 module prototypes and ND-LAr CAD model

Aligned with BOEs and resource-loaded schedule

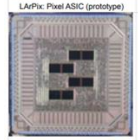
131.ND.02.05: Charge Readout

WBS Dictionary (Concise):

Design and production of the charge readout system for the ND LArTPC modules
Includes:
- Pixel ASICs
- Pixel Anode Tiles
- Cabling and feedthroughs
- (Warm) Control Interface Electronics and enclosures
- Control, configuration, and readout software/firmware
- Electronics power supplies, power cables
- Clock distribution/synchronization system
- Component testing/QA/QC, and associated tooling
- Prototypes for 2x2, Full-scale Demonstrator
- Packaging and shipping
- Support personnel for prototyping, A&T, and I&I, and their travel

Reference CAD Image(s):

LArPix: Pixel ASIC (prototype)



PACMAN Controller (prototype)

PACMAN Feedthrough (prototype)

Pixel Anode Tile (prototype)

Task/Item	Qty	Spares	Institutions	Funding Source	Funding Status	Detailed description
Pixel ASICs	320000	66691	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Pixel Anode Tiles	1400	600	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Tile Data Cables	1400	600	Rutgers	DUNE-US Project	Allocated	Specification and procurement
Tile Power Cables	140	28	Rutgers	DUNE-US Project	Allocated	Specification and procurement
Charge Readout Feedthroughs	35	5	Rutgers	DUNE-US Project	Allocated	Design, production, and assembly
PACMAN Controllers (hardware)	140	60	UC-Davis	DUNE-US Project	Allocated	Design, production, and assembly
PACMAN Controllers (firmware)	-		UC-Irvine	DUNE-US Project	Allocated	Design, production, and assembly
PACMAN Enclosures	35	5	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Power Supplies	7	1	LBNL	DUNE-US Project	Allocated	Specification and procurement
Ethernet Cables	140	60	LBNL	DUNE-US Project	Allocated	Specification and procurement
Data Cables	140	60	LBNL	DUNE-US Project	Allocated	Specification and procurement
Clock System Fibers	140	60	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Packaging and shipping	-		Various	DUNE-US Project	Allocated	Packaging and shipping to MATF
Assembly Procedures	-		Various	DUNE-US Project	Allocated	Subsystem procedures for use during A&T and I&I
Support during ND A&T	-		Various	DUNE-US Project	Allocated	Technical/scientific support during TPC Module assembly and test program at the MATF, including travel.
Support during ND I&I	-		Various	DUNE-US Project	Allocated	Technical/scientific support during TPC Module installation and integration at the DUNE Near Detector Site, including travel.
QA/QC and characterization						
Pixel ASIC: Socket Test PCBs			U-Penn	DUNE-US Project	Allocated	Design, production, and assembly
Pixel ASIC: High-Volume Testing			Caltech	DUNE-US Project	Allocated	Bench qualification tests of Pixel ASICs before assembly to pixel tiles
Pixel ASIC: Characterization			UCSD, UC-Irvine	DUNE-US Project	Allocated	Detailed bench-testing of Pixel ASICs to inform design
Pixel Tile: RT Characterization			CSU/Yale/Syracuse	DUNE-US Project	Allocated	Detailed bench-testing of Pixel Tiles to inform design
Pixel Tile: Cryo Characterization			CSU/Yale/Syracuse	DUNE-US Project	Allocated	Detailed cryo-testing of Pixel Tiles to inform design
Pixel Tile: Cryo-test TPCs			LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Pixel Tile: Cryo-test Apparatus			LBNL	DUNE-US Project	Allocated	Design, production, assembly, and operation
Pixel Tile: Room-temp QA/QC			LBNL	DUNE-US Project	Allocated	Bench qualification tests
Pixel Tile: RT QA/QC Enclosures			LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Pixel Tile: Cryo QA/QC			UTA	DUNE-US Project	Allocated	Cryo-qualification tests of Pixel Tiles
Pixel Tile: Cryo QA/QC Apparatus			UTA	DUNE-US Project	Allocated	Design, production, assembly, and operation
Tile Data Cables: QA/QC			Rutgers	DUNE-US Project	Allocated	Bench qualification tests
Tile Power Cables: QA/QC			Rutgers	DUNE-US Project	Allocated	Bench qualification tests
CR Feedthroughs: QA/QC			Rutgers	DUNE-US Project	Allocated	Bench qualification tests
PACMAN Controllers: QA/QC			LBNL/UC-Davis	DUNE-US Project	Allocated	Bench qualification tests
Clock System: QA/QC			LBNL/UC-Irvine	DUNE-US Project	Allocated	Bench qualification tests
Prototypes for 2x2						
Pixel ASICs	6400	1600	LBNL	LBNL (in-kind)	Funded	Design, production, and assembly
Pixel Anode Tiles	64	16	LBNL	LBNL (in-kind)	Funded	Design, production, and assembly
Tile Data Cables	64	16	Rutgers	LBNL (in-kind)	Funded	Specification and procurement
Tile Power Cables	8	4	Rutgers	LBNL (in-kind)	Funded	Specification and procurement
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PACMAN Controllers (hardware)	8	4	UC-Davis	LBNL (in-kind)	Funded	Design, production, and assembly
PACMAN Controllers (firmware)	-		UC-Irvine	LBNL (in-kind)	Funded	Design, production, and assembly
PACMAN Enclosures	8	4	LBNL	LBNL (in-kind)	Funded	Design, production, and assembly
Power Supplies	1	1	LBNL	LBNL (in-kind)	Funded	Specification and procurement
Power Cables	8		LBNL	LBNL (in-kind)	Funded	Specification and procurement
Ethernet Cables	8		LBNL	LBNL (in-kind)	Funded	Specification and procurement
Clock System	1		LBNL	LBNL (in-kind)	Funded	Design, production, and assembly
Packaging and shipping	-		Various	LBNL (in-kind)	Funded	Packaging and shipping to Bern
Assembly Procedures	-		Various	LBNL (in-kind)	Funded	Subsystem procedures for use during 2x2 assembly and testing
Support during 2x2 A&T at Bern	-		Various	LBNL (in-kind)	Funded	Technical/scientific support during TPC Module assembly and test program at Bern, including travel.
Support during 2x2 Beam Test	-		Various	LBNL (in-kind)	Funded	Technical/scientific support during 2x2 Beam Test @ FNAL, including travel.
Prototypes for FSD						
Pixel ASICs	19200	2455	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
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Charge Readout Feedthroughs	1	9	Rutgers	DUNE-US Project	Allocated	Design, production, and assembly
PACMAN Controllers (hardware)	4	2	UC-Davis	DUNE-US Project	Allocated	Design, production, and assembly
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PACMAN Enclosures	1	1	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Power Supplies	1	1	LBNL	DUNE-US Project	Allocated	Specification and procurement
Power Cables	4	1	LBNL	DUNE-US Project	Allocated	Specification and procurement
Ethernet Cables	4	1	LBNL	DUNE-US Project	Allocated	Specification and procurement
Clock System	-		LBNL	DUNE-US Project	Allocated	Design, production, and assembly
Packaging and shipping	-		Various	DUNE-US Project	Allocated	Packaging and shipping to MATF
Assembly Procedures	-		Various	DUNE-US Project	Allocated	Subsystem procedures for use during A&T and I&I
Support during FSD A&T	-		Various	DUNE-US Project	Allocated	Technical/scientific support during TPC Module assembly and test program at the FSDTF, including travel.

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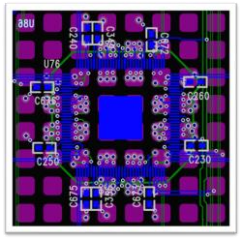
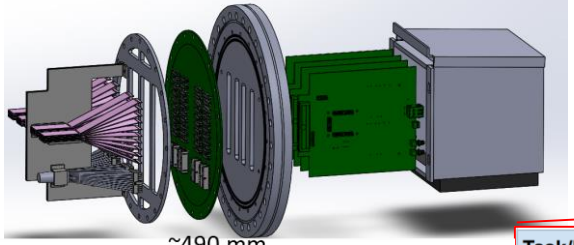
131.ND.02.05 Charge Readout: Scope

Readout controllers, feedthrough, & enclosure

ASIC PCB Layout

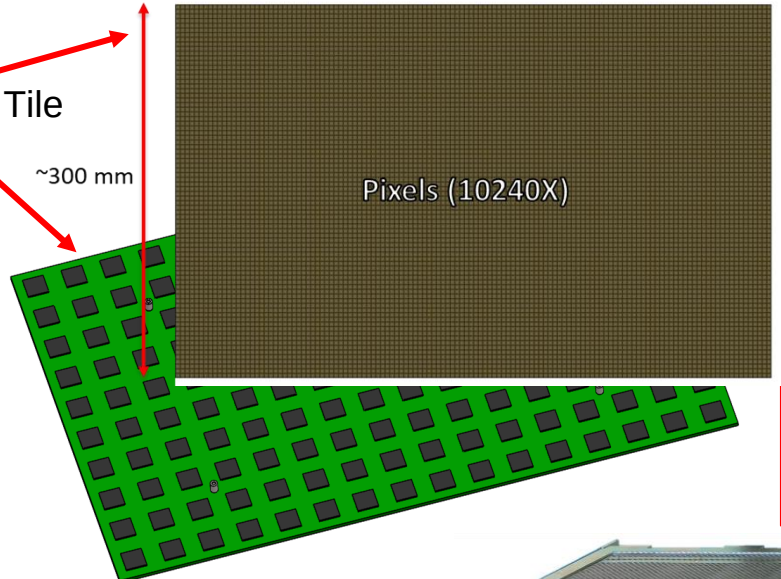


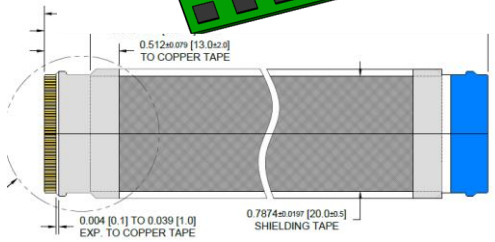


~490 mm

Pixel Tile

~300 mm





Data Cable

Power Supply

Production phase deliverables

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PACMAN Enclosures	35	5	LBNL
Power Supplies	7	1	LBNL
Ethernet Cables	140	60	LBNL
Data Cables	140	60	LBNL
Clock System Fibers	140	60	LBNL
Packaging and shipping	-		Various
Assembly Procedures	-		Various
Support during ND A&T	-		Various
Support during ND I&I	-		Various

DUNE-SP Timing Master

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Reference CAD Image(s):

LArPix: Pixel ASIC (prototype) | PACMAN Controller (prototype) | PACMAN Feedthrough (prototype) | Pixel Anode Tile (prototype)

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PACMAN Enclosures	1	1	LBNL	DUNE-US Project	Allocated	Design, production, and assembly
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Power Cables	4	1	LBNL	DUNE-US Project	Allocated	Specification and procurement
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LBNF/DUNE

https://edms.cern.ch/document/2589287

131.ND.02.05 Charge Readout: Requirements

Materials produced to date meet vast majority of requirements

- Validated with 2x2 program

Requirement	Design Value	Status
Multi-hit separation time	< 3 μs	2.6 μs
Spatial resolution	< 4.7 mm	3.7 mm
Pixel efficiency	> 90%	80%
Noise	< 1000 e- ENC	850 e- ENC
Tile leakage current	<< 1 ke- / 500 μs	< 5 e- / 500 μs
Dynamic range	> 180 ke-	> 200 ke-
Power dissipation	< 3.9 kW	< 2.24 kW

Primary focus moving forward: quality control in mass production

Name	Primary Text	Value	Rationale
3D Pixel Charge Readout	The ND LArTPC shall use unambiguous 2D pixelated charge readout anodes (unique electronics channel for every anode pixel) in order to achieve accurate 3D charge imaging.		Outcome of comparative studies of the performance of 2D versus 3D readout in the ND environment
Pixel Spacing	The pixel spacing for the ND readout shall provide spatial resolution < 4.7 mm	< 4.7 mm	The pixel spacing for the ND readout shall provide spatial resolution as good as the far detector.
Multi-Hit Separation Time	Pixel sampling time shall be < 3 µs	< 3 µs	The pixel sampling time should provide equivalent spatial resolution in the drift direction as in the transverse directions.
Pixel noise	The noise (uncertainty) in the measurement of ND pixel charge shall be < 1000 electrons	< 1000 electrons	The noise (uncertainty) in the measurement of ND pixel charge should be as good as the FD specification. The noise must be low enough to enable stable pixel self-triggering for 1/4-MIP signals
Pixel Saturation Level	The pixel electronics shall have sufficient dynamic range such that it saturates at >180,000 electrons	>180,000 electrons	Pixel electronics should have sufficient dynamic range for high multiplicity heavily ionizing particles at the neutrino vertex typical of LBNF nu-Ar interactions
Pixel Charge Resolution	The charge resolution of the pixel channel should not limit signal fidelity.	< 3% sigma_Q/Q	The resolution contributed by the pixel electronics should be smaller than the intrinsic (Landau) fluctuations for MIP signals.
Pixel Linearity (post-cal)	The linearity error shall be better than 2%	< 2%	The linearity is one component of the pixel charge resolution (in addition to the pixel noise). Combined, these should be < 3%.
Pixel Efficiency	The pixel channels shall be > 95% efficient for signals greater than 1/4 MIP track traversing full pixel pitch	> 95%	The channel efficiency should be high enough that we do not lose signal fidelity, particularly for MIP-level or larger signals.
Instrumented Anode Area	The instrumented area of the anode shall not introduce substantial dead volume.	> 99%	The uninstrumented area of the anode should not be a driving factor in total dead volume of the ND. This can be delivered by design.
Pixel Multiplexing	Each IO cable shall control and readout > > 1000 pixels	> 1000	Driven by heat conduction from feedthru, impurities especially in gas region, spacing and reliability
Bad Pixel Fraction	The fraction of pixels outside of performance specs shall be < 5%	< 5%	Isolated loss of pixels can generally be compensated by reconstruction algorithms. The fraction of pixels outside of performance specs should be low enough to have negligible impact to the physics capabilities of the ND.
Bad ASIC Fraction	The fraction of dead ASICs should be low enough to have negligible impact to the physics capabilities of the ND.	< 3%	Loss of clusters of pixels (currently 64) associated with a given ASIC can generally be compensated by reconstruction algorithms (to some extent). Short track stubs (<few cm) may be lost/biased.
Dead Pixel Tile Fraction	The fraction of dead pixel tiles shall be < 0.1%	< 0.1%	Loss of a complete pixel tile is difficult to compensate via reconstruction algorithms. It introduces a substantial dead volume within the LArTPC, biasing event selection and pileup rejection. This may likely require detector servicing to restore detector physics performance. There are roughly ~1400 pixel tiles in the ND, hence <0.1% dead tiles.
Pixel Failure Rate	The rate of pixel failure during operation should be low enough to avoid substantial impact to physics performance of the ND during the lifetime of the experiment.	< 0.5% / year	Maintain less than 5% total sub-spec pixel fraction after 10yrs (?) of operation.
ASIC Failure Rate	The rate of ASIC failure during operation should be low enough to avoid substantial impact to physics performance of the ND during the lifetime of the experiment.	< 0.3% / year	Maintain less than 3% total dead ASIC fraction after 10yrs (?) of operation.
Pixel Tile Failure Rate	The rate of pixel tile failure during operation should be low enough to avoid substantial impact to physics performance of the ND during the lifetime of the experiment.	< 0.01% / year	Maintain less than 0.1% total dead tile fraction after 10yrs (?) of operation.
Pixel Tile I/O channels redundancy	The number of redundant pixel tile data input/output channels should be sufficient such that expected loss of ASICs does not result in failure of I/O to the entire tile.	> 2	Each input channel talks to one unique 'root node' ASIC on the tile. With at least 3 redundant input/output channels, the odds of failure of all three root nodes is small enough to reduce the odds of loss of any tile due to I/O failure to less than 0.1%.
Pixel Data Loss Fraction	The fraction of pixel data lost during readout should be negligible.	< 0.1%	A loss of 0.1% of pixel hit data should be easy to achieve technically, and would be insignificant to the physics performance of the detector.
Heat Dissipation	Charge readout heat generation in LAr shall be < 3.9 kW	< 3.9 kW	Charge readout heat generation in LAr shall be within the agreed cooling capacity of the cryogenic infrastructure.
Heat density	Pixel tile maximum heat density shall be < 20mW / ASIC	< 20mW / ASIC	Boiling of LAr poses two risks: bubble motion near pixel induces noise, bubble presence in high field gradient (e.g. drift region) can induce HV discharge. Both can be very detrimental to physics performance of the detector.
Charge Readout Electron Lifetime Reduction	Emission of electronegative impurities (O2, H2O) from the charge readout components shall be less than 0.1 ppm/day (TBC)	0.1 ppm / day (TBC)	At this emission rate, and considering the cryogenics system recirculation rate, the impact on electron lifetime should be small compared to the requirement

https://edms.cern.ch/document/2746199/1

LArPix ASIC

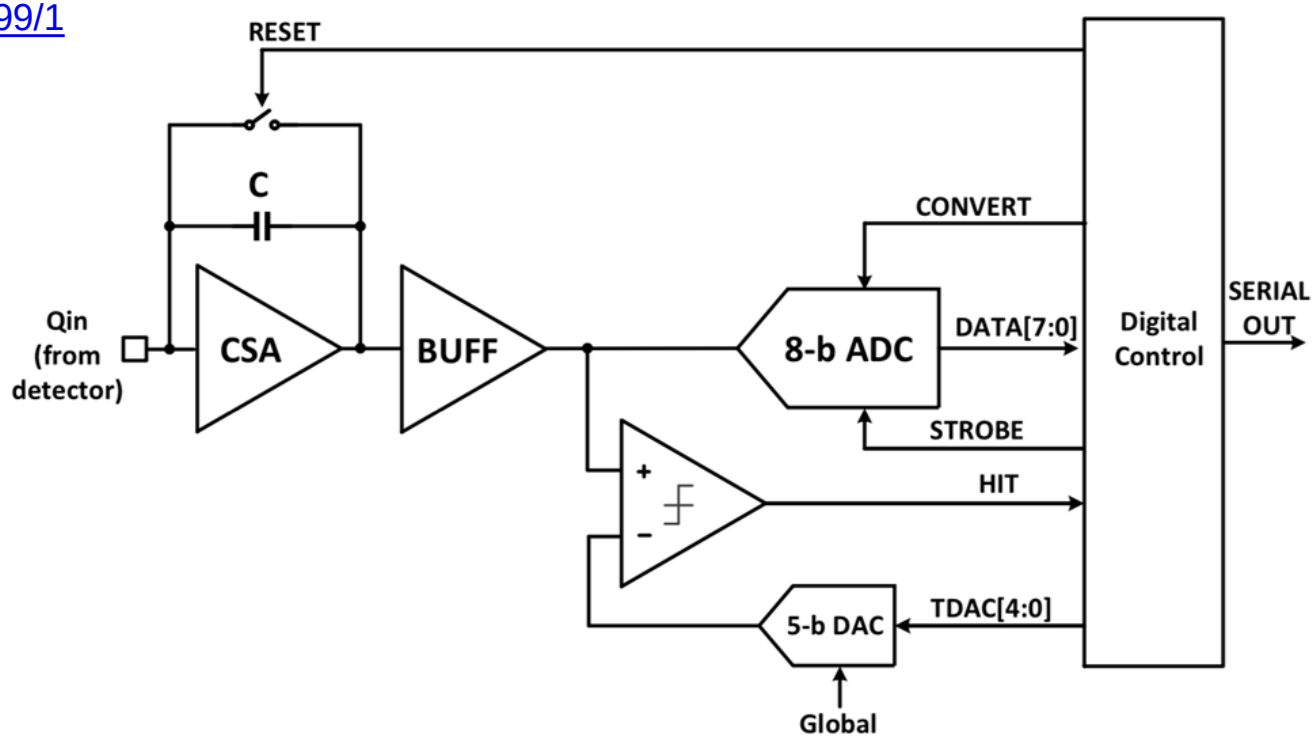
Low-power, integrating amplifier with self-triggered digitization and readout

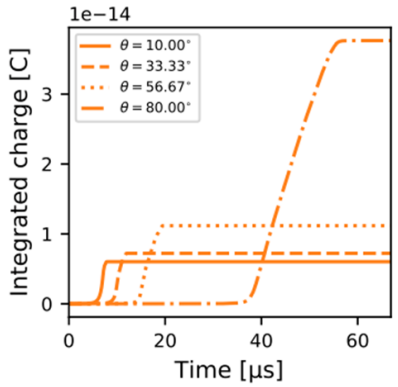
Pixel dormant until signal exceeds tunable threshold

- Integrates charge for ~3 μs (~4 mm drift), then digitizes
- Ready for next signal

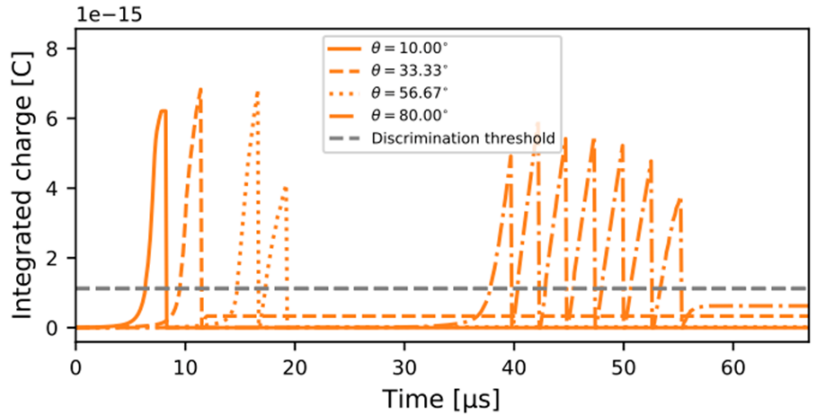
Pixels are continuously active

- ~100M cosmic-ray events recorded in prototypes
- Serial I/O data rate is slow (~5 Mb/s per channel) to limit digital power
- Modest data volumes: ~1 MB/s per square meter of anode in surface cosmic flux





Simulated front-end charge integration



Incorporation of buffering, ADC sampling, and digitization

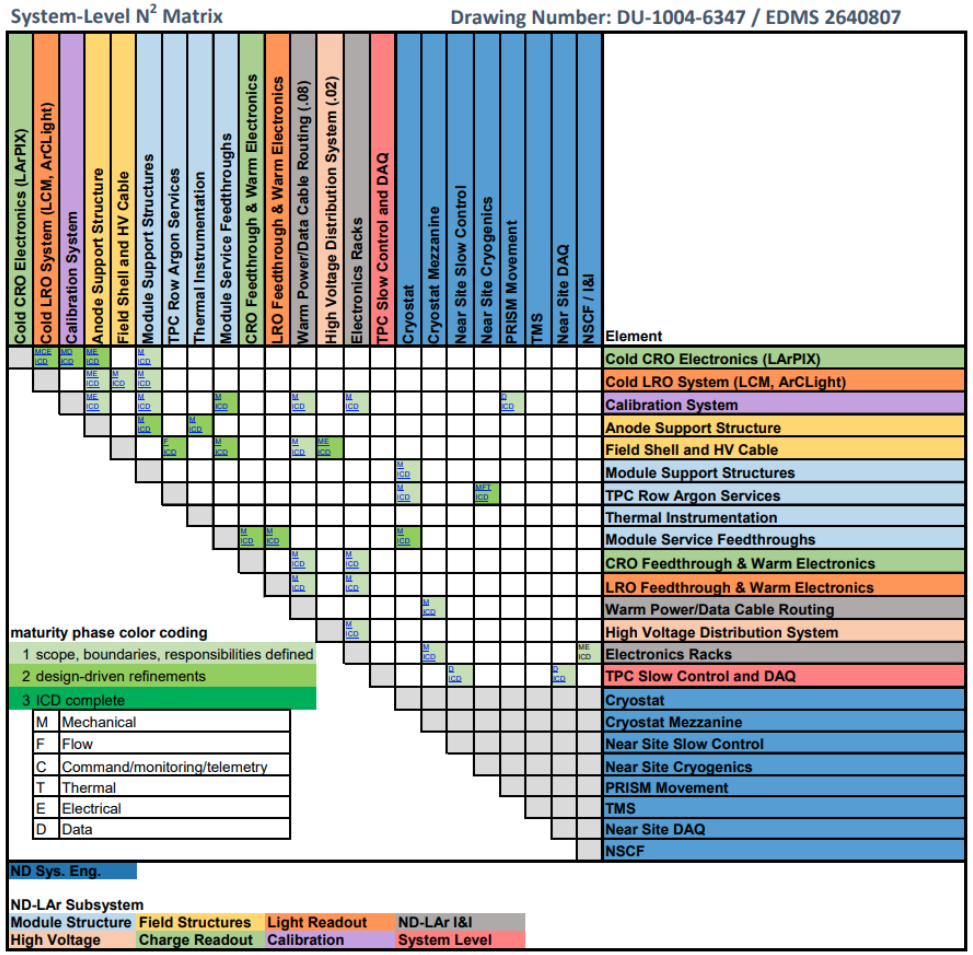
https://edms.cern.ch/project/CERN-0000223195

Interfaces

- Engineering CAD model captures interfaces, https://edms.cern.ch/project/CERN-0000226247
- Interfaces realized and validated in 2x2 program

Subsystem	Interface	Maturity
Anode support structure	Mechanical	Partially defined
Anode support structure	Cabling	Defined
Calibration system	Mechanical	Partially defined
Dewar structure	Cabling, Feedthrough	Defined
Light readout	Trigger	Defined
DAQ	Data IO & control	Defined
Timing	Fiber & transceiver	Defined
Facilities	Rack AC	Defined
Cryostat structure	Cables & rackspace	Defined

Defined = meets preliminary design maturity

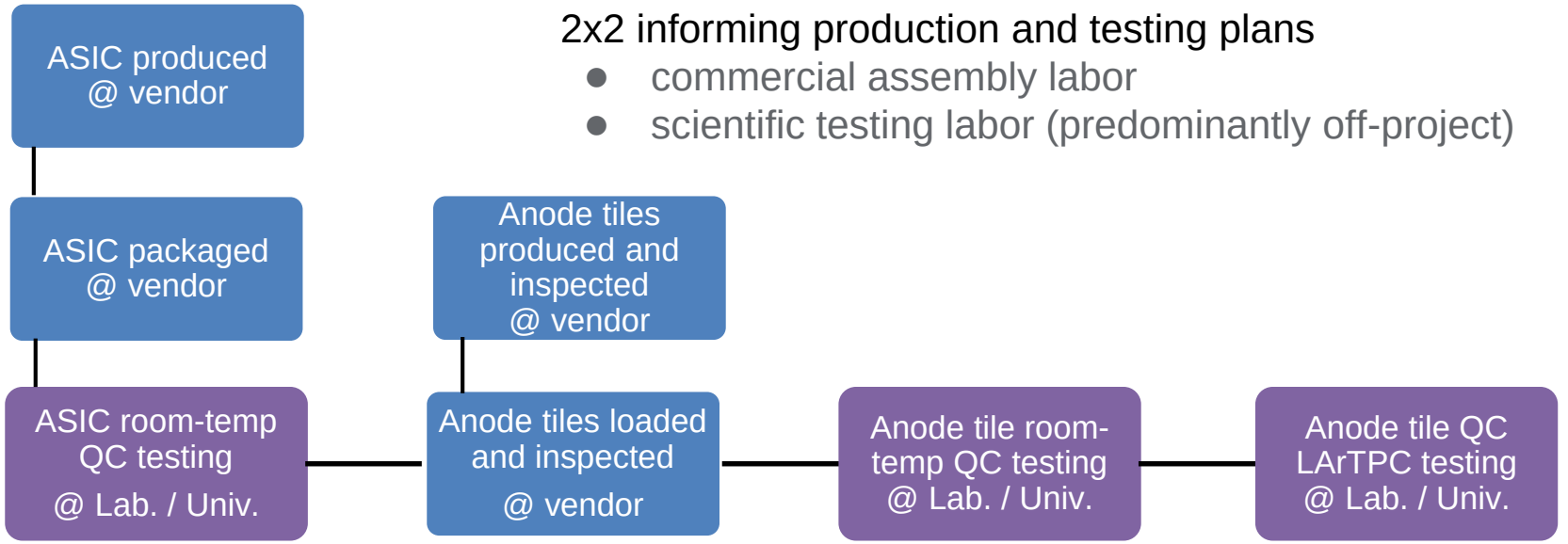


131.ND.02.05 Charge Readout: QA/QC, Procurement, Manufacturing

https://edms.cern.ch/document/2605601
https://edms.cern.ch/document/2605603
https://edms.cern.ch/document/2605602

15 national laboratory & university partners participating in QA/QC

2x2 informing production and testing plans
- commercial assembly labor
- scientific testing labor (predominantly off-project)



Current:
~10k ASICs tested manually & robot
~1 min/chip
~20% sub-spec performance

Current:
~50 tiles tested
~45 minutes/tile
2 of 5k chips DOA
~20 chips replaced

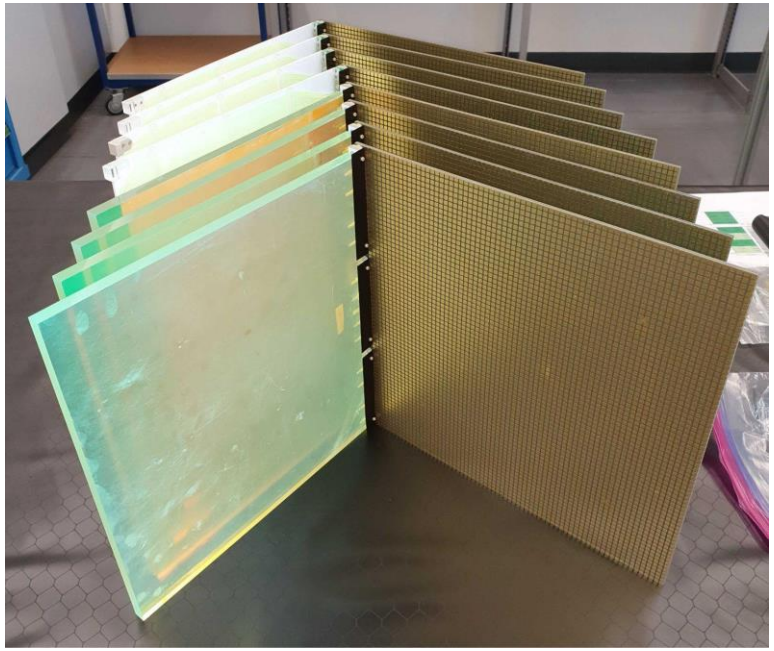
Current:
35 tiles tested in prototype detectors
1 chip failure at cold

https://edms.cern.ch/document/2459149

131.ND.02.05 Charge Readout: Prototyping

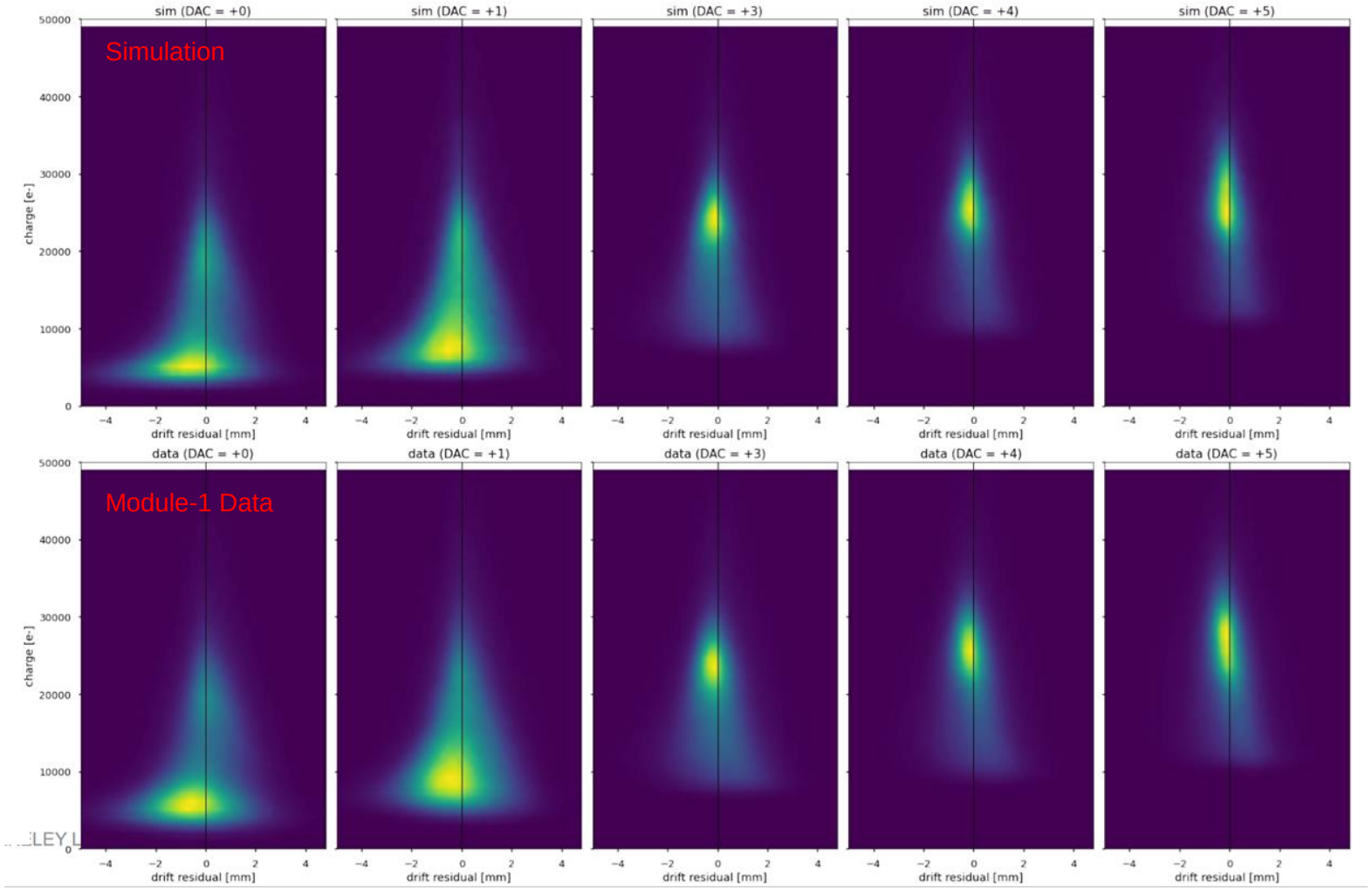
2x2 program substantially advanced technical maturity of charge readout system

- Charge readout design is mature
  - no gaps in scope
- Design efficacy evaluated with prototype data
- >10k ASICs and O(100) pixel tiles tested



Pixel Response Validation

Varying pixel thresholds, good data-MC agreement in low-level front-end response



https://edms.cern.ch/document/2459149

131.ND.02.05 Charge Readout: Prototyping

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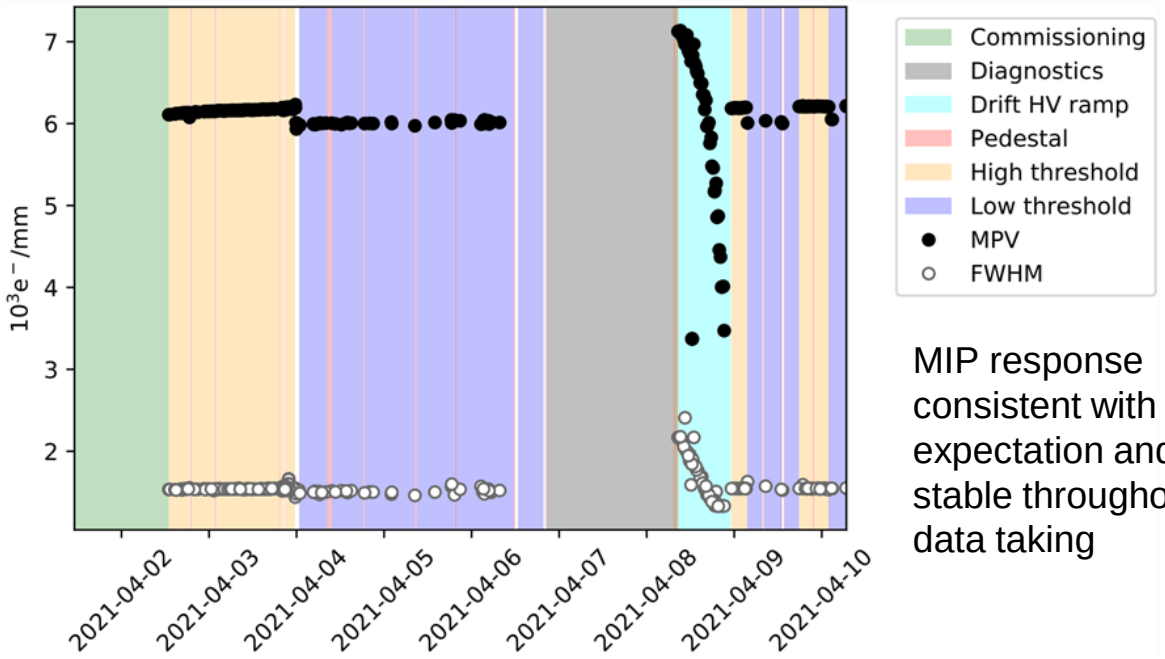
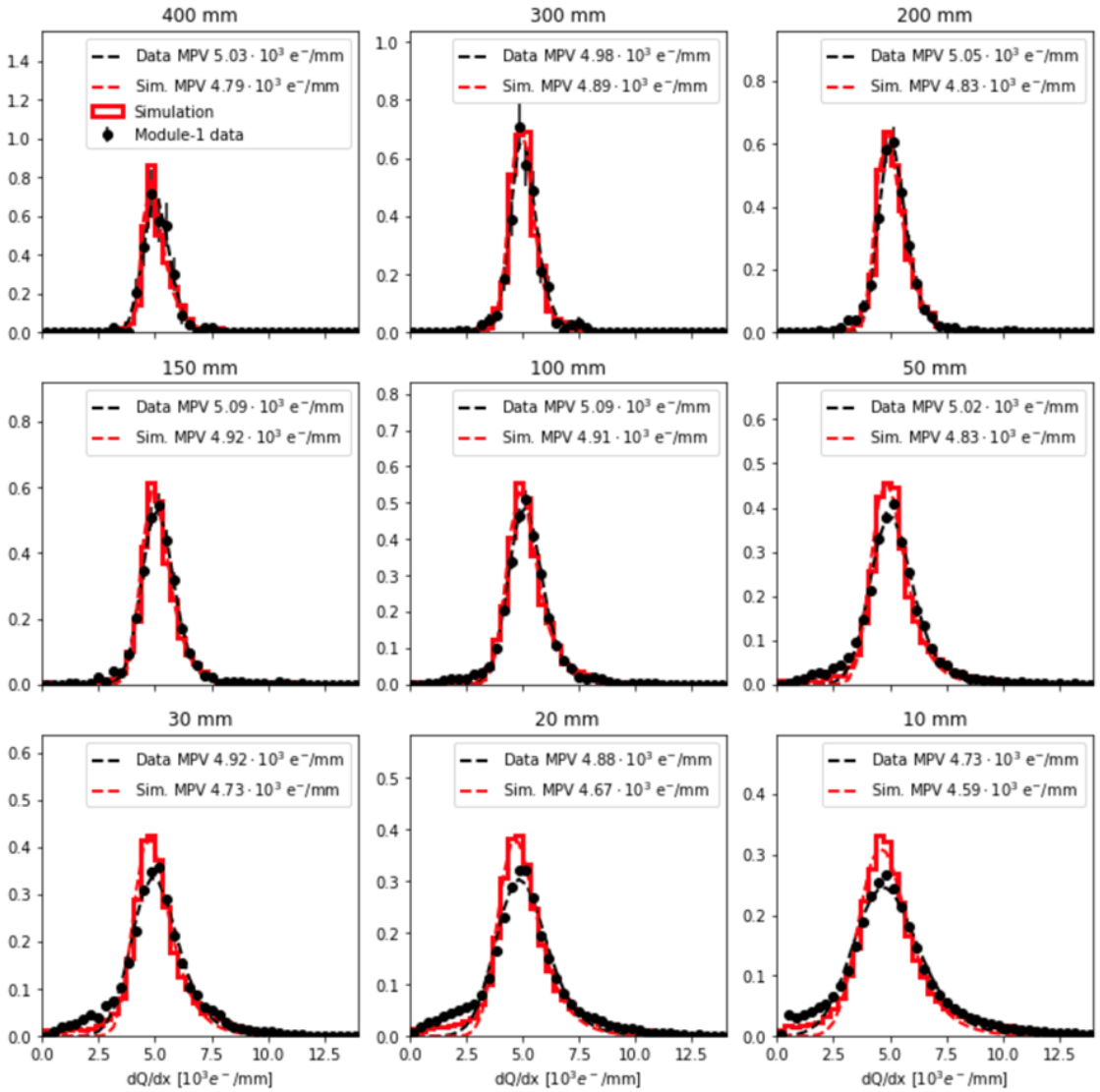


MIP response consistent with expectation and stable throughout data taking

Track-level Cosmic-ray Analysis



https://edms.cern.ch/document/2589288

131.ND.02.05 Charge Readout: Risks

Risks actively tracked through Consortium risk registry. Most impactful risks highlighted here

Title	Summary	Mitigation	Probability	Schedule Impact [Months]	Cost Impact [$k]
ASIC foundry access for engineering runs	IF we lose access to non-US ASIC foundry for LArPix engineering runs, THEN we will need additional funds to procure full runs	None	100% - realized -	6-12-24	500-1000-2000
Loss/limitation to produce prototype ASICs	IF ability to produce prototype ASICs is lost or limited through the duration of design phase, THEN we will need additional resources/time to migrate to a different technology and/or ASIC foundry	ASIC technology migration to 12” wafer (from 8” wafer) to enable long term support of technology at TSMC more likely	20%	12	1000
Insufficient quality control of off-shore produced PCBs	IF quality control over off-shore PCB quality is insufficient THEN production will be moved on-shore to ensure consistent quality	Hold schedule and cost reserves for possible on-shore production	45%	0-1-3	500-1000-1500
Charge readout data cable incompatible with LAr	IF the selected charge readout data cables proves incompatible with liquid argon, THEN a new cable technology will need to be selected, which could increase material cost	Early prototyping and validation of cable technology in 2x2 module and FNAL cryogenic test stand	30%	3	180
Component failures due to assembly cleanliness	IF we observe failures due to particulates at MATF, THEN cleanliness standards and procedures will need to be revised and improved before additional module assembly can occur	Cryo-cycle the module multiple times to mitigate particulates from assembly becoming free within the module structure	30%	2-4-6	

https://edms.cern.ch/document/2741842

131.ND.02.05 Charge Readout: Previous Review Recommendations

Actively working to address recommendations from past reviews. 7 of 16 recommendations closed.

Recommendation	Status	Response
Describe and explain design choices (ADC resolution, DAC resolution, FIFO depth, etc.) in PDR documentation	In progress	Technical notes on ASIC design are uploaded to EDMS
Provide overall guide of documentation within EDMS to reviewers ahead of review	Closed	Provided to PDR review committee 2 weeks prior to review
Review requirements and establish plan for finalizing them	Closed	Technical specifications table updated accordingly with plan for validation
Work with FNAL Neutrino Division for materials test in LAr MTS	In progress	Discussions with FNAL MTS personnel on-going; schedule for materials test not in place
Work with other groups DUNE ASIC teams in ASIC fabrication/packaging and risk mitigation strategies	In progress	Coordinating with FD cold electronics consortium
Study optimal module orientation relative to beam axis	In progress	Simulation tools not yet in place to carry out this study
Evaluate risk of one additional ASIC prototyping iteration	Closed	Given ASIC prototyping cadence and evaluation of M&S/labor profiles, LArPix-v3, -v4, and –v5 prototyping iterations deemed on-shell for mitigating overall ND-LAr cost/scheduling risks
Consider adding means for checking inter-chip synchronization (apart from issuing regular reset commands)	In progress	Inter-chip synchronization evaluation on-going

***Recommendations from May 2021 PDR readiness review (page 1 of 2)**

https://edms.cern.ch/document/2741842

131.ND.02.05 Charge Readout: Previous Review Recommendations

Actively working to address recommendations from past reviews. 7 of 16 recommendations closed.

Recommendation	Status	Response
Consider a specialized review of LArPix-v3 early in the design cycle	In progress	ASIC port to 130 nm technology is current focus; planned review with external engineers/physicists in next months with return to LArPix-v3 design
Investigate pixel geometry optimization with data/simulation	In progress	Simulation and prototyping efforts on-going
Better communicate overall completeness of design and how much work remains to be done	Closed	Addressed in this review
Work with the DAQ group to ensure all the required features of the timing endpoint are exposed in the Bristol firmware IP block; investigate compatibility of the use of Bristol timing for charge readout and White Rabbit timing for light readout	In progress	Timing endpoint integration to PACMAN firmware on-going. Compatibility of Bristol (charge) and White Rabbit (light) timing systems is common to ND-LAr and FD
Coordinate with relevant FNAL safety/electrical compliance committees for timely deployment of 2x2 and as preparation for detector deployment in ND hall	In progress	Coordination with FNAL on-going
Clarify plan for demonstrating that LArPix-v2b addresses issues observed in Module-0	Closed	LArPix-v2b has met all design targets; supporting documentation uploaded to EDMS
Evaluate ASIC QC testing impacts on schedule and consider multiple testing sites	Closed	Performed assessment
Ensure system design and safety procedures are in compliance with FESHM and the FNAL Engineering Manual	Closed	Coordination with FNAL on-going, e.g. ORC review for 2x2 charge readout components

***Recommendations from May 2021 PDR readiness review (page 2 of 2)**

Cost

From Mar. 2022 cost review

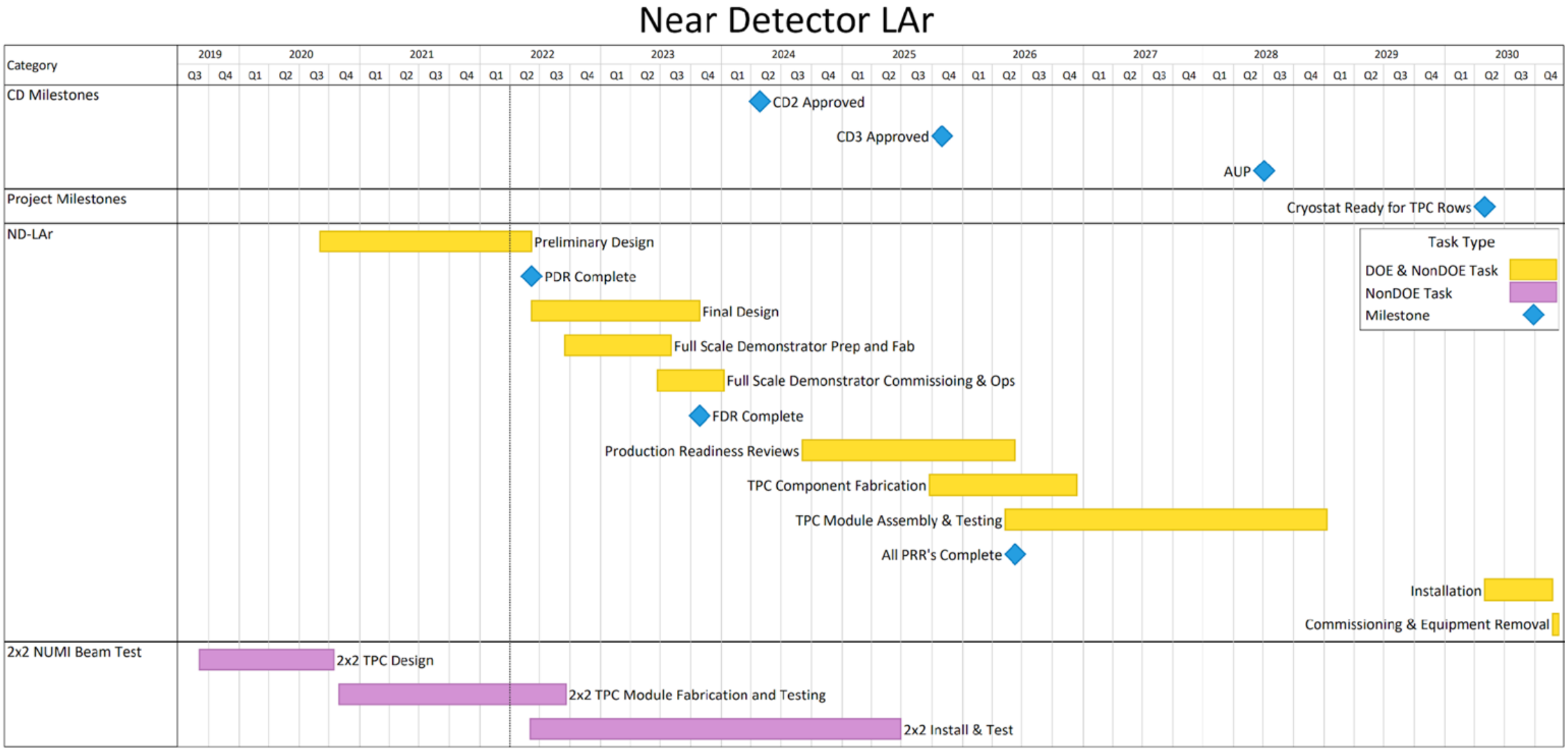
	Design & Prototyping				Production					
	On-Project		Off-Project		On-Project		Off-Project		On-Project	
131.ND.02: ND-LAr	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]	Total Cost [FBAY-k$]	*Avg. Uncert.*
01 ND LArTPC Management	$401.5	18.3	-	43.9	$412.5	13.8	-	72.5	$10,114.9	*10%*
02 Module Structure	-	-	-	14.3	-	-	$2,448.0	22.0	-	-
03 HV	-	-	-	10.5	-	-	$816.0	14.0	-	-
04 Field Structure	$159.1	9.4	-	0.6	$3,560.1	4.9	-	6.5	$7,642.6	*60%*
05 Charge Readout	$1,331.3	17.7	-	16.6	$3,366.0	5.5	-	20.8	$10,741.6	*35%*
06 Light Readout	-	-	-	71.1	-	-	$5,508.0	15.1	-	-
07 Calibration	$193.7	1.3	-	33.1	-	-	-	20.3	$414.0	*50%*
08 TPC Module Assembly and Testing	$368.1	7.1	-	8.6	$103.0	5.7	-	32.0	$1,865.1	*41%*
09 TPC Integration and Installation	$584.2	11.4	-	12.4	$426.0	9.6	-	15.0	$5,384.2	*50%*
10 Module Assembly & Test Facility	-	5.7	-	-	$1,483.0	10.8	-	27.3	$4,114.0	*60%*
11 Full-scale Demonstrator Test Facility	$1,497.5	9.1	-	6.3					$3,726.2	*60%*
12 ArgonCube Test Facility	-	-	$1,250.0	20.9					-	-
13 2x2 NUMI Test Beam Facility	-	-	$2,300.0	15.0				-	-	-
Total:	$4,535.3	79.9	$3,550.0	253.2	$9,350.6	50.5	$8,772.0	245.5	$44,002.5	*43%*

Notes:

1. Extracted EAC from working resource-loaded schedule for internal cost review (P6/Cobra ND-LAr Sandbox, 22 Mar. 2022)
2. Includes all on-project and majority of off-project resource estimates for ND-LAr Consortium.
3. Off-project resources include both international and domestic investments
4. CY-k$: Costs in current-year direct kilo-dollars. FBAY-k$: Costs in fully-burdened at-year (escalated) kilo-dollars.

https://edms.cern.ch/document/2603073

Schedule



Design Path to FDR

ASIC design targets

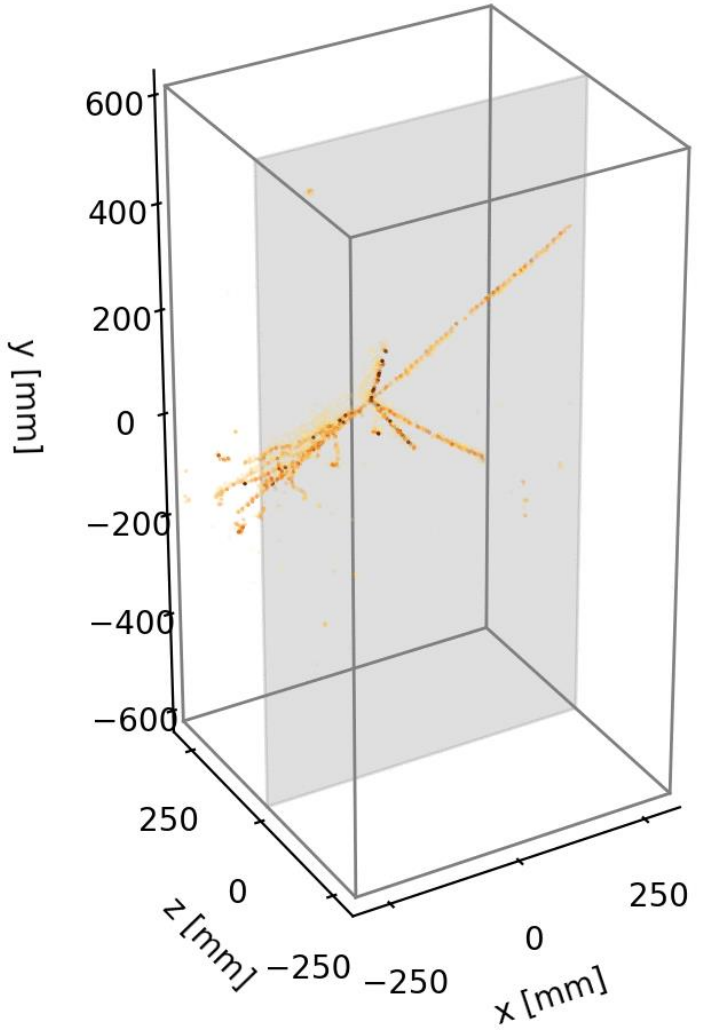
- LArPix-v3: physics performance
- LArPix-v4: quality assurance and reliability/longevity

Verify data/power cables LAr compatibility

Feedthrough FESHM approval

DUNE-SP timing implementation in firmware

Elaboration on technical details in next talk by Armin Karcher



Imaged cosmic-rays from Module-1 prototype data February 2022

Summary

- The ND-LAr charge readout system plays a critical role in delivering DUNE ν oscillation physics
- Validation and maturity of charge readout design exercised through 2x2 program
  - Scope is well-defined with no gaps
  - Intra-system and inter-system interfaces are well-understood
  - System requirements evaluated with prototype data and simulation
  - Exercised parts production, QA, and QC with already constructed/operated Module-0, Module-1
- 2x2 program has critically informed M&S/labor profiles and schedule projection
- **Demonstrated design maturity at the preliminary design level, ready for FSD & final design phase**

https://edms.cern.ch/document/2742778

131.ND.02.05 Charge Readout: Costs

	Design & Prototyping				Production			
	On-Project		Off-Project		On-Project		Off-Project	
131.ND.02.05: Charge Readout	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]	M&S [CY-k$]	Labor [k-hrs]
01 LArPix ASIC	$571.0	6.9	-	4.5	$1,190.3	0.9	-	3.9
02 Cables and Feedthrough	$69.3	1.8	-	0.8	$196.6	0.1	-	0.5
03 Control Interface Electronics	$111.9	2.1	-	3.8	$294.4	0.4	-	0.7
04 Power Supply	$19.0	0.3	-	0.2	$82.8	0.0	-	0.2
05 Clock System	$10.0	0.2	-	0.8	$4.3	0.0	-	0.2
06 Pixel Tile	$525.2	6.2	-	6.0	$1,522.6	2.7	-	4.3
07 Charge Readout Support	$25.0	0.2	-	0.4	$75.0	1.4	-	11.0
Total:	**$1,331.3**	**17.7**	**-**	**16.6**	**$3,366.0**	**5.5**	**-**	**20.8**

Notes:

1. Extracted from current resource-loaded schedule (P6/Cobra ND-LAr Sandbox, 22 Mar. 2022)
2. Includes all on-project and majority of off-project resource estimates for ND-LAr Consortium.
3. Off-project resources include both international and domestic investments
4. CY-k$: Costs in current-year direct kilo-dollars. FBAY-k$: Costs in fully-burdened at-year (escalated) kilo-dollars.