131.ND.02.05 Charge Readout Electronics: Technical Description

Armin Karcher, Charge Readout Lead Electrical Engineer

ND-LAr Preliminary Design Review

27 June 2022

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U.S. DEPARTMENT OF ENERGY | Office of Science

Introduction – Who am I?

- Electrical engineer with strong physics background
- I have been with LBNL for 25 years
- Long history with ASICs and low noise readout
  - BaBar SVT (ATOM ASIC)
  - JDEM ASIC based CCD readout
  - DESI CCD readout and CAN bus controller system

Outline

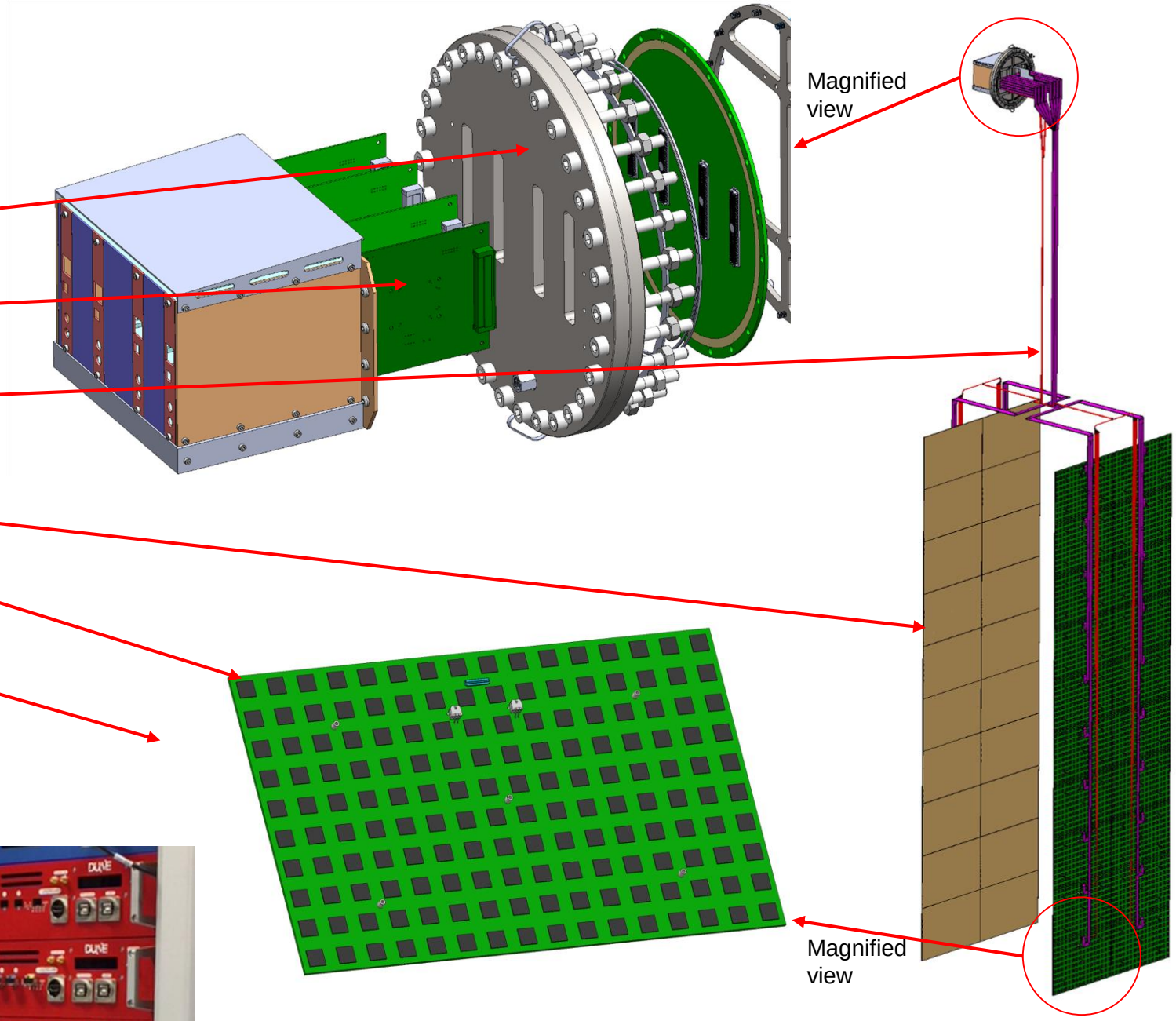
- Documentation Reference
- Charge Readout Components
- Simulation and Analysis
- Overview of Charge Readout Documentation on EDMS
- Code and Standards Compliance
- Open issues – road to FDR
- Summary

Documentation Reference

Charge Readout Documentationc	Description	EDMS Link
Charge Readout Folder	Top level folder for Charge Readout documentation	https://edms.cern.ch/project/CERN-0000217528
Requirements	Spreadsheet with all ND-LAr requirements, see sheet "Charge Readout (05)"	https://edms.cern.ch/document/2589287
Internal ICDs	Interface control documents (ICDs) internal to the ND-LAr Consortium	https://edms.cern.ch/project/CERN-0000223195
Analyses	Collection of analyses write-up: FEAs, bench testing, 2x2 prototype evaluations	https://edms.cern.ch/project/CERN-0000229967
QAQC Plan	Subsystem QAQC plan with focus on high-level QAQC test plans	https://edms.cern.ch/document/2605601
Manufacturing Plan	Subsystem Manufacturing plan with focus on manufacturing methods of key items	https://edms.cern.ch/document/2605602
Procurement Plan	Subsystem Procurement plan with focus on procurement management of key items	https://edms.cern.ch/document/2605603
Previous Review Tracking	Spreadsheet with previous review recommendations, see "Charge Readout"	https://edms.cern.ch/document/2741842
Cost	High-level cost estimate for ND-LAr and subsystems	https://edms.cern.ch/document/2742778
Schedule	High-level "one-pager" schedule for ND-LAr Consortium activities	https://edms.cern.ch/document/2603073
CAD Model (Row Assembly, TPC Assembly)	Solidworks "Pack & Go" and Parasolid exports of CAD models	https://edms.cern.ch/project/CERN-0000230732
Mechanical Component Drawings	Subsystem mechanical component drawings	https://edms.cern.ch/project/CERN-0000218263
Mechanical Assembly Drawings	Subsystem assembly drawing	https://edms.cern.ch/project/CERN-0000220711
Parts List	Subsystem parts list	https://edms.cern.ch/project/CERN-0000220712
Electrical Schematics and Board Layouts	Subsystem electrical schematics and board layouts	https://edms.cern.ch/project/CERN-0000218262
Electrical Cabling and Wiring Specification	Specification of electrical cables/wiring	https://edms.cern.ch/project/CERN-0000218261
Bill of Materials for Electronics Boards	Bill of materials for electroncis boards	https://edms.cern.ch/project/CERN-0000228165

Design Elements – Overview

- Feedthrough
- PACMAN
- Cabling
- Tile PCB
- ASIC
- Timing System
- Power Supply



Design Motivation – charge readout pixelated TPC

- High occupancy environment → Pixelated read out, optically segmented TPC.
- Pixelated read out → very large channel count.
- Self triggering, high channel count ASIC → reduce data volume and interconnect count.
- Highly configurable ASIC with chip-to-chip networking → reduce off-PCB interconnect.
- Ultra low power ASIC is needed for cryogenic power budget.
- One ASIC converts charge input to data packet output → monolithic detector.
- Only one active component in cold electronics → simplifies testing and validation.

- Tile PCB is the detector → back side contains only charge sensing pads, no other conductors.
- Design PCB for production with industry standard processes → direct scalability.

- Digital data from the cold enables simpler warm electronics
  - One warm controller can drive 10 tile PCBs, 1600 ASICs, 102400 pixels

Design Elements – LArPix ASIC

LArPix ASIC: 64-channel CSA with self triggered ADC

Integrates all electronics for TPC readout

Design drivers:

- Ultra low power, ultra low leakage
- High channel count
- Chip-to-chip network

Design Status:

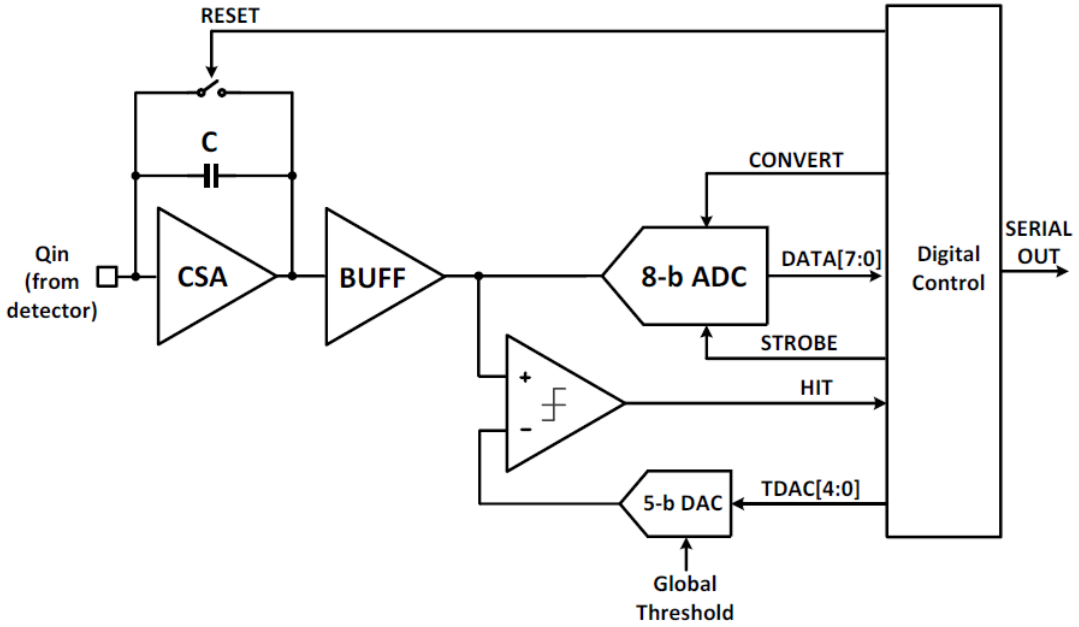
- V2A built and tested
  - CMOS I/O hampers performance
  - minor logic bugs
- V2B Built and initial testing
  - logic bugs fixed

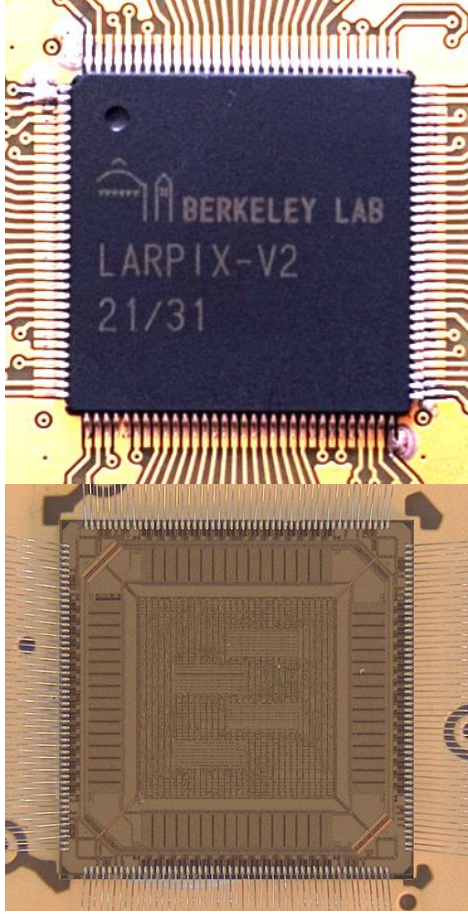
Prototyping:

- Initial module 0 data with V2A ASIC
- V2B will be in module 2&3, V3 in the Full Scale Demonstrator

Challenge:

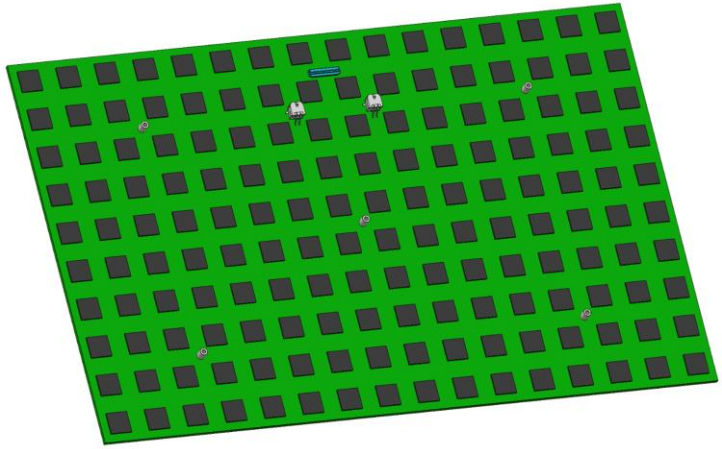
- Reliability testing
- 180nm process unavailable, migrate to 130nm





https://edms.cern.ch/document/2746199/1

Design Elements – Tile PCB

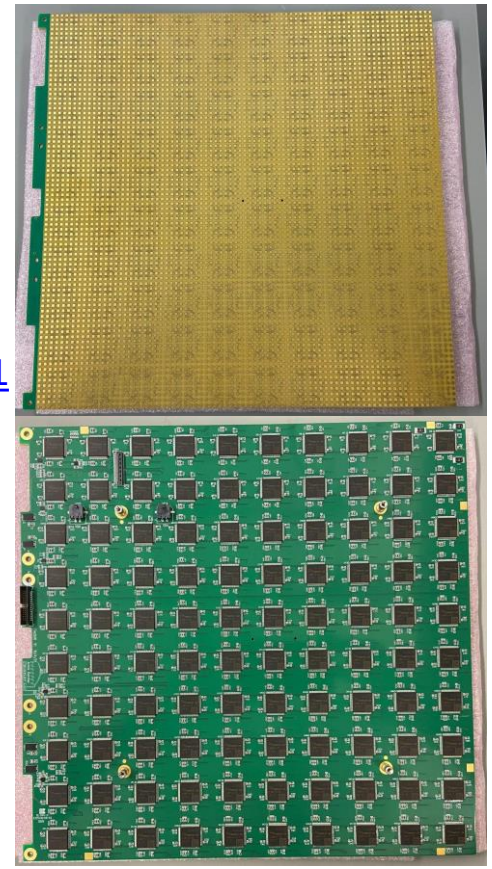


The PCB that is the detector
- Bottom side has only pixel pads
- Top side has all electronics: ASICs, passives, connectors
- 8 layers, buried vias, micro vias

Design drivers:
- Support 160 ASICs, 30x47cm
- Minimize input capacitance, no through vias
- Prevent coupling of digital signals into charge sensitive inputs

Design Status:
- 30x30cm version designed and built
- Schematic and 80% Layout done for full size

https://edms.cern.ch/document/2745017/1



Prototyping:
- Initial testing with V2A ASIC on module 0,1
- Qualification with V2B ASIC is ongoing
  - higher pixel count, ultra low swing differential I/O

Challenge:
- Fabricating unique detector PCBs with scalable commercial PCB technology

Design Elements – Cabling

Power Cable: Twisted pair PTFE insulated 18AWG – low voltage drop

Data Cable: Polyester based shielded FFC – 10MHz differential signals

- extruded cable, ends processed for connector (stiffener, gold plating, exposed shield

Design drivers:

- LAr compatibility
- Power delivery with low voltage drop
- Data signal integrity

https://edms.cern.ch/document/2589305/1

Design Status:

https://edms.cern.ch/document/2589306/1

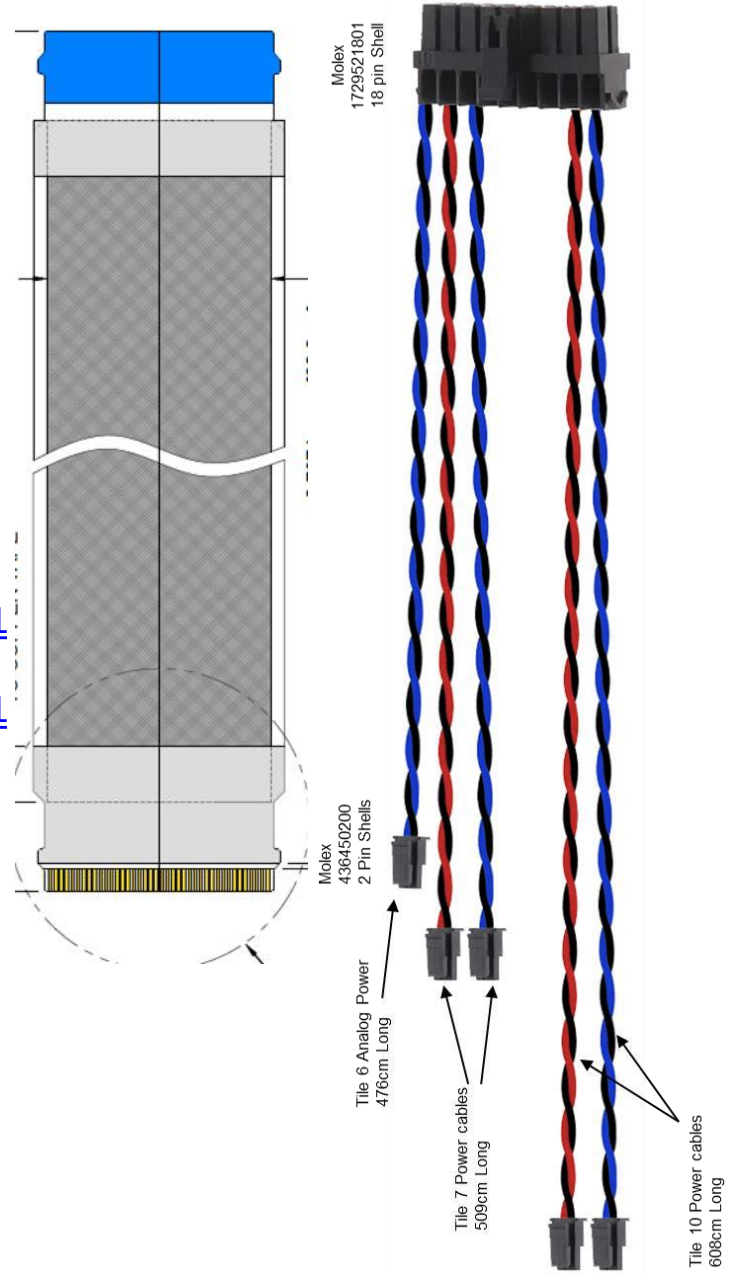
- Drawings exist with vendor quote

Prototyping:

- Data and power cables for 2x2 in hand
- Investigation in other vendors ongoing
- Qualification of cables in LAr not complete

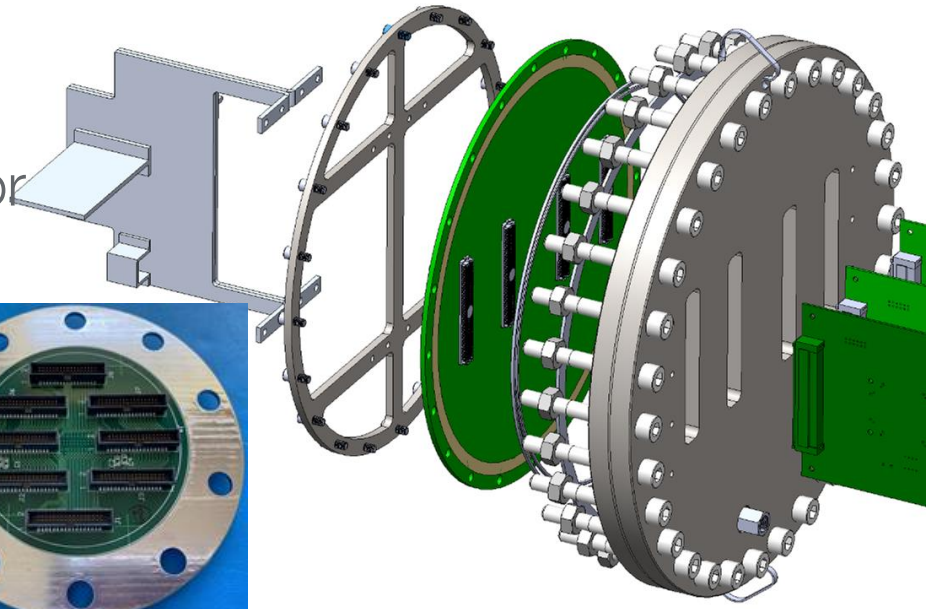
Challenge:

- Selecting a vendor & technology to allow scaling from prototypes to 1400 cables



Design Elements – Feedthrough

RUTGERS
THE STATE UNIVERSITY OF NEW JERSEY



6-layer filled-via PCB assembly and mechanical support for electrical feed-through into argon

Design drivers:

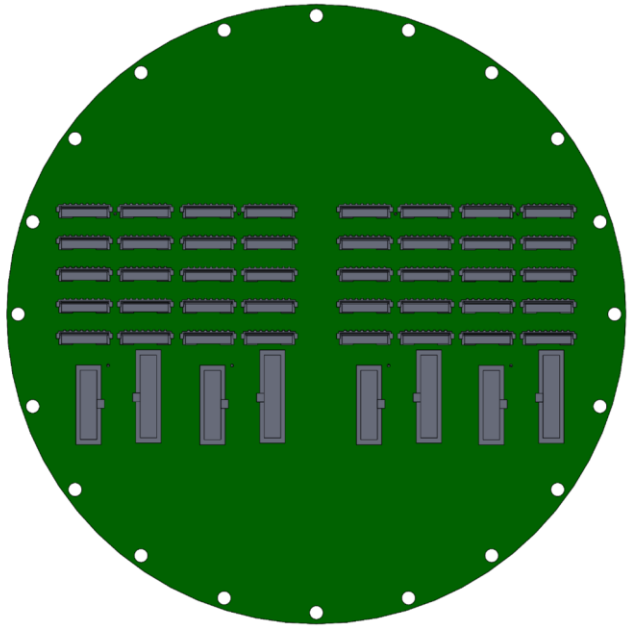
- Hermeticity
- Pressure safety (4x MAWP of 350 mbarg)
- Power (<1A) and data (<10MHz) fan-out

Design Status:

- PCB layout exists with vendor quote https://edms.cern.ch/document/2745382/1
- Hardware drawings exist with vendor quote
- Pressure analysis completed (https://edms.cern.ch/document/2737730/1)

Prototyping:

- Module 0,1 have been tested.
  - Much smaller PCB
  - Required epoxy sealing of alignment pins
- Module 2,3 not yet tested
  - Did implement partial drill for fully hermetic PCB as delivered



Design Elements – PACMAN

UC DAVIS
UNIVERSITY OF CALIFORNIA

Based on a commercial XILINX SOC module running linux

Direct link to the DAQ system via ethernet

Isolated power & data inputs, passive and active power filters

Design drivers:

- Power 10 tiles, 1600 ASICs
- Implement 40 custom UARTs
- DAQ and timing system interface

Design Status:

https://edms.cern.ch/document/2745018/1

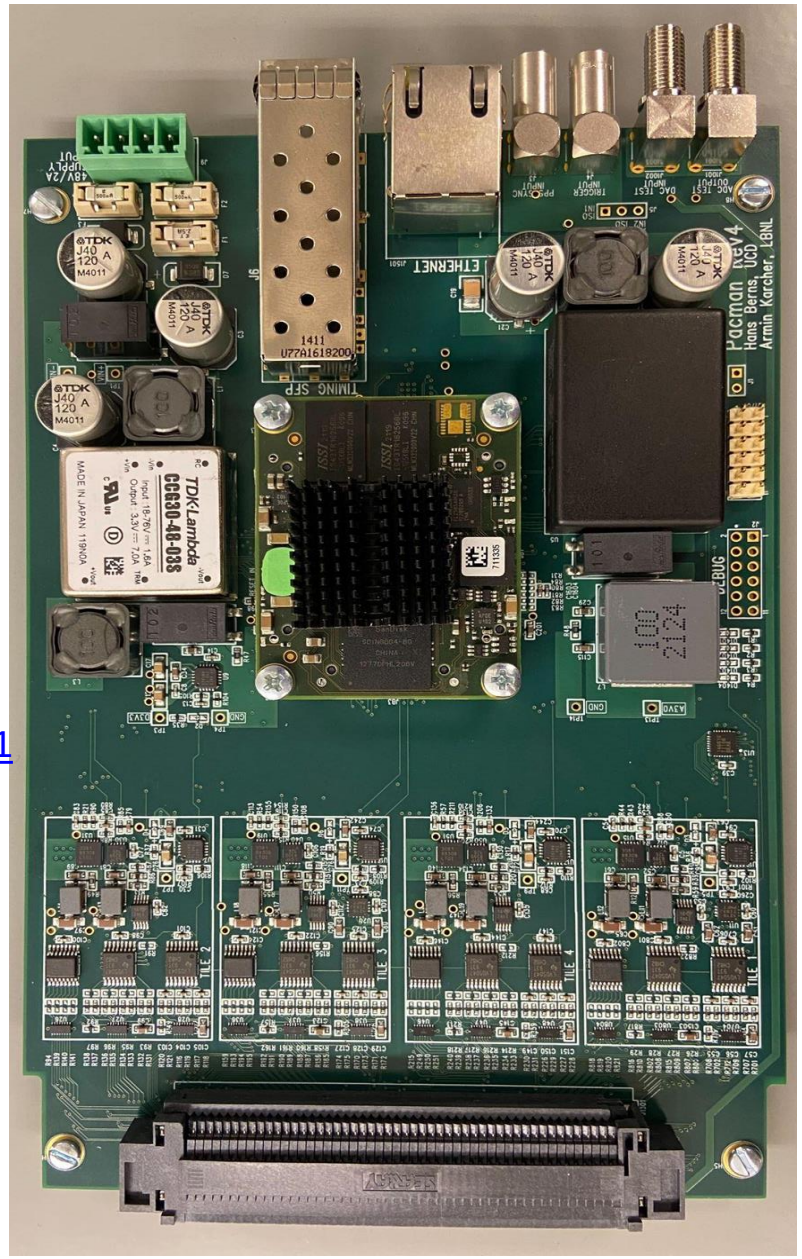
- 8 tile version designed and built
  - Power system designed for 10 tiles
  - Pinouts assigned for 10 tiles

Prototyping:

- Operational on module 0 and 1 for 2x2
- Timing endpoint firmware and testing ongoing

Challenge:

- Component unavailability and lead times over 52 weeks make prototyping challenging



LBNF/DUNE

Design Elements – Timing, PSU

Commercial off-the-shelf power supply

DUNE-SP timing system, designed in Bristol for DUNE FD

Design drivers:

- Synchronize all ASICs
- Provide unique timestamps
- Power the PACMAN

Design Status:

- UCI is implementing the PDTS endpoint in PACMAN firmware
- For the power supply we chose the Wiener PL506

Prototyping:

- Timing system has been tested in Proto DUNE
  - Implementation in PACMAN complete, testing just beginning

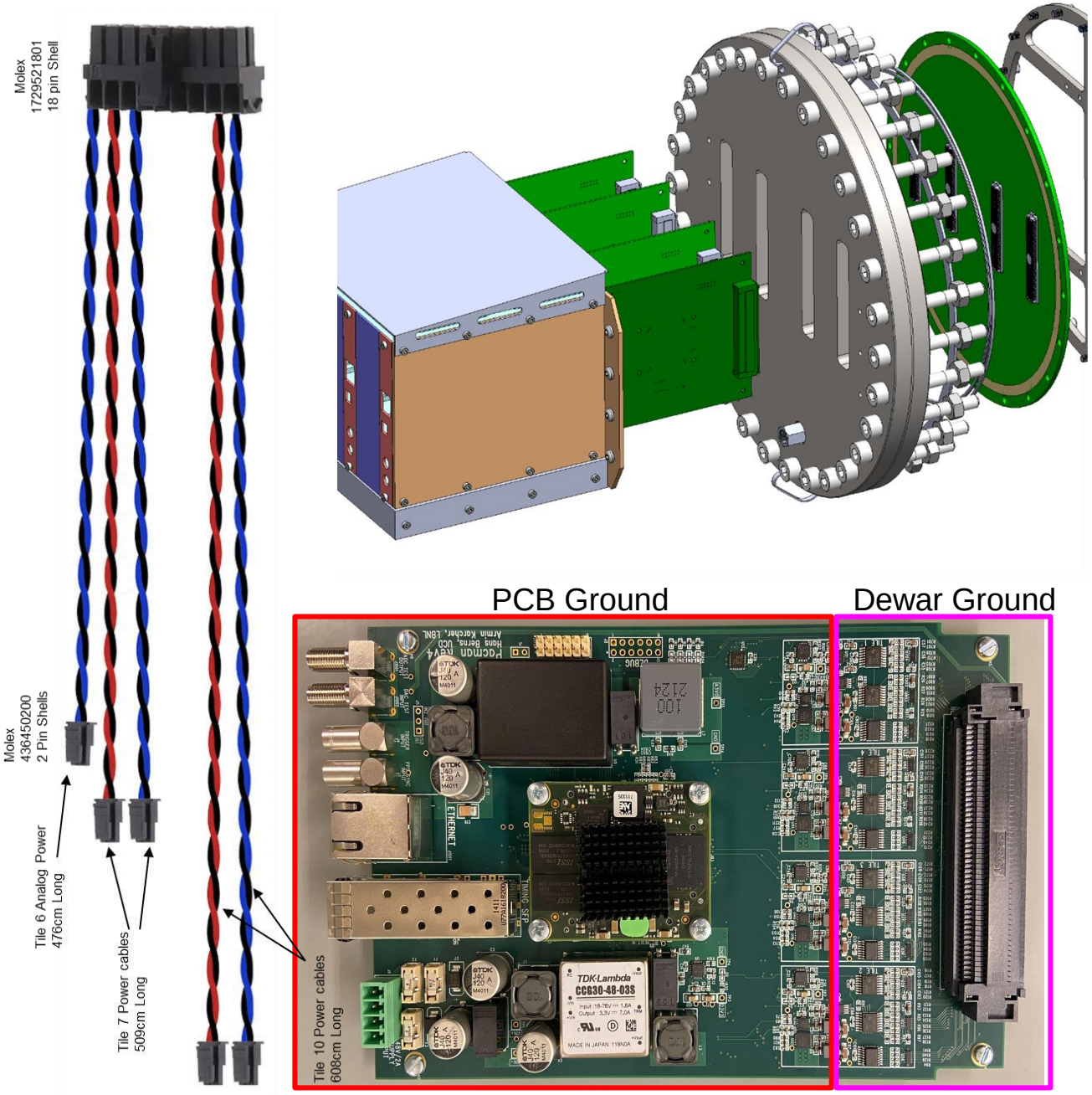
Challenge:

- Timing system testbed and simulation environment is complex
  - System bring-up more involved than expected

Grounding

https://edms.cern.ch/document/2459152/1

- Feedthrough acts as backplane
  - Low impedance to dewar ground
- PACMAN implements filters
- 18AWG cable, <1A current
  - Low voltage drop
- All electronics on flange
  - Data on fibers
  - Power supply is floating, return not ground referenced at PSU



3D Imaging Requirements

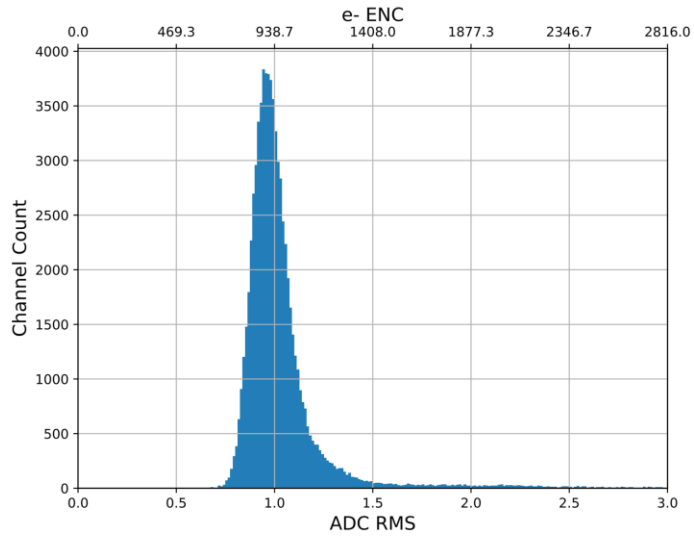
ID	Requirement	Value	Parent ID	Parent Requirement	Notes
CRO-001	Pixel charge readout		SYS-003	Pileup rejection efficiency	Unambiguous 2D pixelated charge readout anodes for accurate 3D charge imaging
CRO-002	Pixel spacing	< 4.7 mm	SYS-004	3D charge imaging accuracy	Spatial resolution comparable to or better than the far detector
CRO-003	Pixel time resolution	< 3 us	SYS-004	3D charge imaging accuracy	Provide equivalent spatial resolution in the drift direction as the transverse directions
CRO-004	Pixel noise	1 ke^-	SYS-004	3D charge imaging accuracy	Noise uncertainty comparable to or better than the far detector
CRO-005	Pixel saturation level	>180 ke^-	SYS-004	3D charge imaging accuracy	Charge dynamic range comparable to or better than the far detector
CRO-006	Pixel charge resolution	<5% MIP signal	CRO-004	Pixel noise	Electronics noise contribution to charge resolution should be smaller than the intrinsic fluctuations for MIP signals
CRO-007	Pixel linearity (post-calibration)	<2%	CRO-004	Pixel noise	Pixel charge measurement linearity after channel calibration should not exceed the charge resolution specification
CRO-008	Pixel efficiency	>95%	SYS-004	3D charge imaging accuracy	Self-trigger efficiency for ¼ MIP charge (irrespective of track topology)
CRO-018	Pixel data loss fraction	<0.1%	SYS-004	3D charge imaging accuracy	Tolerable data loss fraction for negligible physics performance degradation
CRO-034	Pixel tile leakage current	< 1 ke^-	CRO-004 CRO-006	Pixel noise Pixel charge resolution	Maximum integrated leakage current between front-end reset

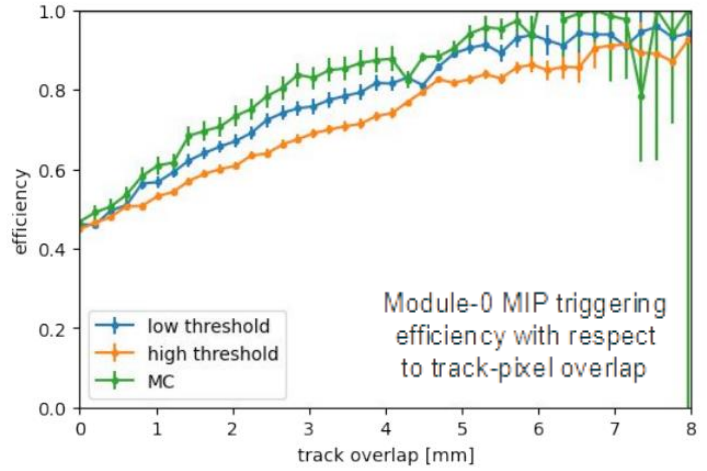
3D imaging validation

https://edms.cern.ch/document/2748462/1

- Pixel spacing: 4.4 mm (Module-0, -1), 3.8 mm (Module-2, -3)
- Pixel time resolution: 2.7 us
  - Tunable signal integration dominates timing resolution
  - Threshold crossing timing resolution: 30 ns
- Pixel noise: 920 e- (LArPix-v2a Module-0), 850 e- (LArPix-v2b CTS)
- Pixel saturation level: >200 ke-
  - Module-0 cosmic data: no ADC saturation observed
- Pixel charge resolution: <1200e-
  - MIP charge per pixel ~27ke- → 5% MIP ~1350e-
- Pixel linearity: < 1.2% pre-calibration
- Pixel efficiency: ~80% for MIP (Module-0); to be assessed for Module-1 data
  - 5.8 ke- charge threshold, 7.8% inactive channels (Module-0)
  - 4.5 ke- charge threshold, 2.4% inactive channels (Module-1)
- Pixel data loss fraction: <0.005% (Module-0)
- Pixel tile leakage current: ~100aA (LArPix-v1)
  - Assessment in progress (N. Rowe, UC Berkeley)

LArPix meets all performance requirements except track efficiency

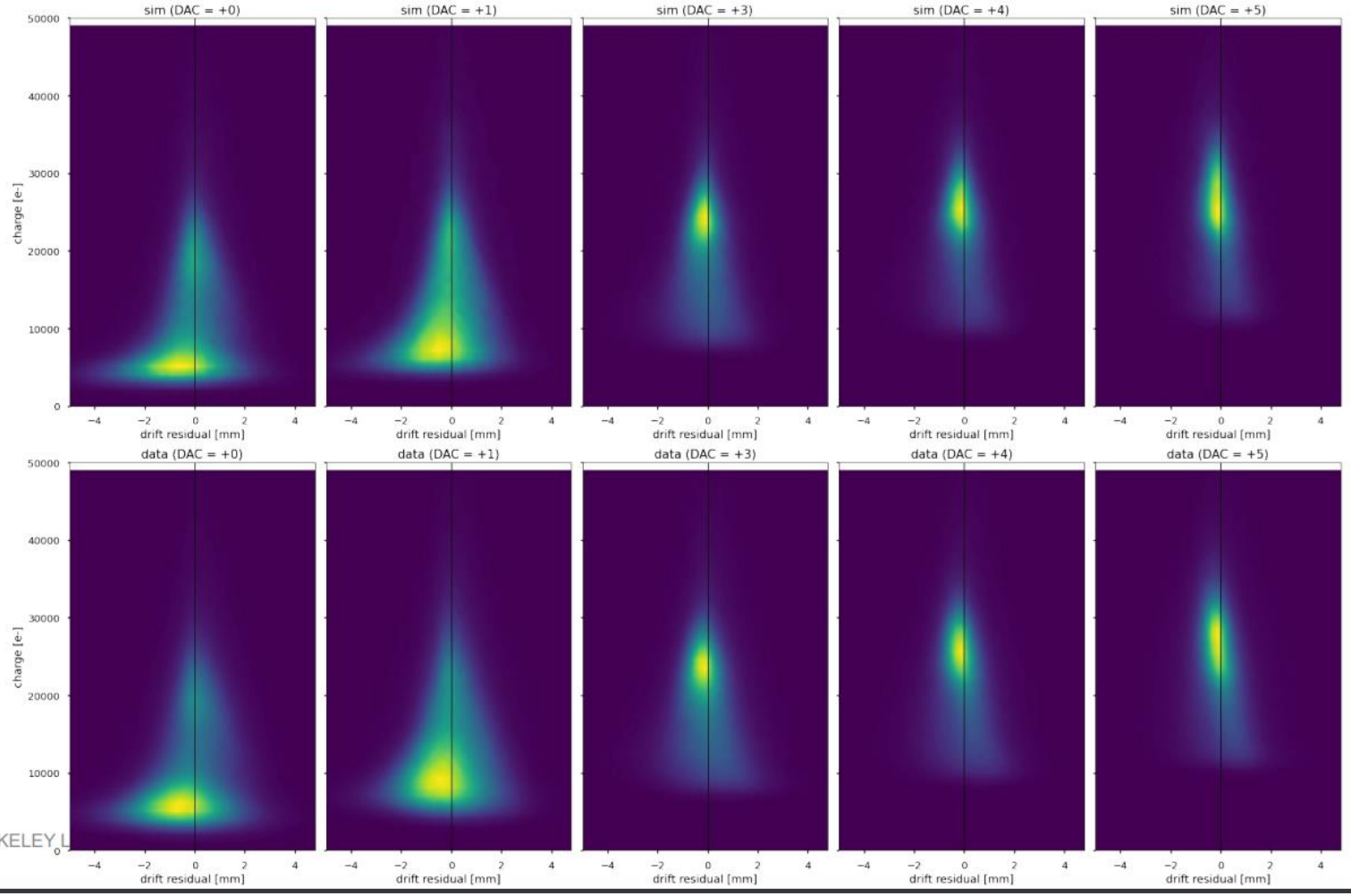




Studies

Understanding LArPix response

https://edms.cern.ch/document/2745338/1



Simulation

Data

P. Madigan, UCB

Active Volume Requirements

ID	Requirement	Value	Parent ID	Parent Requirement	Notes
CRO-009	Instrumented anode area	>99%	SYS-007	Interior Fiducial Volume Fraction	Mitigate inactive volume
CRO-011	Bad pixel fraction	<5%	CRO-009	Instrumented anode area	Fraction of channels outside of performance specifications
CRO-012	Bad ASIC fraction	<3%	CRO-009	Instrumented anode area	Fraction of ASICs outside of performance specifications
CRO-013	Dead pixel tile fraction	<0.1%	CRO-009 SYS-004	Instrumented anode area 3D charge imaging accuracy	Fraction of pixel tiles outside of performance specifications
CRO-014	Pixel failure rate	<0.5% per year	CRO-009	Instrumented anode area	Meet CRO-011 after 10 years detector operation
CRO-015	ASIC failure rate	<0.3% per year	CRO-009	Instrumented anode area	Meet CRO-012 after 10 years detector operation
CRO-016	Pixel tile failure rate	<0.01% per year	CRO-009	Instrumented anode area	Meet CRO-013 after 10 years detector operation
CRO-017	Pixel tile I/O channel redundancy	>2	CRO-013	Dead pixel tile fraction	Sufficient I/O redundancy such that loss of ASICs does not result in loss of I/O to entire tile
CRO-025	Gaps between tiles	TBD	SYS-007	Interior Fiducial Volume Fraction	Mitigate inactive volume

Covered by QC/QA https://edms.cern.ch/document/2605601/1

Yield Requirements

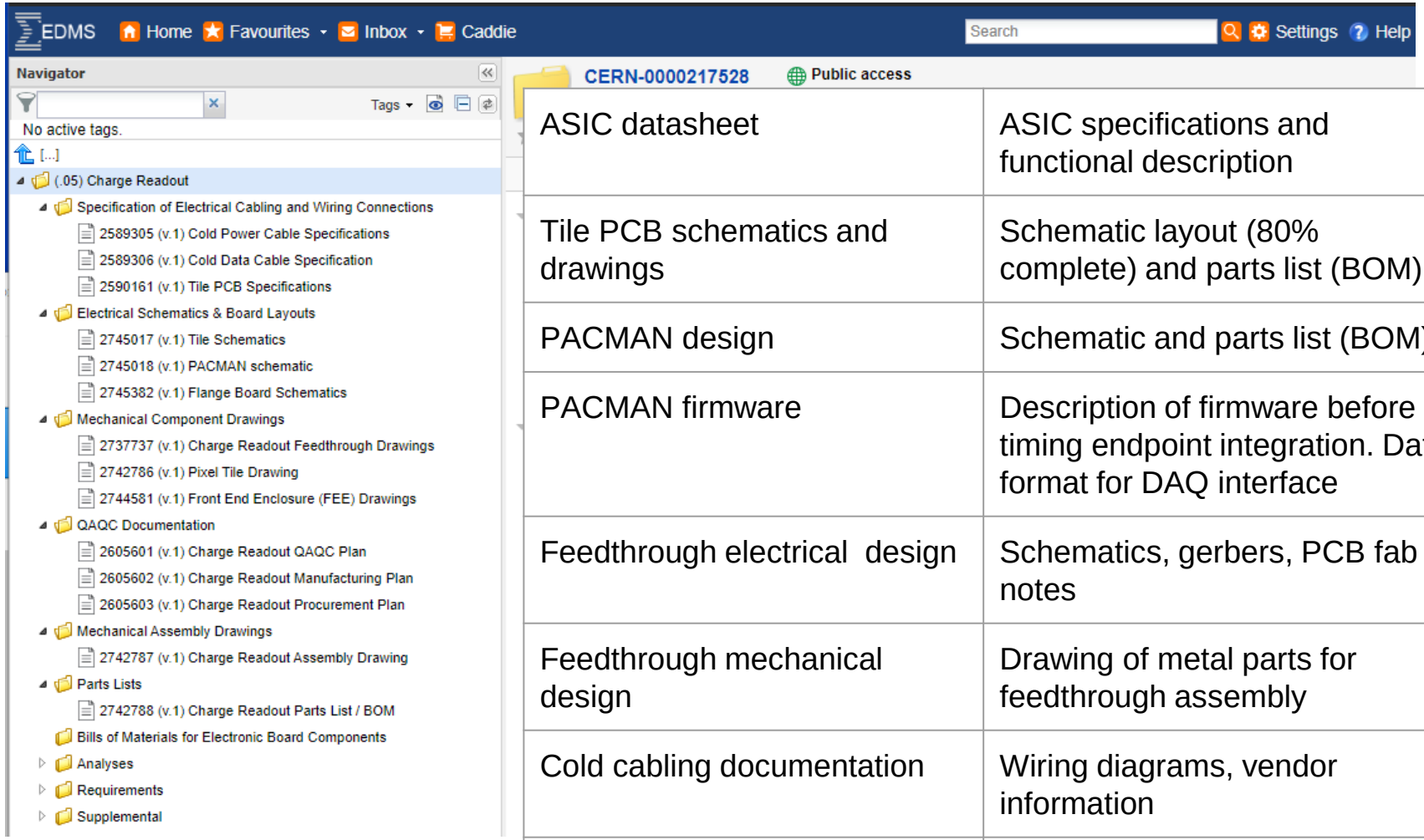
ID	Requirement	Value	Parent ID	Parent Requirement	Notes
CRO-027	ASIC yield (room temperature)	>70%	CRO-002 SYS-007	Pixel spacing Interior Fiducial Volume Fraction	Fraction of ASICs passing room temperature QC and integration testing
CRO-028	ASIC yield (cryogenic temperature)	>99.5%	CRO-002 SYS-007	Pixel spacing Interior Fiducial Volume Fraction	Fraction of ASICs passing cryogenic QC and integration testing
CRO-026	Pixel tile yield	>80%	SYS-007	Interior Fiducial Volume Fraction	Fraction of pixel tiles passing cryogenic QC and integration testing
CRO-024	Pixel tile thermal cycling	3	CRO-013	Dead pixel tile fraction	Multi-thermal cycled tile testing to mitigate detector infant mortality

Power Requirements

ID	Requirement	Value	Parent ID	Parent Requirement	Notes
CRO-010	Pixel multiplexing	1000	SYS-025	Thermal load	Driven by head conduction from feedthrough, ullage impurities, feedthrough spacing constraints
CRO-019	Heat dissipation	<3.9 kW	SYS-025	Thermal load	
CRO-020	Heat density	<20 mW/ASIC	SYS-025	Thermal load	Shall not induce LAr boiling in the detector
CRO-022	Total power	<20 kW	SYS-025	Thermal load	Defined by capabilities of site infrastructure

Documentation Tour

https://edms.cern.ch/project/CERN-0000217528



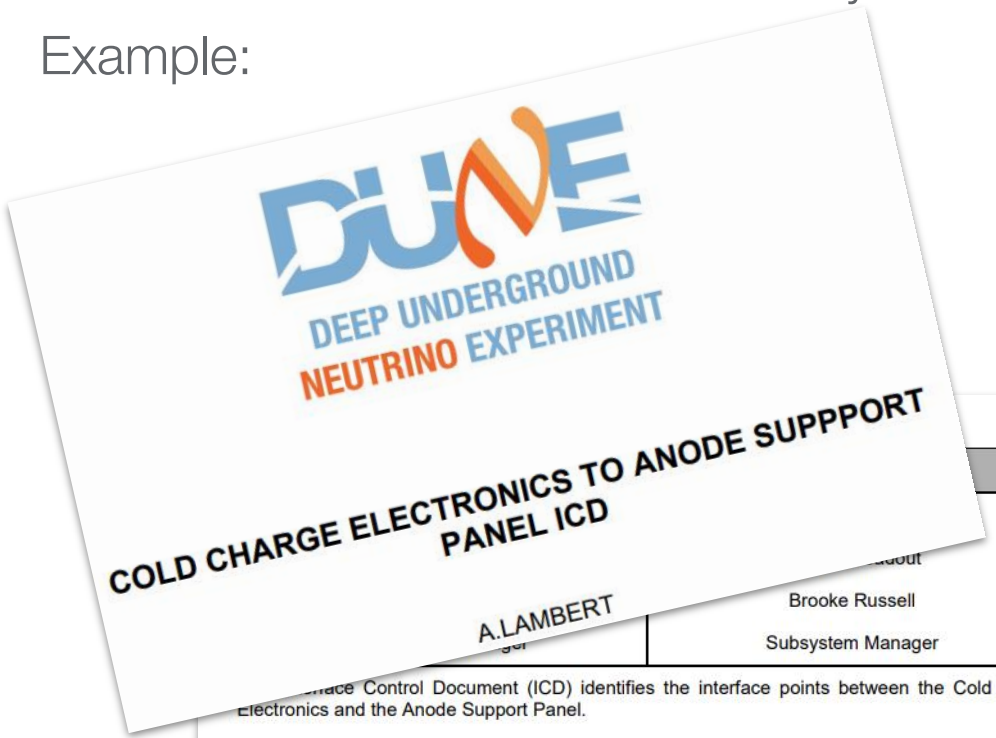
ASIC datasheet	ASIC specifications and functional description	https://edms.cern.ch/document/2746199/1
Tile PCB schematics and drawings	Schematic layout (80% complete) and parts list (BOM)	https://edms.cern.ch/document/2745017/1
PACMAN design	Schematic and parts list (BOM)	https://edms.cern.ch/document/2745018/1
PACMAN firmware	Description of firmware before timing endpoint integration. Data format for DAQ interface	https://edms.cern.ch/document/2745789/1
Feedthrough electrical design	Schematics, gerbers, PCB fab notes	https://edms.cern.ch/document/2745382/1
Feedthrough mechanical design	Drawing of metal parts for feedthrough assembly	https://edms.cern.ch/document/2737737/1
Cold cabling documentation	Wiring diagrams, vendor information	https://edms.cern.ch/project/CERN-0000218261
Charge - Light readout interface		https://edms.cern.ch/document/2667843/1

Interfaces

https://edms.cern.ch/project/CERN-0000231363

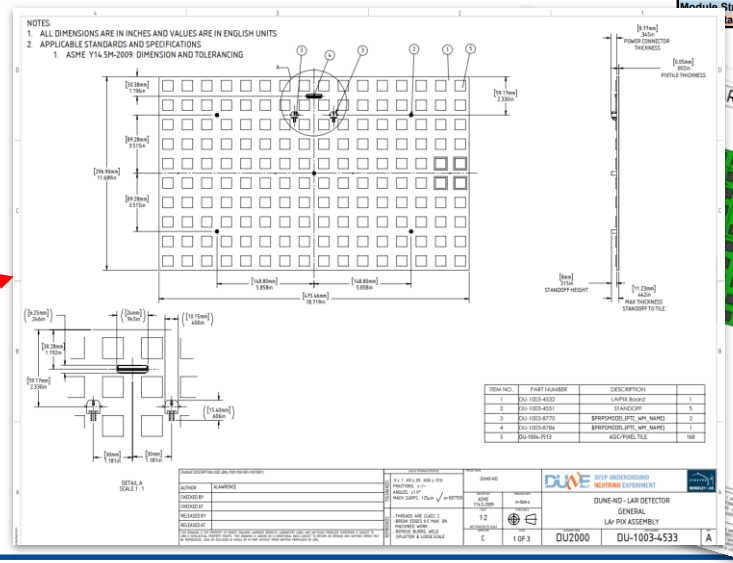
Interfaces can be found in the subsystem interfaces folder or N² matrix

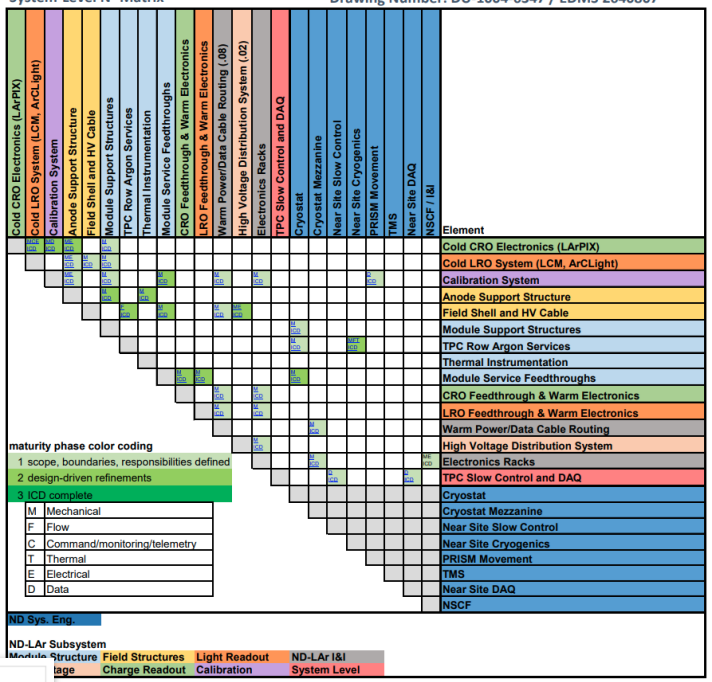
Example:

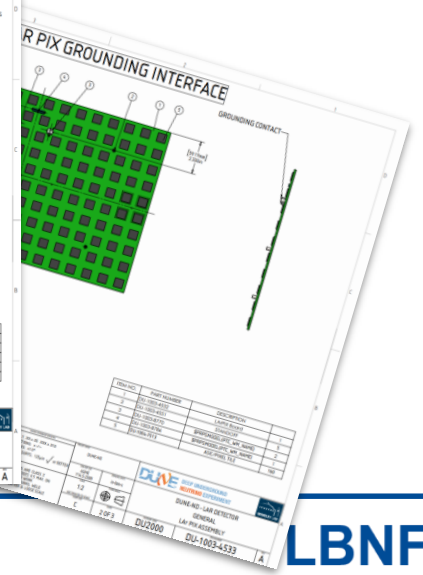


Control Document (ICD) identifies the interface points between the Cold Charge Electronics and the Anode Support Panel.

Item	WBS 131.02.ND.04 Provides	WBS 131.02.ND.05 Provides	Interface Point
Mechanical Mounting	Clearance hole pattern on Anode Panel	Mounting hardware	EDMS 2688547
Charge Readout Cable Route	Field structures routes cables based on LBNL provided interface spec sheet	Diagram/schematics with bend radii, cable counts, cable cross section, cable type ID, connector type, connector size, proposed cable route	EDMS 2688547
		Routing/Strain relief	







ESH Codes and Standards

- All commercial electrical equipment needs NRTL approval (UL, ETL etc)
  - Computers and networking equipment
  - Power supplies
  - If no NRTL listed equivalent exists, needs to be approved by FNAL
- All power cabling shall meet specifications in FNAL engineering handbook:
  - See Table 2, Page 6 https://esh-docdb.fnal.gov/cgi-bin/sso/RetrieveFile?docid=2781)
- All custom PCBs need to meet specifications in the FNAL engineering handbook and pass ORC approval. (see especially pages 3 and 5)
  - See example document for PACMAN on 2x2: https://edms.cern.ch/document/2745371/1
  - Focus of ORC is fire prevention
- Charge readout uses low voltage <36V, low power supplies <600W.
  - No additional hazards.

Open Design Issues / Path to FSD & FDR

Current preliminary design status:

- LArPix ASIC works well. Version v2b resolves all v2a issues.
- Tile PCB design decouples digital IO from charge sensitive input.
- Readout Controller (PACMAN) meets requirements needed thus far.
- We can use commercial mass manufacturing to produce the pixelated TPC at ~$0.10/channel at large scale.

Open Design tasks:

- LArPix ASIC migration to 130nm.
- LArPix ASIC LSB reduction. ⇨ Tracking efficiency
- LArPix ASIC noise reduction.
- LArPix ASIC cryogenic reliability testing.
- LArPix ASIC ESD tolerance.
- Tile PCB scaling to full DUNE size. (x 1.6 area)
- PACMAN scaling and optimization.
- Full size feedthrough production.
- Incorporation of timing endpoint testing.

Summary

Status

- LArPix meets all performance requirements except track efficiency
  - 80% feature complete
- 10x10 tile PCB valitates PCB design choices
  - Tile PCB design and procurement process 75% complete
- PACMAN performance is adequate for tile read-out
  - Hardware >80% complete, Firmware 60% complete
- Cabling and Feed-through design is mature
  - Feed through 90% complete, Cabling selection and validation 60% complete

Final Design Phase

- Evolve LArPix design to full performance targets
- Test LArPix reliability
- Finalize Tile and PACMAN design
- Verify system level performance (FSD)
- Verify cabling performance in LAr

Summary

The Charge Readout system design maturity meets PDR requirements.

Moving forward towards FDR we will refine the design and interfaces.
Focus on procedure formalization to ensure repeatability and scalability.
No undefined design choices or scope gaps exist.