131.ND.02.06 Light Readout: Technical Description

Alexander Selyunin, Light Readout Subsystem technical coordinator

ND-LAr Preliminary Design Review

27 June 2022

Who am I

Alexander Selyunin

- Scientific Researcher, I have been working at Joint Institute for Nuclear Research for 12 years
- SiPM R&D, Background in EM-calorimetry (COMPASS-II, CERN), 20-inches PMT scanning and testing for JUNO (China).
- Researcher in the Sector of Experimental Methods, Experimental Department of Particle Physics, Dzhelepov Laboratory of Nuclear Problems, Joint Institute for Nuclear Research

Outline

- Key Documents (table)
- Design elements & status / CAD model
- Key Analyses / Performance Assessment
- Documentation Tour
- EH&S / Codes & Standards
- Open design issues / Final Design plan
- Summary

Key Documents

Light Readout Documentation	Description	EDMS Link
Light Readout Folder	Top level folder for Light Readout documentation	https://edms.cern.ch/project/CERN-0000217529
Requirements	Spreadsheet with all ND-LAr requirements, see sheet "Light Readout (06)"	https://edms.cern.ch/document/2589287
Internal ICDs	Interface control documents (ICDs) internal to the ND-LAr Consortium	https://edms.cern.ch/project/CERN-0000223195
Analyses	Collection of analyses write-up: FEAs, bench testing, 2x2 prototype evaluations	https://edms.cern.ch/project/CERN-0000231222
QAQC Plan	Subsystem QAQC plan with focus on high-level QAQC test plans	https://edms.cern.ch/document/2587876
Manufacturing Plan	Subsystem Manufacturing plan with focus on manufacturing methods of key items	https://edms.cern.ch/document/2605604
Procurement Plan	Subsystem Procurement plan with focus on procurement management of key items	https://edms.cern.ch/document/2605605
Previous Review Tracking	Spreadsheet with previous review recommendations, see "Light Readout"	https://edms.cern.ch/document/2741842
Cost	High-level cost estimate for ND-LAr and subsystems	https://edms.cern.ch/document/2742778
Schedule	High-level "one-pager" schedule for ND-LAr Consortium activities	https://edms.cern.ch/document/2603073
CAD Model (Row Assembly, TPC Assembly)	Solidworks "Pack & Go" and Parasolid exports of CAD models	https://edms.cern.ch/project/CERN-0000230732
Mechanical Component Drawings	Subsystem mechanical component drawings	https://edms.cern.ch/project/CERN-0000218197
Mechanical Assembly Drawings	Subsystem assembly drawing	https://edms.cern.ch/project/CERN-0000218198
Parts List	Subsystem parts list	https://edms.cern.ch/project/CERN-0000220723
Electrical Schematics and Board Layouts	Subsystem electrical schematics and board layouts	https://edms.cern.ch/project/CERN-0000218199
Electrical Cabling and Wiring Specification	Specification of electrical cables/wiring	https://edms.cern.ch/project/CERN-0000217668
Bill of Materials for Electronics Boards	Bill of materials for electronics boards	https://edms.cern.ch/project/CERN-0000231223

Design Elements - Light Detectors

Two complimentary light trap detectors: ArCLight & LCM.
Mechanically interchangeable. Same readout for both.

High maturity - long detectors is in production

Design drivers:

- Dielectric materials **OK**
- Large surface covering **OK**
- Relatively high PDE **OK**

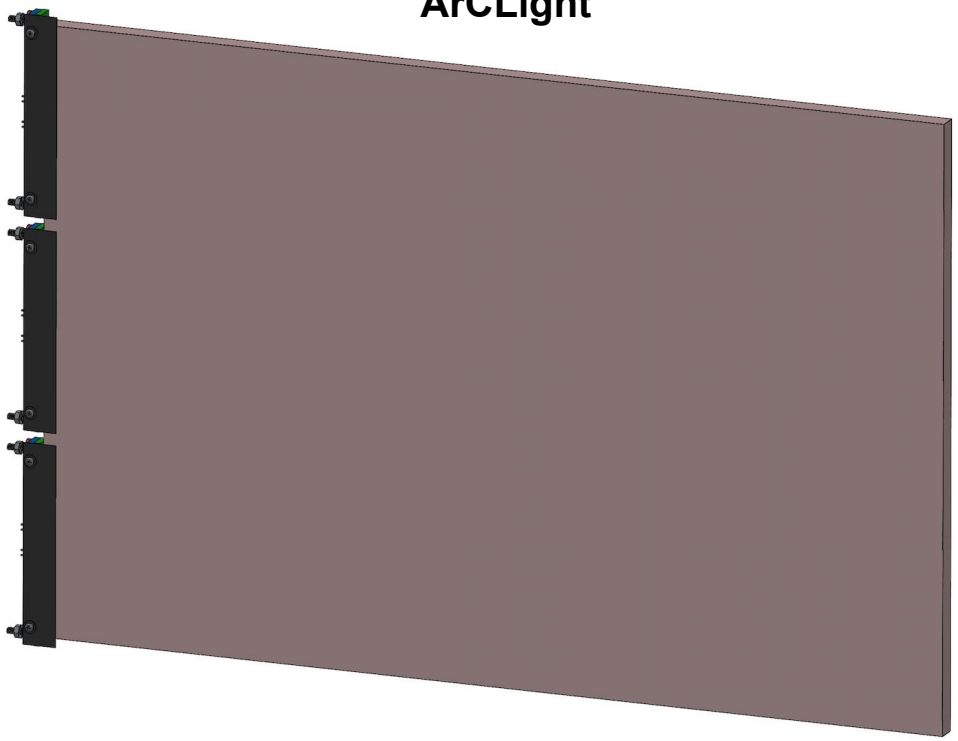
Design status:

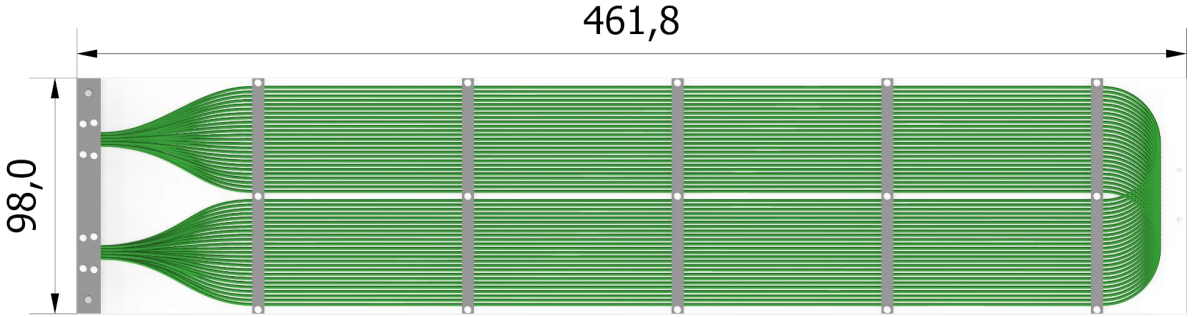
- 30 cm long versions designed & built
- Full size prototypes under production

Prototyping:

- Initial performance on module 0,1
- ArCLight modification for Module 1->higher PDE

ArCLight





LCM

https://edms.cern.ch/project/CERN-0000230732

Design Elements - Front-End Electronics

PCBs with amplifiers, cold & warm operation.

Cold PCB holds SiPMs, additional shielding implemented

VGA - VME-bus powered 6U PCB. **80% maturity achieved**

Design drivers:

- Signal transmission to long lines **OK**
- Low heat dissipation in LAr ~ 50mW per ch **OK**
- Signal adjustment for calibration & physics run **OK**
- Low noise pick-up **OK**

Design status: **OK**

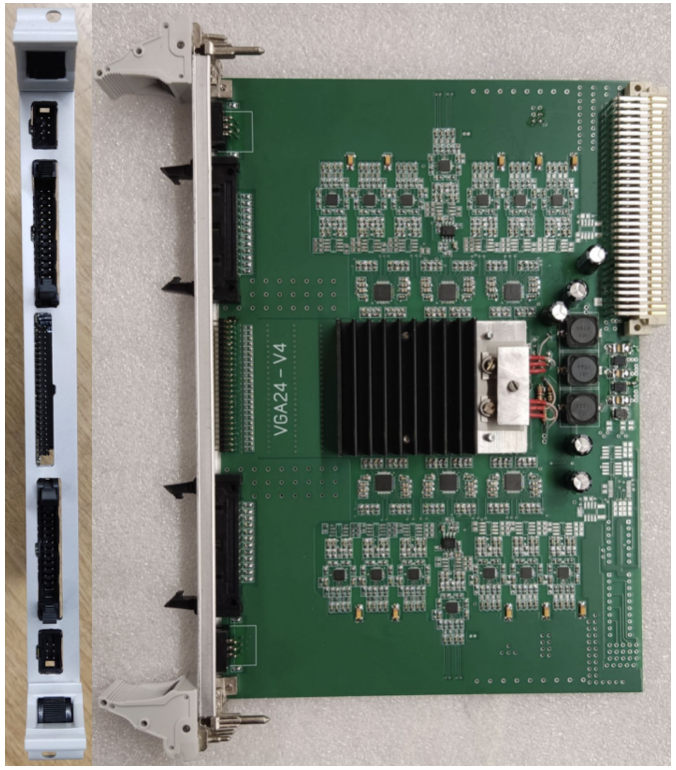
- 2x2 versions designed & built
- Schematics and layouts are 70% done for ND

Prototyping:

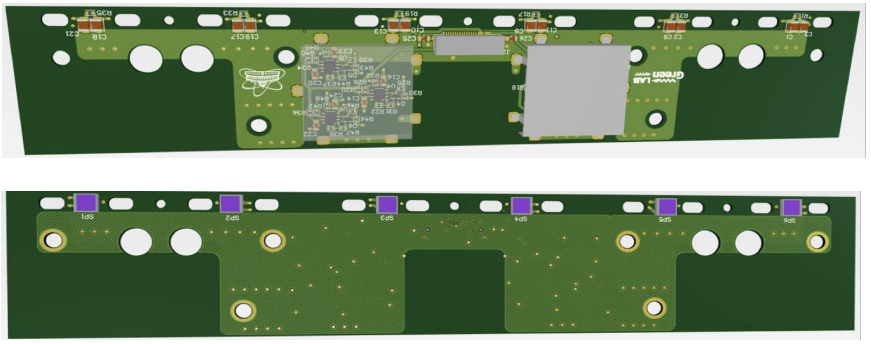
- Operational on module 0,1 for 2x2

https://edms.cern.ch/project/CERN-0000218199

60-ch Variable Gain Amplifier (VGA)



Cold PCB with built-in preamps & SiPMs



Design Elements - SiPM biasing, CAN-VME controller

VME-bus powered 6U PCBs.

128ch HV DAC-based PCB for SiPM biasing - **DONE, 100% maturity**

Built-in System on Modules chip provides CAN-VME interface - **80% maturity achieved**

Design drivers:

- Individual SiPM biasing up to 60V **OK**
- Multi channel board **OK**
- Remote control via reliable interface **OK**

Design status:

- SiPM biasing designed & built
- 2x2 version of CAN-VME controller designed & built
- Schematics and layouts are 90% done for ND

Prototyping:

- Initial testing on module 1 for 2x2
- Qualification is ongoing

SiPM biasing PCB and CAN-VME controller

https://edms.cern.ch/project/CERN-0000218199

Design Elements - Cabling

Cold Data/Power cables: Microcoaxial cables 38AWG or flex PCB

Warm Data cables: twisted pair flat cable 28AWG, 30AWG flat cable, optical fiber. **Off-the-shell cables-> High maturity.**

Design drivers:

- LAr compatibility **OK** - tests in LAr for Mod 0,1
- Noise protection **OK**
- Low voltage drop for power **OK**

Design status:

- Off-the-shell cables with specs by Samtec/3M

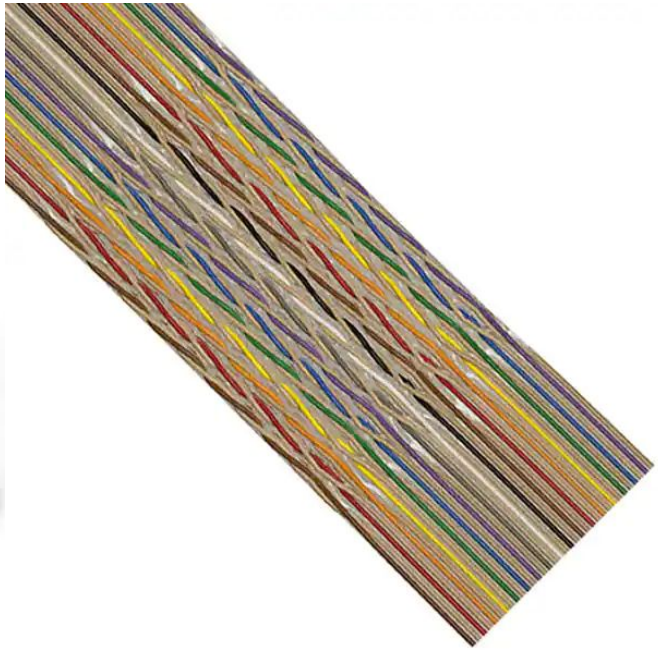
Prototyping:

- Power and data cables in hand for 2x2
- Flex PCB usage study is ongoing
- Cables qualification in LAr not complete

Challenge:

- Long cables for ND
- Mass production to ND

https://edms.cern.ch/project/CERN-0000217668



Design Elements - DAQ, timing

White Rabbit switch for time sync - **off-the-shell unit -> 100% mature**

VME AFI ADC, GPS timestamp 8ns (<100ps jitter) - **100% mature**

Design drivers:

- DAQ and timing system interface, precise timestamp **OK**
- Digitization of the whole beam spill (~30us) **OK**
- Flexible DAQ configuration **OK**

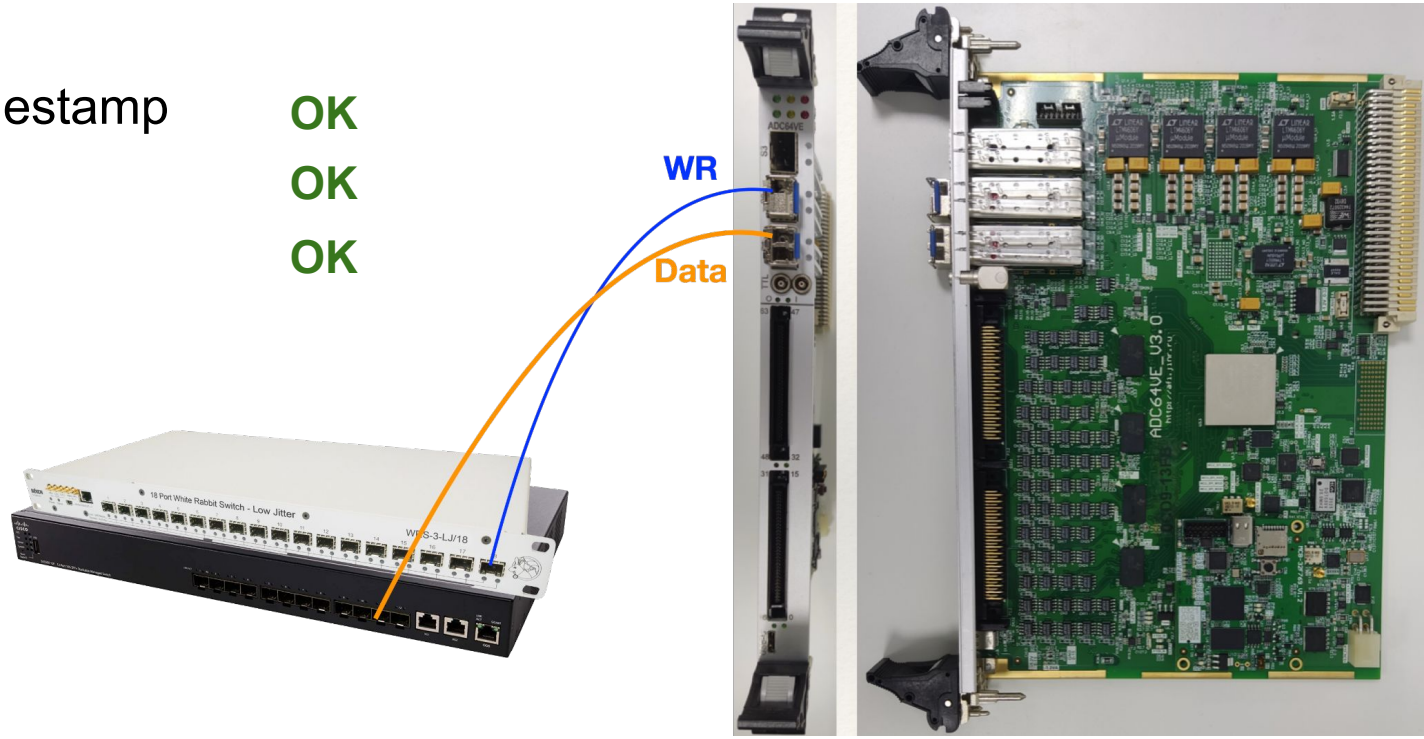
Design status:

- AFI ADC64 is chosen
  - 62,5MHz, 14-bit
  - WR client
  - Multi channel - 64 ch
  - 2048 sample digitization window
  - 10G Optical line data transfer
- White Rabbit switch, VXS crate for timing distribution ???

Prototyping:

- Initial testing ADC+WR switch on Module 1

https://edms.cern.ch/project/CERN-0000218199



Design Elements - Feedthrough, PSU

Off-the-shell power supplies -> **100% mature**

Custom feedthrough PCB - **50% mature**

Design drivers:

- Power the SiPM, cold preamps. **OK**
- Remote control **OK**
- Hermiticity, pressure safety, power/data fan-out **OK**

Design status:

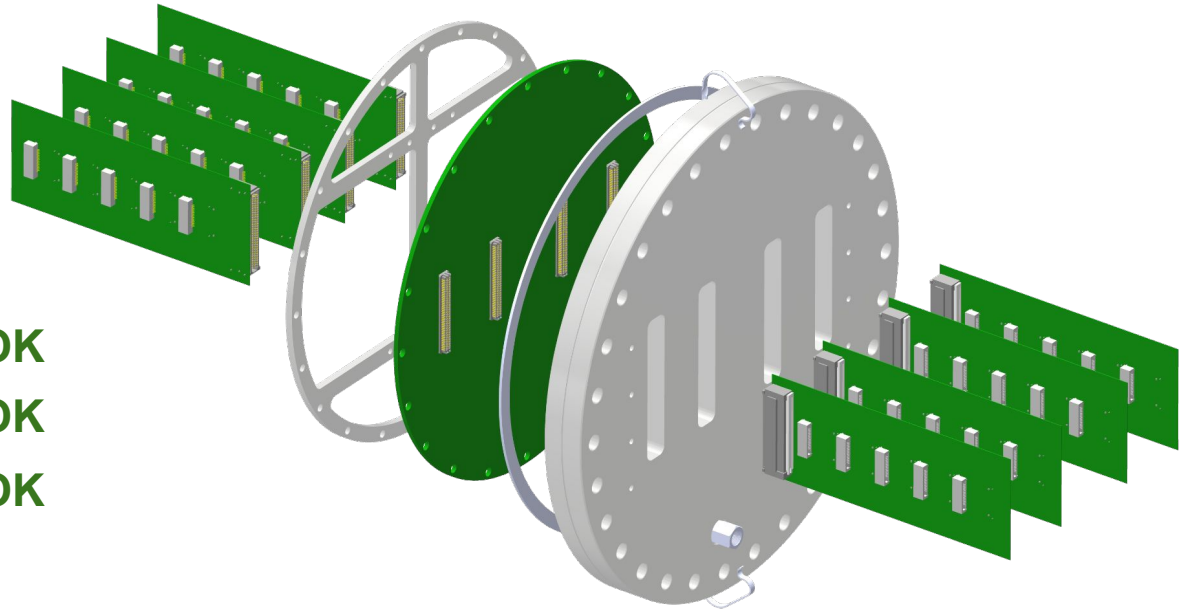
- Based on the charge system FT->pressure analysis
- FT model exists, layout need to be finalized
- For SiPM biasing TTi PLH120-p is chosen
- For LV DC -> Wiener LV MPOD or Lab PS

Prototyping:

- Module 0,1 FT have been tested, same design for Module 2,3
  - small PCB via flange fixed by compound
- TTi PS, Lab LV PS for Module 0,1

https://edms.cern.ch/project/CERN-0000230732

Feedthrough



TTi PLH120-P

Design Elements - Trigger, Calibration

Custom trigger unit - **90% mature, firmware update required**

LED or Laser calibration system - **50% mature**

Design drivers:

- Light insertion into the detector **OK**
- Custom trigger logic **OK**

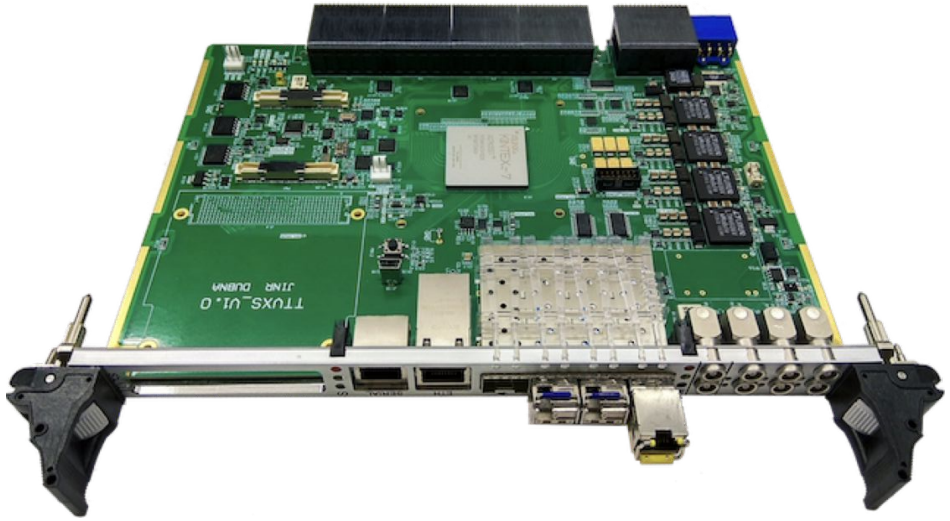
Design status:

- LED calib system or Common with charge
- Custom made trigger module by AFI on demand

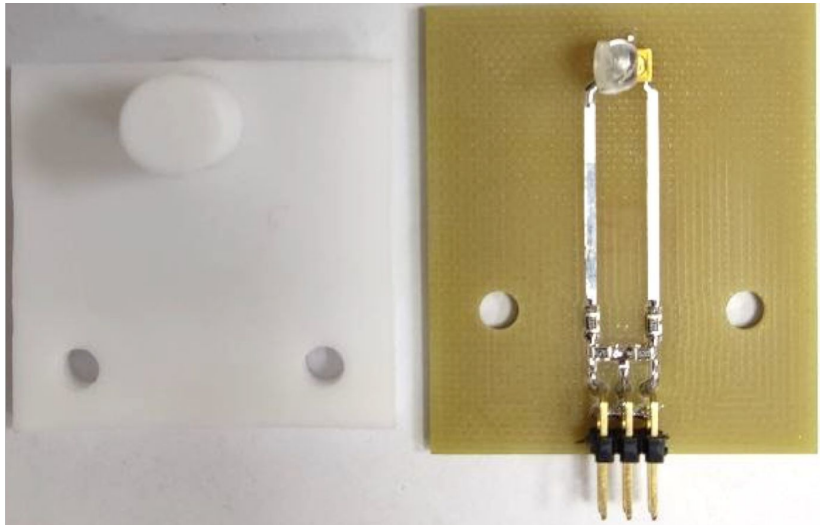
Prototyping:

- LED calibration system testing on Module 0,1
- NIM trigger modules on Module 0,1

Trigger unit

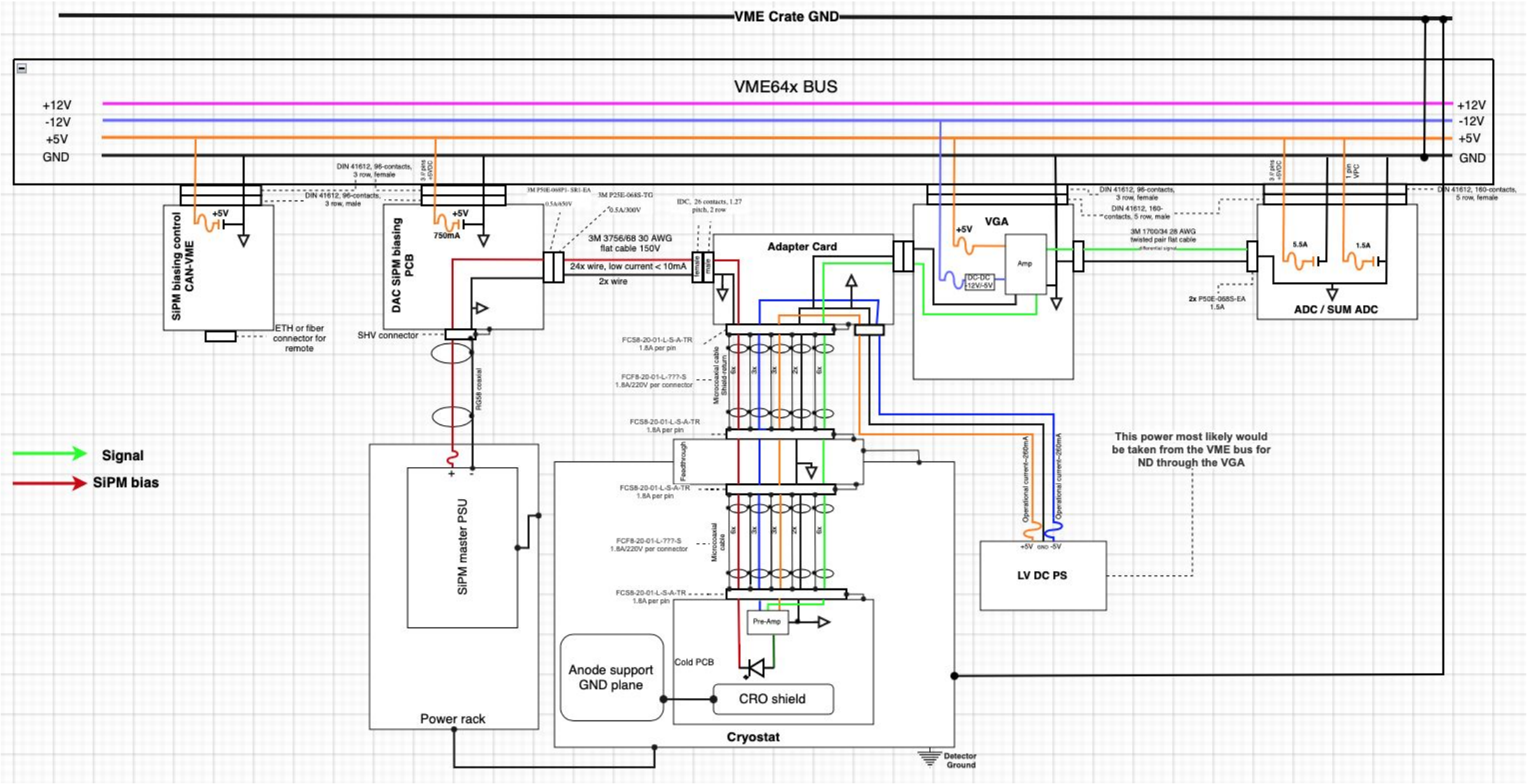


LED unit



Light Readout DC/signal/grounding distribution

First draft

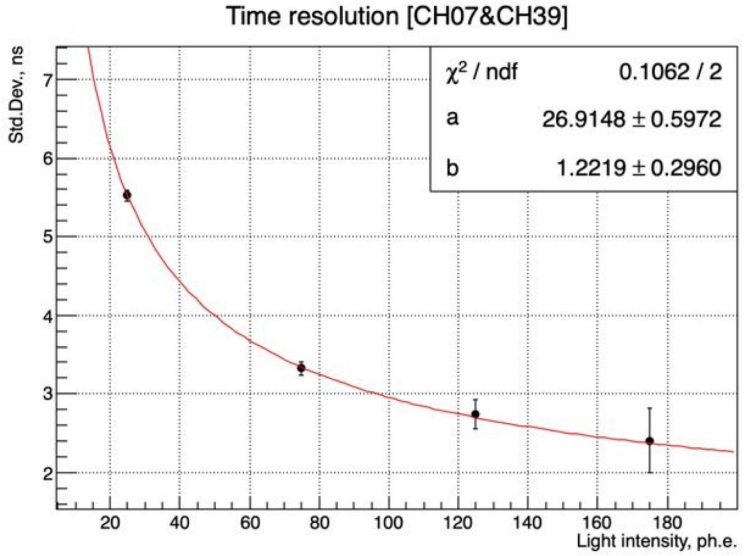


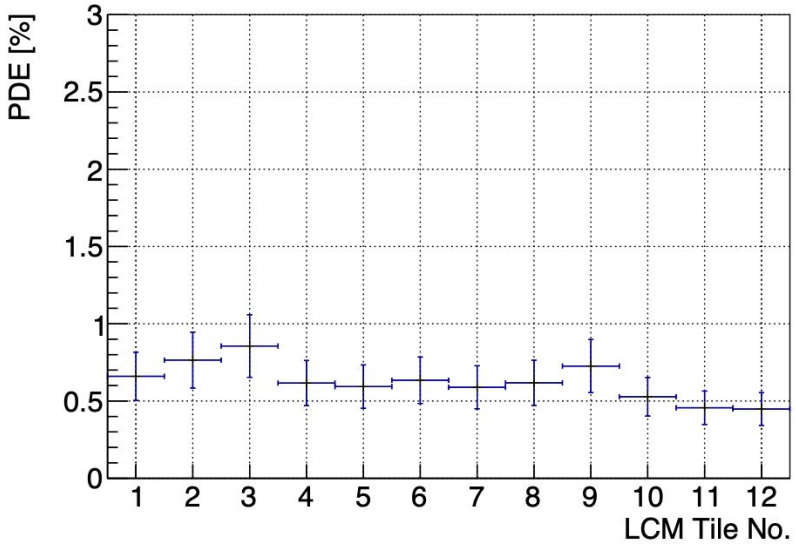
Analyses and/or Performance Assessment

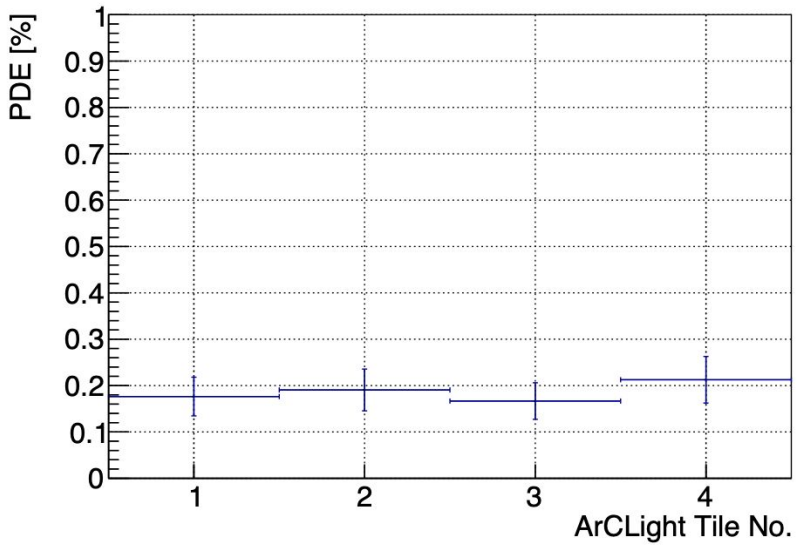
7	LRO-009	Specification	**time resolution of the LRO**	The time resolution of the photon detection system to resolve neutrino interaction time shall be < 10ns	< 10 ns	TBR
8	LRO-010	Specification	**Photon detection efficiency**	The photon detection efficiency shall satisfy to LRO-006, LRO-004, LRO-007.	>0.6%	

LCM PDE~0.62%

ACL PDE~0.2%

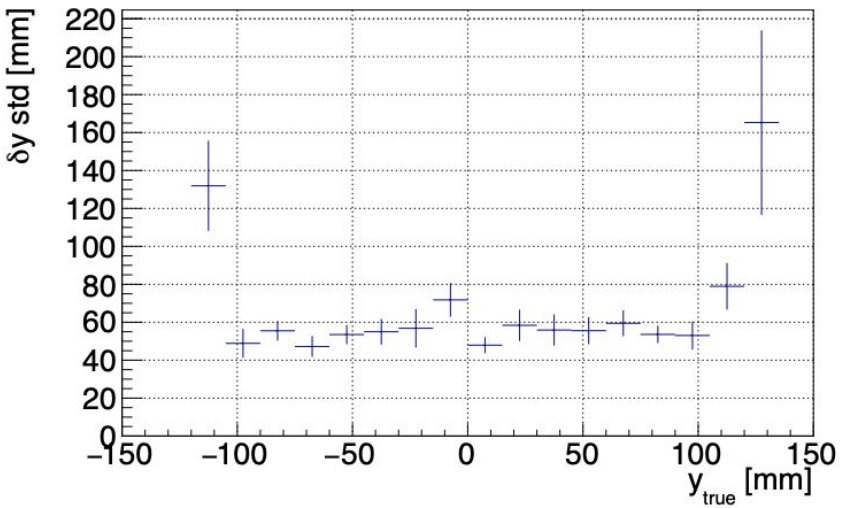




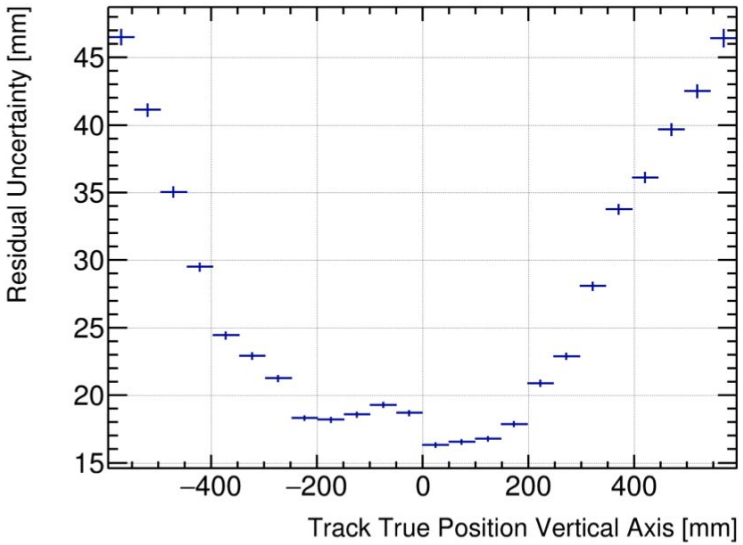


Analyses and/or Performance Assessment

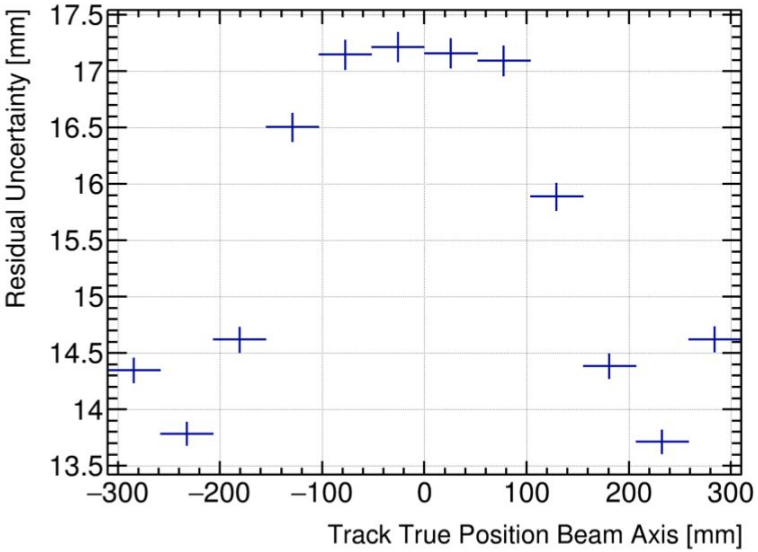
9	LRO-012	Specification	**Spatial Resolution/ fast timing within a module**	Horiz/Vert spatial resolution shall be ~10 cm	~10 cm



ArCLight spatial resolution reconstructed from SingleCube data (Vertical direction)



Light Readout spatial resolution simulation for ArgonCube TPC (Vertical direction)

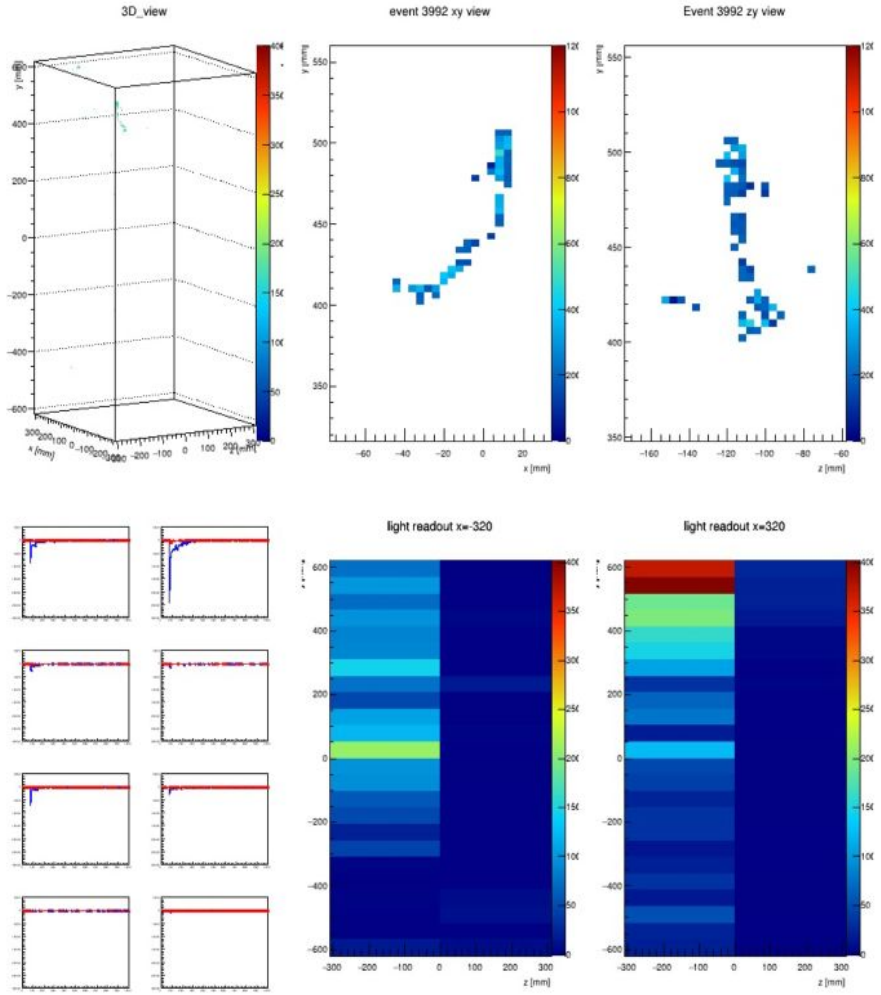


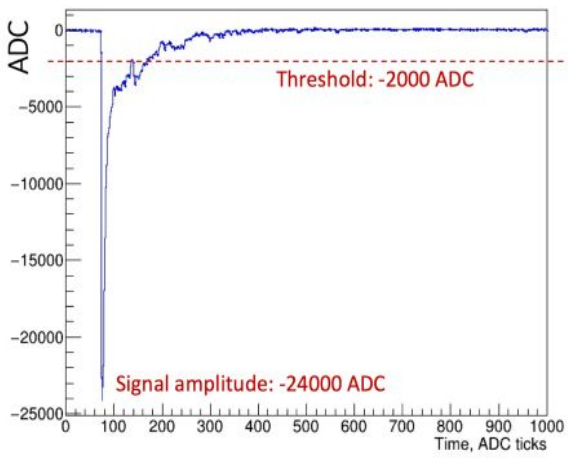
Light Readout spatial resolution simulation for ArgonCube TPC (along beam direction)

Analyses and/or Performance Assessment

4	LRO-006	Specification	**LCM Light threshold**	3LCM Modules shall be triggered when there is greater than ~ 7500 LAr photons	~ 7500 LAr photons

- Trigger signal is based on the sum channels of the LCM light readout with threshold at -2000 ADC ch.
- This is a gamma conversion with total energy deposition of ~20 MeV
- Sum signal peak at ~ 24000
- So effective threshold was 1.6 MeV
- Given signal clarity we can operate at lower threshold below 1 MeV
- Threshold ~ 16 ph.e., 120ADC/ph.e
- Fast/Total = 0.35 -> PDE=0.62% -> 2750/0.35~7500 LAr photons

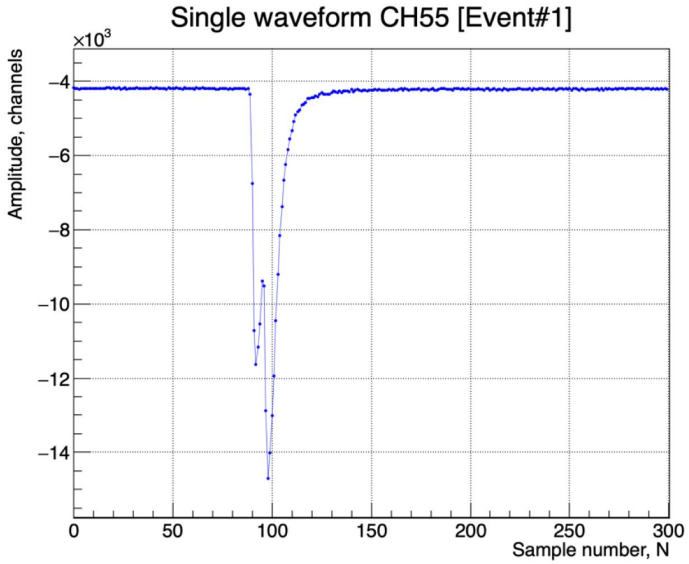




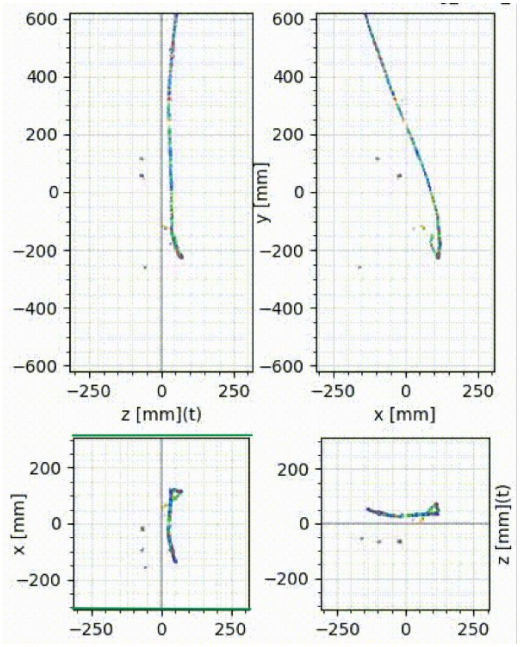
Analyses and/or Performance Assessment

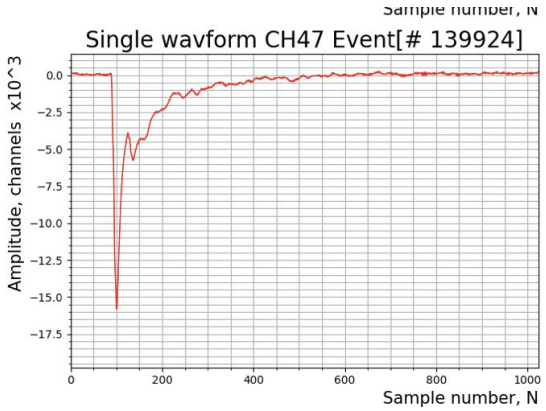
6	LRO-008	Specification	**pileups time resolution**	LRO shall be able to resolve 2 signals separated by > 200ns	~ 200 ns
	LRO-020	Specification	**Light system calibration**	There shall be a light system calibration for time calibration of different light modules due to different signal lines	<1ns

100 ns, LED double pulse

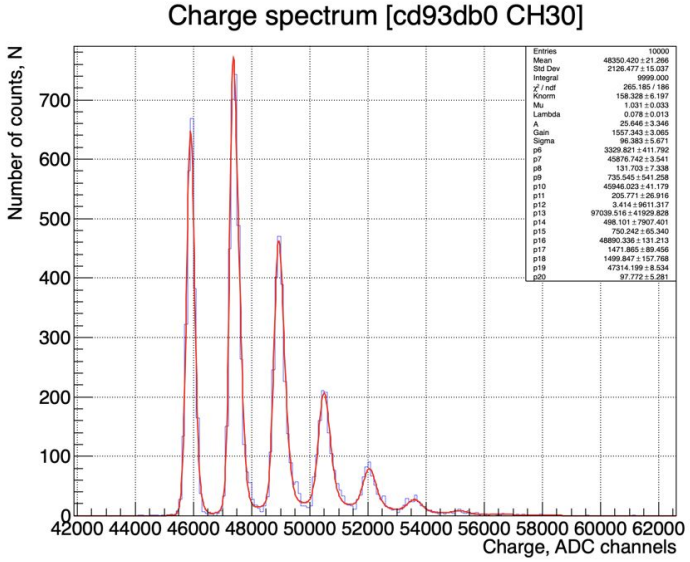


~250 ns pile-up, Michel event



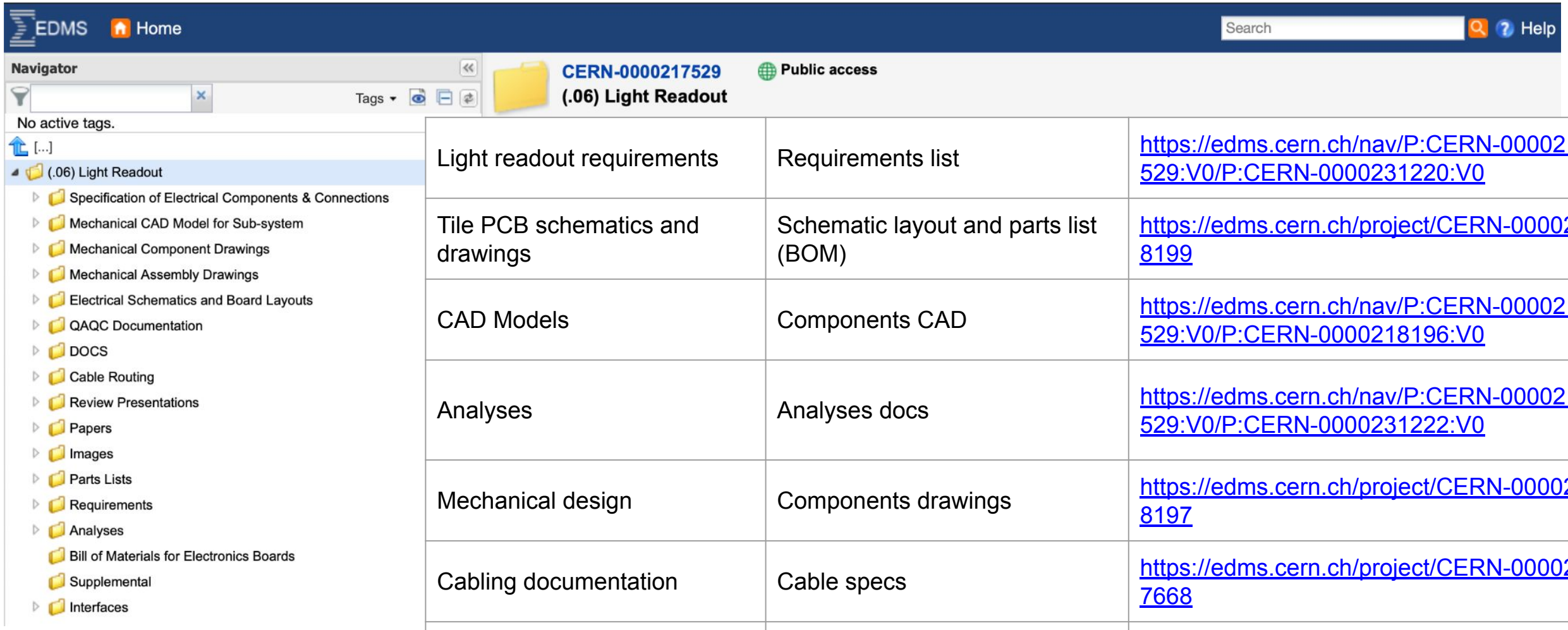


Calibration spectrum



Documentation Tour

https://edms.cern.ch/project/CERN-0000217529



Light readout requirements	Requirements list	https://edms.cern.ch/nav/P:CERN-0000217529:V0/P:CERN-0000231220:V0
Tile PCB schematics and drawings	Schematic layout and parts list (BOM)	https://edms.cern.ch/project/CERN-0000218199
CAD Models	Components CAD	https://edms.cern.ch/nav/P:CERN-0000217529:V0/P:CERN-0000218196:V0
Analyses	Analyses docs	https://edms.cern.ch/nav/P:CERN-0000217529:V0/P:CERN-0000231222:V0
Mechanical design	Components drawings	https://edms.cern.ch/project/CERN-0000218197
Cabling documentation	Cable specs	https://edms.cern.ch/project/CERN-0000217668
Light readout interfaces	Interfaces to subsystems	https://edms.cern.ch/nav/P:CERN-0000217529:V0/P:CERN-0000231364:V0

ESH Codes and Standards

- All commercial electrical equipment needs NRTL approval (UL, ETL etc)
  - Computers and networking equipment
  - Power supplies
  - If no NRTL listed equivalent exists, needs to be approved by FNAL
- All power cabling shall meet specifications in FNAL engineering handbook:
  - See Table 2, Page 6 https://esh-docdb.fnal.gov/cgi-bin/sso/RetrieveFile?docid=2781)
- All custom PCBs need to meet specifications in the FNAL engineering handbook and pass ORC approval. (see especially pages 3 and 5)
  - See example document for VGA on 2x2: DUNE-doc-24868
    - **VGA, ADC, SiPM biasing ORC is ongoing in Fermilan for 2x2**
  - Focus of ORC is fire prevention
- Light readout uses VME powered boards, low power supplies <200W.
  - No additional hazards.

Open Design Issues / Path to FSD & FDR

Current preliminary design status:

- Scaling up light detectors to FSD is ongoing
- Electronics design 80% mature for FSD
- DAQ & timing mature for FSD

Open Design tasks:

- 60ch VGA PCB design is ongoing
- Cable choice for FSD: microcoaxial or flexPCB
- Full size feedthrough design for FSD
- Trigger unit configuration or upgrade to required needs for ND, has not been tested
- Calibration system choice
- Slow control software implementation to DUNE ND SC

Summary

Status

- Light system maturity
  - 80% feature complete
- Front-End Electronic design choices maturity
  - PCB design process 75% complete
  - 2x2 program design 100% complete
- DAQ, timing, SiPM bias maturity - 100%
- Cabling and Feed-through design is mature
  - Feed through 90% complete, Cabling selection and validation 60% complete

Final Design Phase

- Calibration system option
- Verify system level performance (FSD)
- Verify cabling performance in LAr

Summary

The Light Readout system design maturity meets PDR requirements.

Moving forward towards FDR we will refine the design.