

# DAPHNE Baseline noise

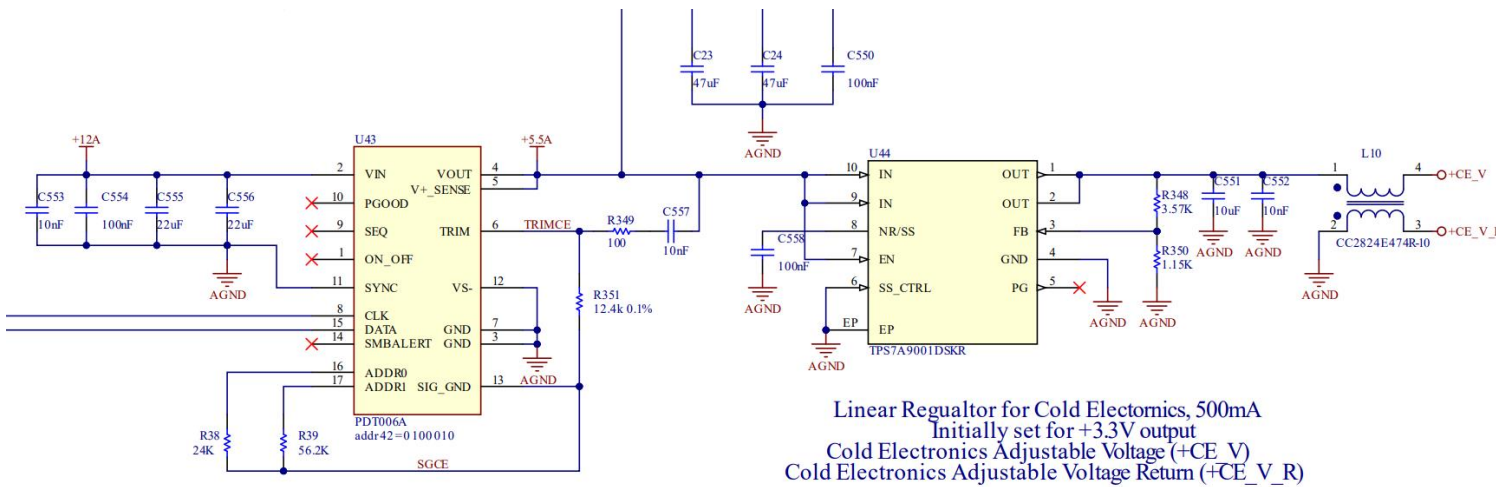
E. Cristaldo , M. Delgado , C. Gotti , F. Terranova

June 20<sup>th</sup> , 2022

## Introduction

- The following slides provides some evidence of the presence of noise at the inputs of DAPHNEs AFE digitalization chips.
- The noise is injected at the input nodes before the bias-trim decoupling capacitors through the **TRIM circuitry**, the **Analog Multiplexer for the Current Monitoring system** and the **BIAS supply circuitry**.
- The noise originates from the switching regulators for the +5A,-5A. The noise reaches the AFE through VDD and VEE of the mentioned components, possibly due inadequate PSSR. Our most compelling evidence for this hypothesis is that we have detected the switching frequencies components of the regulators in the digitalized waveforms.
- We have detected a 200KHz oscillation at the +5,5V regulator output that is used exclusively for powering the linear 3,3V regulator that feeds V\_CE for the cold amplifier.
- We have applied filter patches at the BIAS and TRIM nodes to mitigate the noise in the acquired waveforms.
- We will present how we addressed these issues and the result in the waveforms signals from the cold amplifier.

# 200KHz oscillation at +5,5V rail



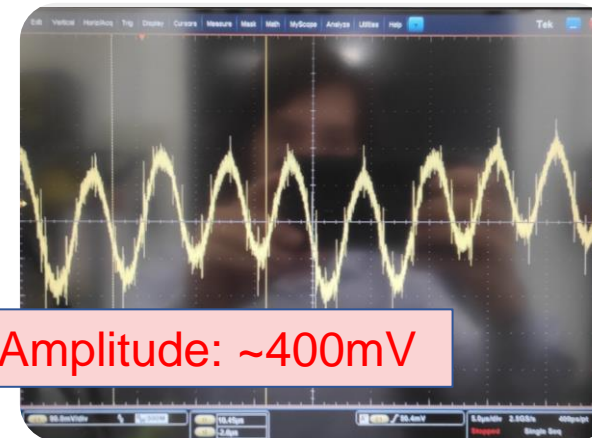
## Applied PATCH

- First, we lowered the output voltage to +5V changing R351 to 2,7KΩ.
- Looking into the datasheet, we found the recommended values for Rtune and Ctune (R349 and C557).
- **Changing Rtune from 100Ω to 270 Ω and Ctune from 10nF to 2200pF mitigated the oscillation.**

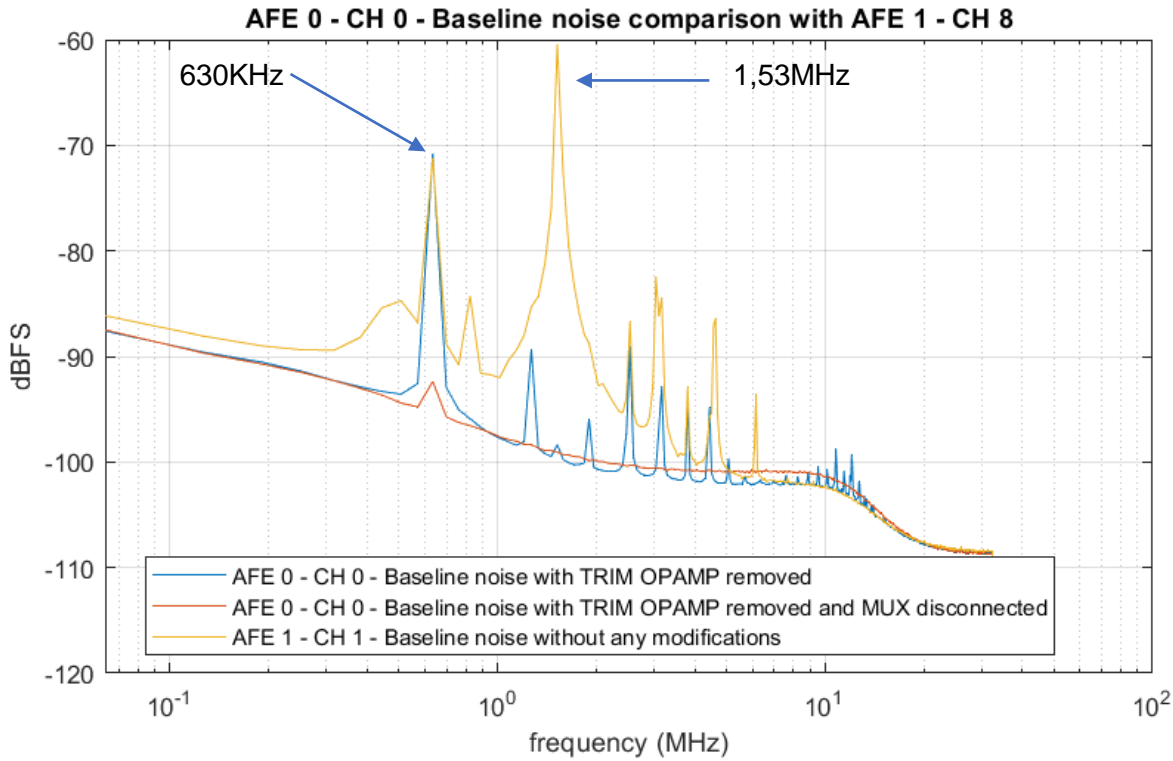
Table 3. Recommended values of RTUNE and CTUNE to obtain transient deviation of 2% of Vout for a 3A step load with Vin=12V.

Vo	5V	3.3V	2.5V	1.8V	1.2V	0.6V
Co	2x47μF	3x47μF	3x47μF	1x330μF Polymer	2x330μF Polymer	4x330μF Polymer
RTUNE	270	180	180	180	180	180
CTUNE	2200pF	3300pF	3300pF	4700pF	12nF	33nF
ΔV	76mV	48mV	47mV	33mV	18mV	10mV

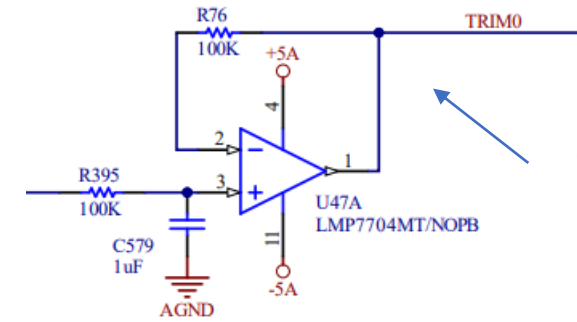
Note: The capacitors used in the Tunable Loop tables are 47 μF/3 mΩ ESR ceramic and 330 μF/12 mΩ ESR polymer capacitors.



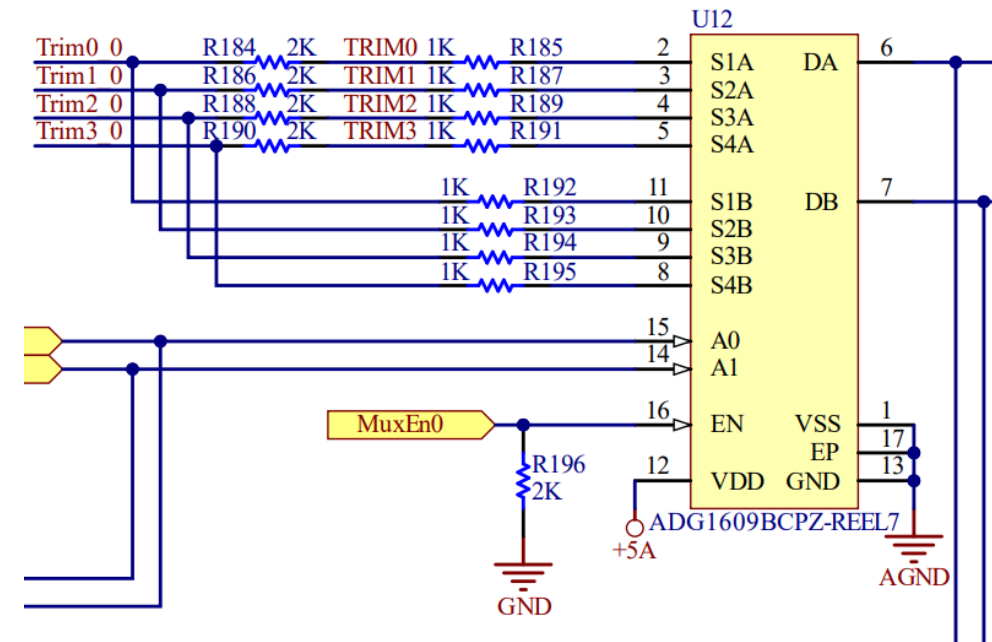
# Noise at the AFE inputs



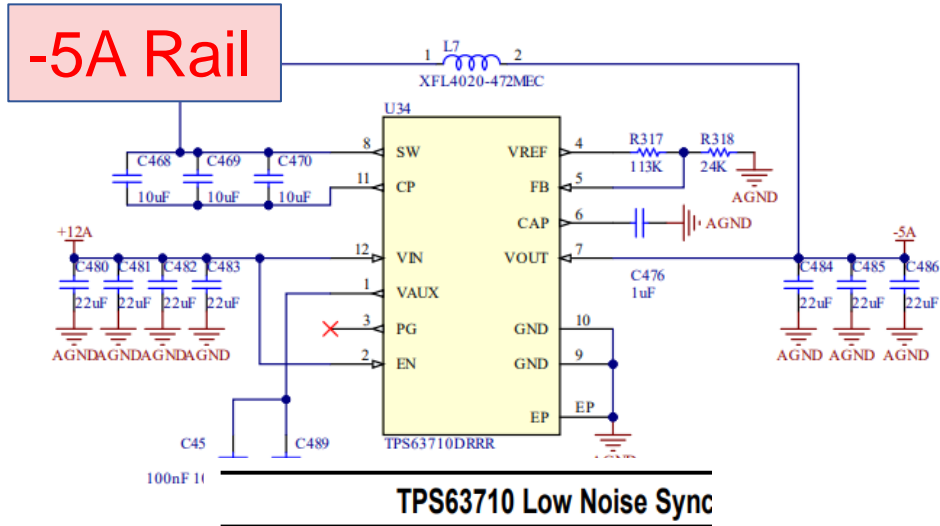
- The noise spectrum in yellow corresponds to the overall noise seen at the AFE input.
- Removing U47 and grounding the TRIM node immediately improves the noise levels, eliminating the 1,53MHz component originating at the -5V rail.
- Removing R192 from U12 eliminates the 630KHz component.



- LMP7704 was removed and TRIM node was grounded.



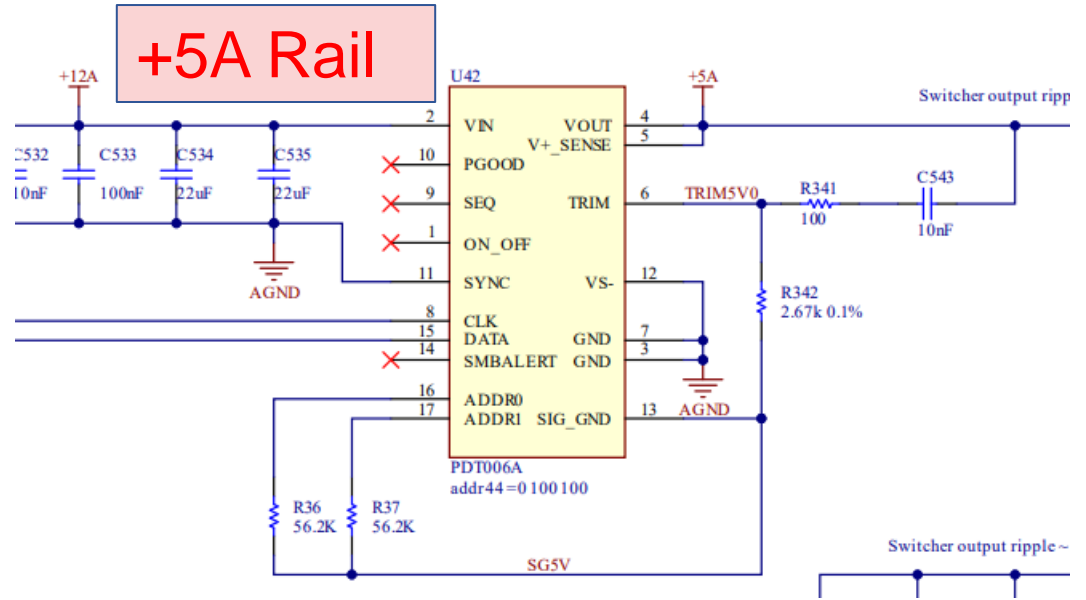
# Switching Frequencies of regulators



TPS63710 Low Noise Sync

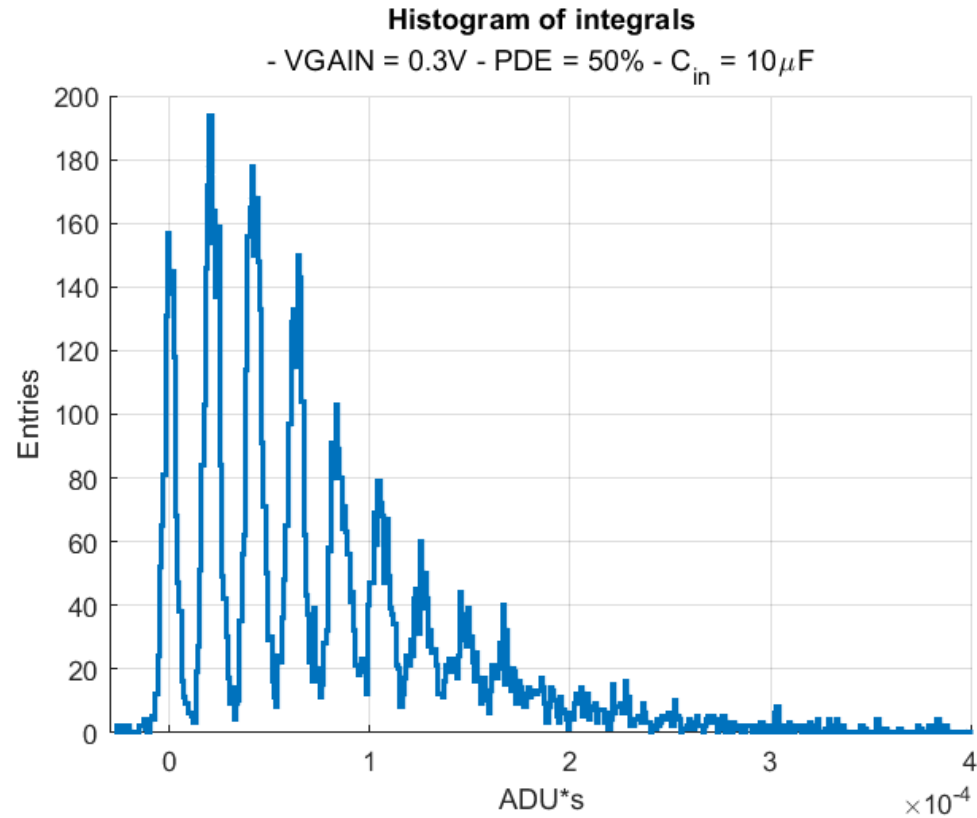
## 1 Features

- 3.1 V to 14 V Input Voltage Range
- 1 A Output Current
- Up to 91% Efficiency
- $\pm 1.5\%$  Output Voltage Accuracy
- Synchronous Rectification
- Low 1/f-Noise Reference System
- Noise:  $22 \mu\text{V}_{\text{RMS}}$  (10 Hz to 100 kHz)
- Output Voltage: -1 V to -5.5 V
- $|V_{\text{out}}| < 0.7 \times V_{\text{in}}$
- 1.5-MHz fixed frequency PWM mode
- Thermal Shutdown
- 5- $\mu\text{A}$  Shutdown Current
- 3-mm  $\times$  3-mm WSON Package
- Create a Custom Design Using the TPS63710 With the [WEBENCH® Power Designer](#)



Efficiency $V_{\text{in}} = 12\text{Vdc}$ , $T_{\text{A}} = 25^\circ\text{C}$ $I_{\text{o}} = I_{\text{o, max}}$ , $V_{\text{o}} = V_{\text{o, set}}$	$V_{\text{o, set}} = 0.6\text{Vdc}$	$\eta$		75.6		%
	$V_{\text{o, set}} = 1.2\text{Vdc}$	$\eta$		85.0		%
	$V_{\text{o, set}} = 1.8\text{Vdc}$	$\eta$		88.6		%
	$V_{\text{o, set}} = 2.5\text{Vdc}$	$\eta$		90.6		%
	$V_{\text{o, set}} = 3.3\text{Vdc}$	$\eta$		92.1		%
	$V_{\text{o, set}} = 5.0\text{Vdc}$	$\eta$		93.8		%
Switching Frequency	All	$f_{\text{sw}}$	—	600	—	kHz

# Histogram obtained after modifications

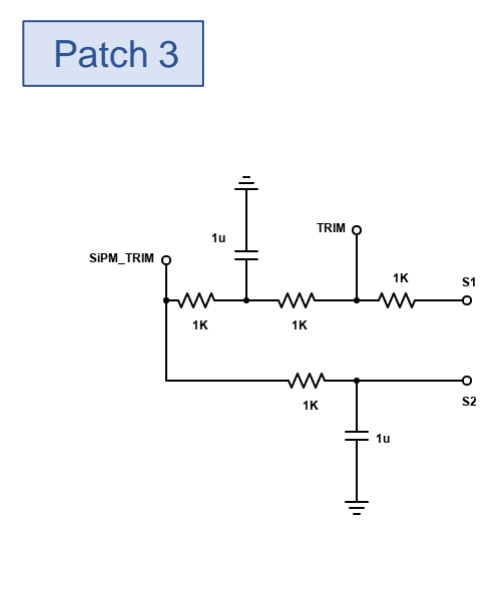
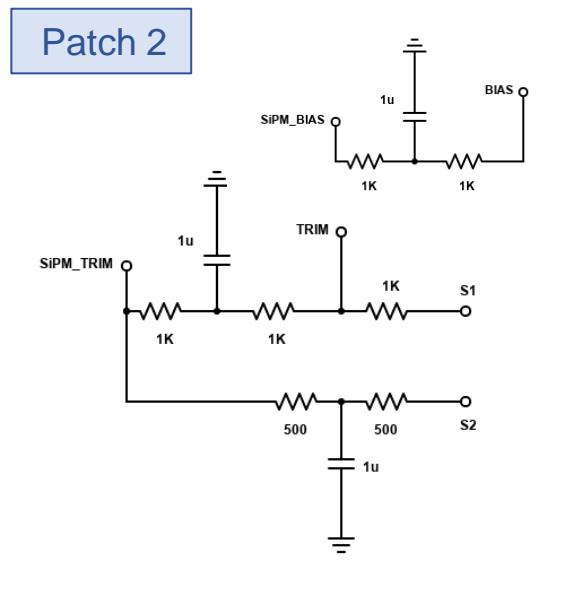
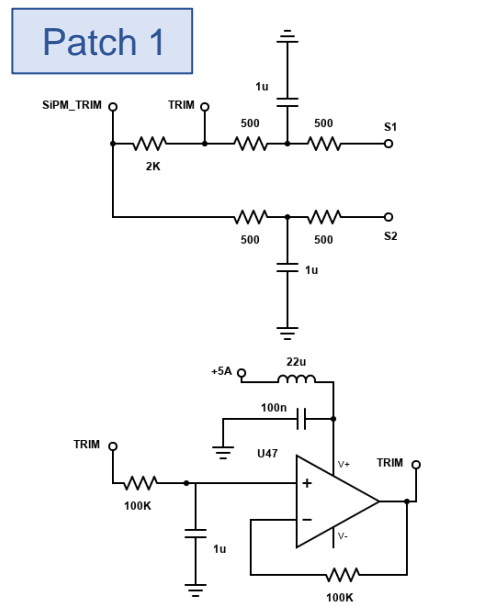
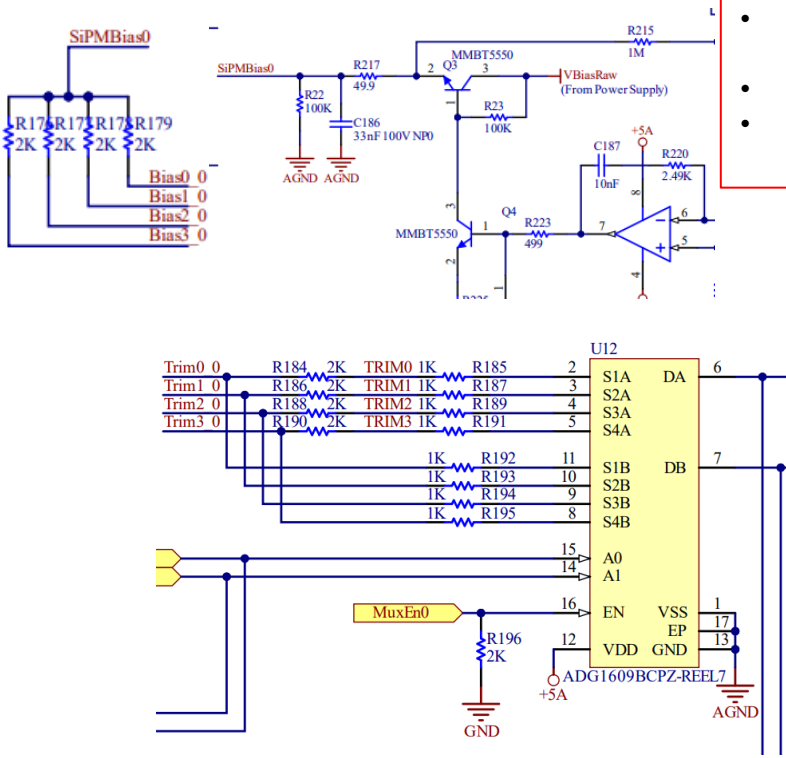


- After the modifications we have obtained this histogram at a PDE of 50%.
- But the modifications have removed the Current Monitoring and TRIM capabilities

# Patches applied to recover TRIM and Current Monitoring systems

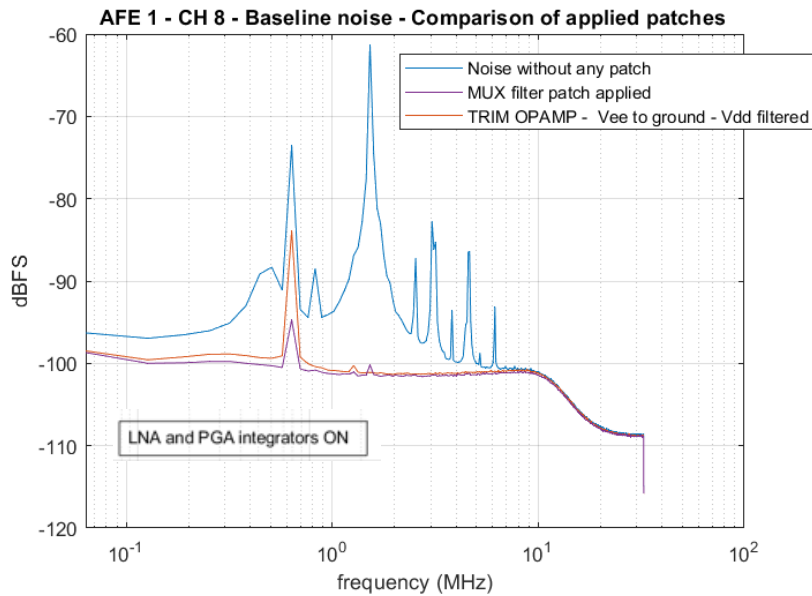
- Three different patch have been applied in successive ordering. Each one of them trying to minimize the number of modifications and components needed.

- To filter better the SiPM bias, R217 value was changed to 1K and C186 was changed to 1u.
- This bias patch is included in (1) and (3)
- Patch (2) splits the 2K resistor (R179) to form a filter with a 1u capacitor.

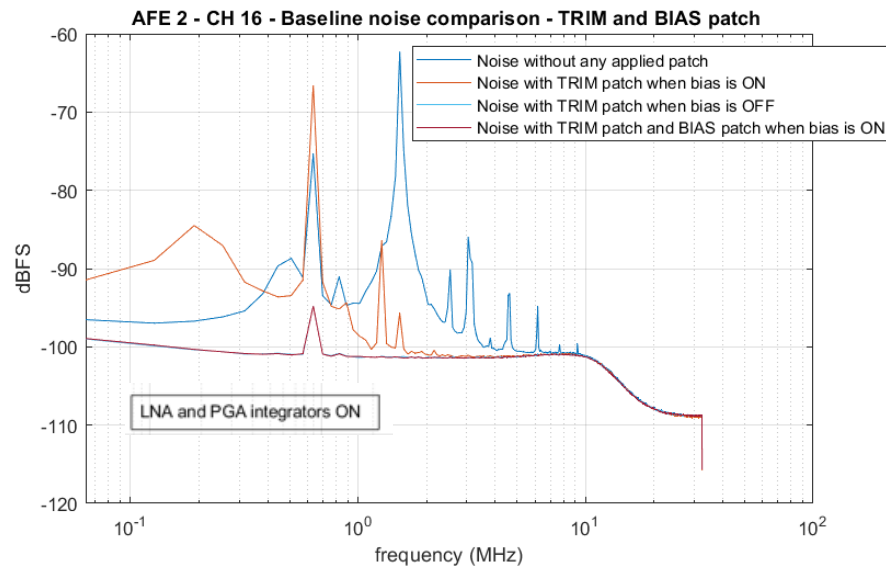


# Patches applied to recover TRIM and Current Monitoring systems

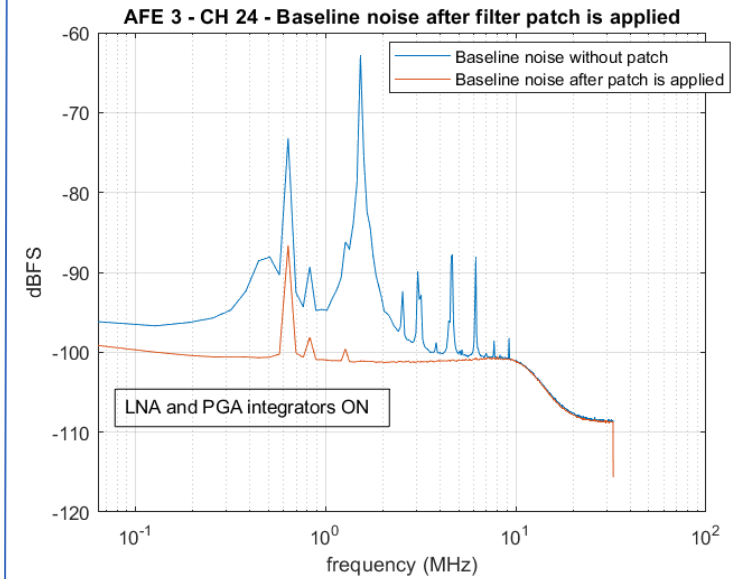
Patch 1



Patch 2



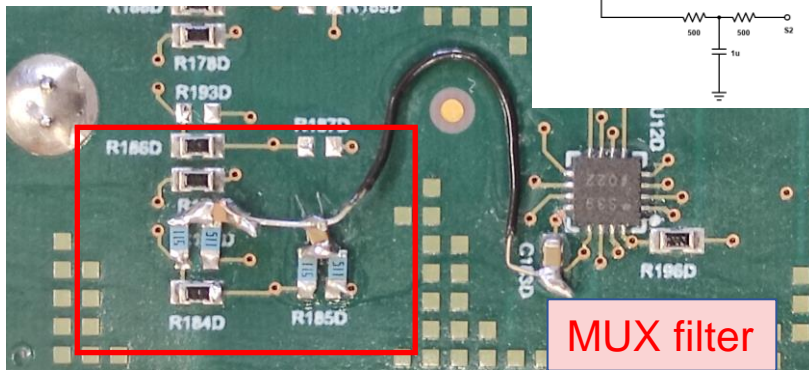
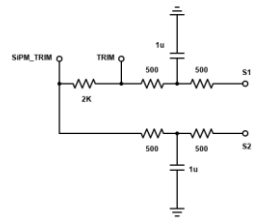
Patch 3



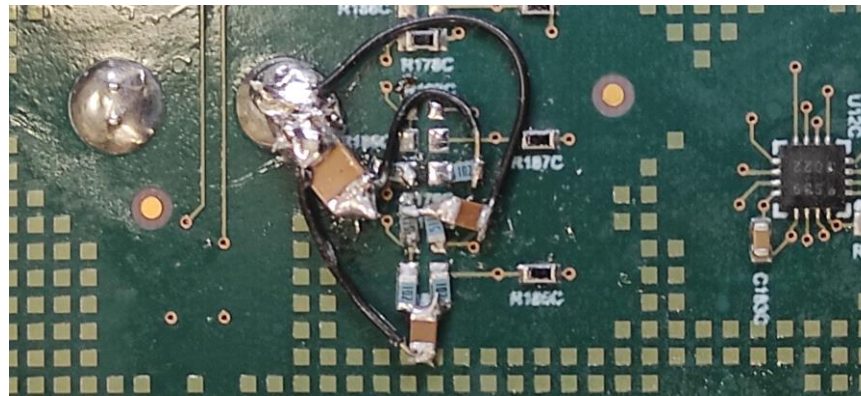


# Patches applied to recover TRIM and Current Monitoring systems

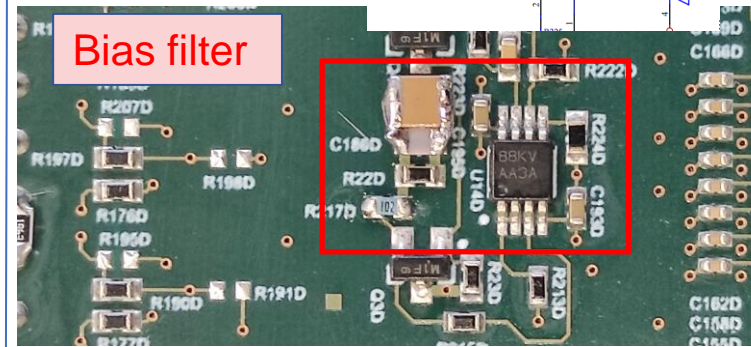
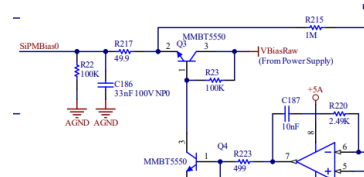
Patch 1



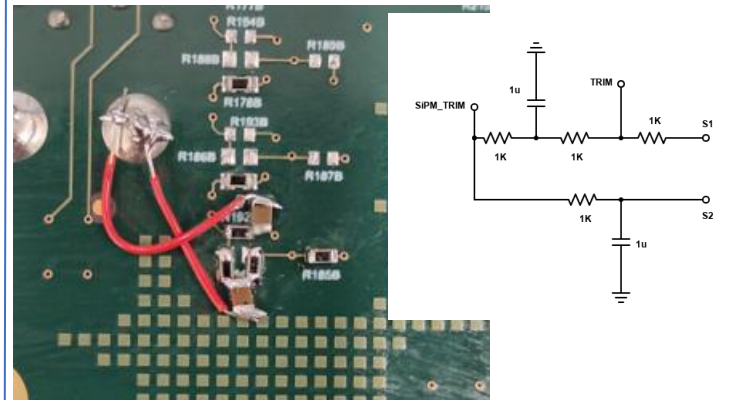
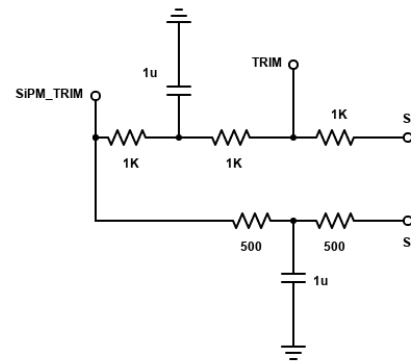
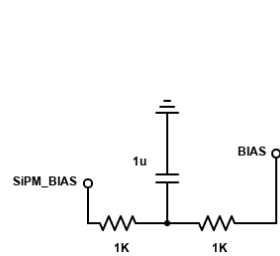
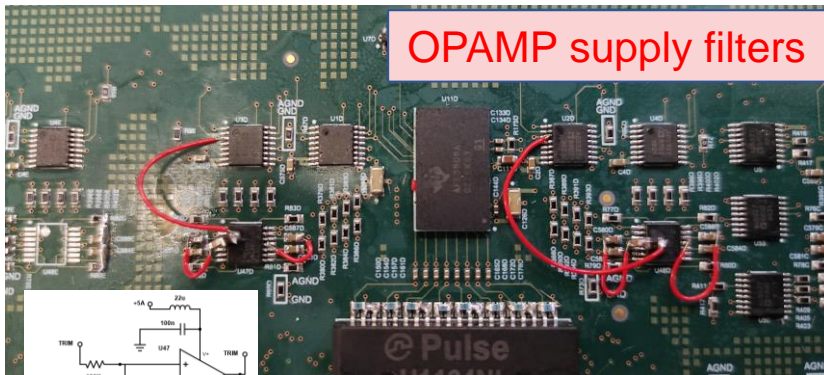
Patch 2



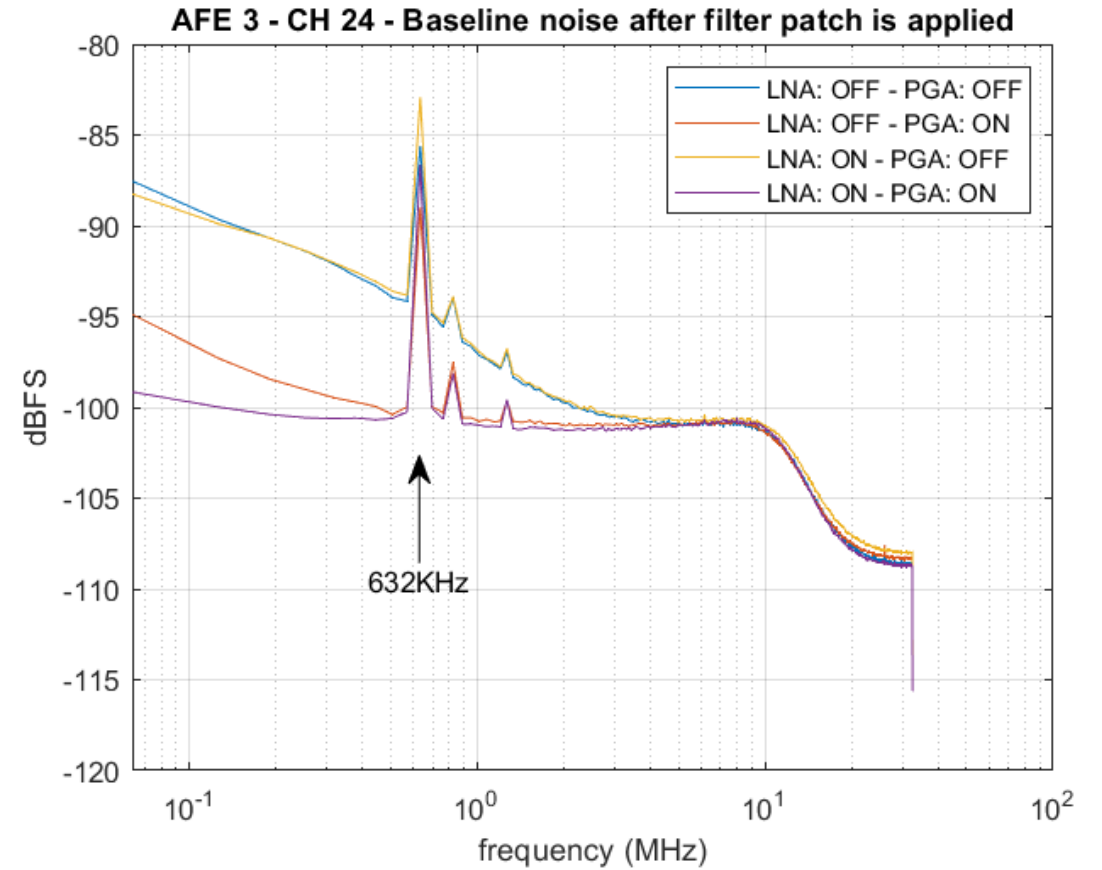
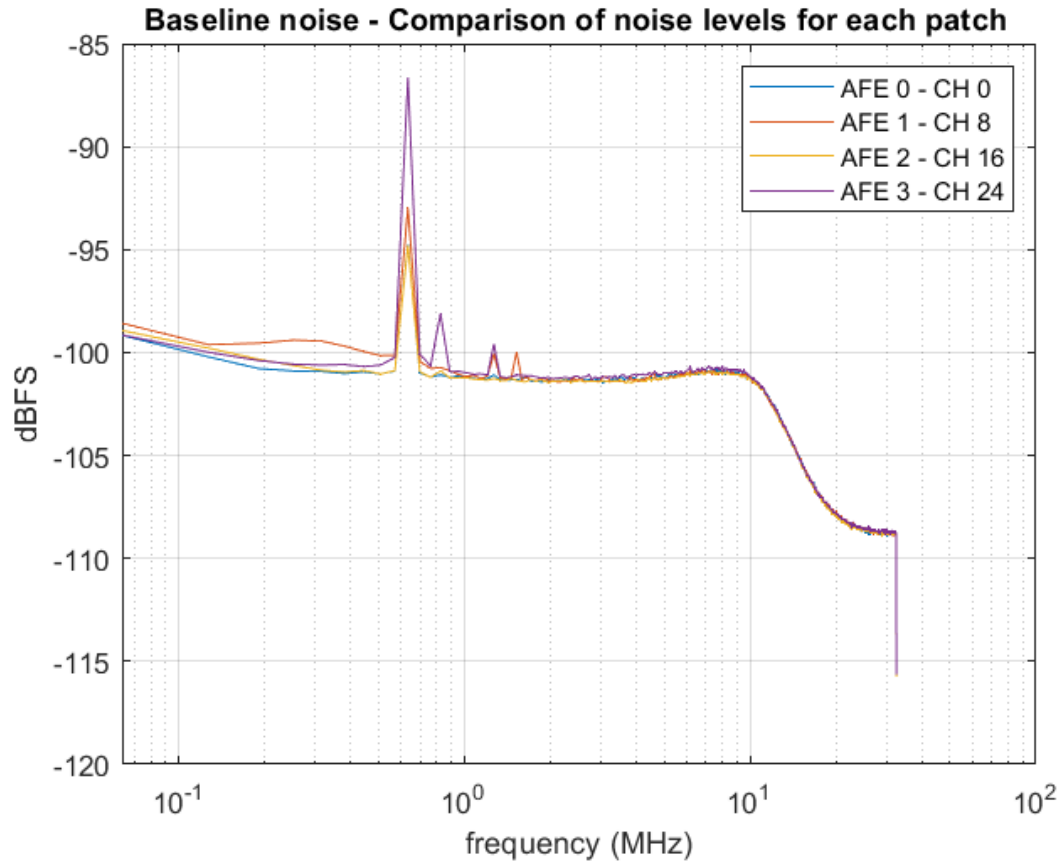
Patch 3



OPAMP supply filters



# Result and comparison with integrators

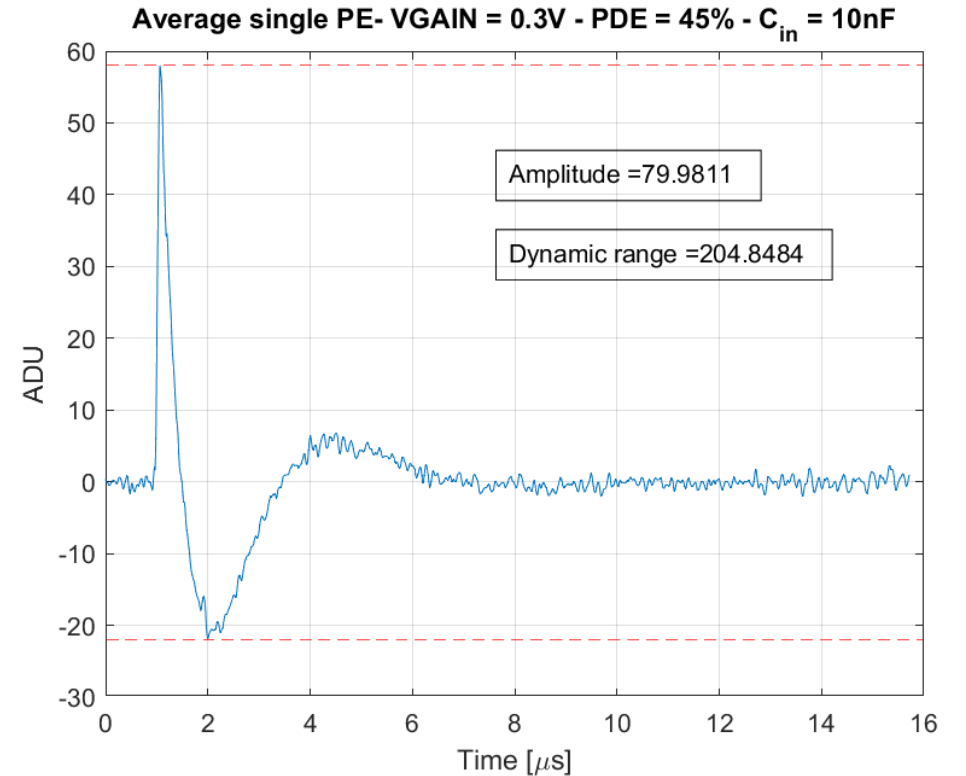
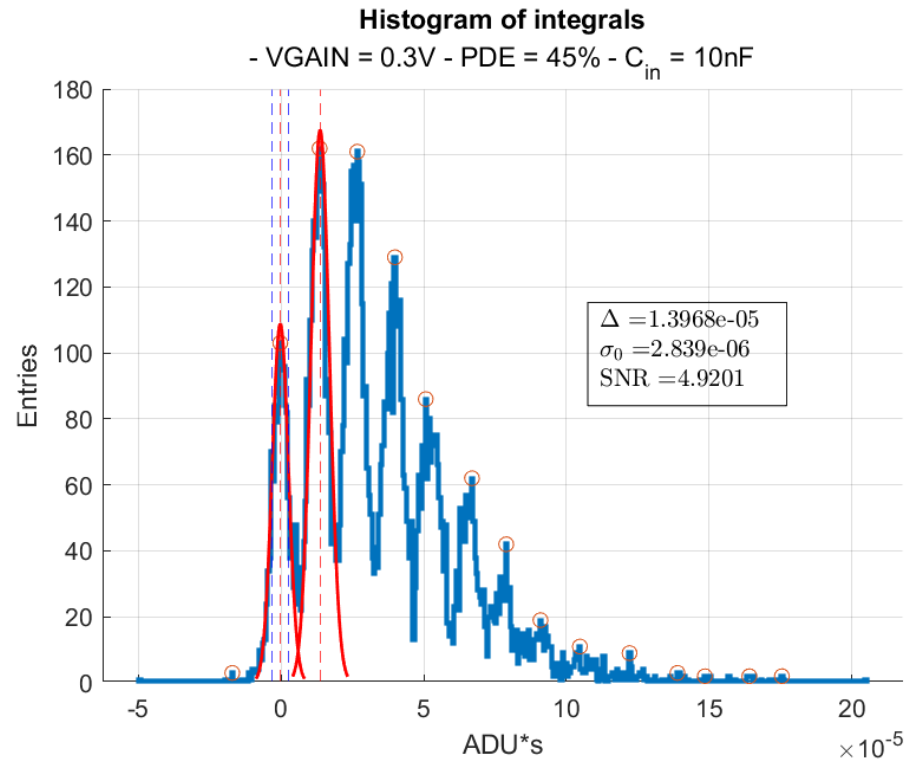


## Cold amplifier testing after applying the patches

- After applying the patches, we tested the cold amplifier with various configurations using FBK SiPMs.
- These are configurations are:
  - PDE at 40%, 45% and 50%.
  - VGAIN 0,3V and 0,5V.
  - Input capacitors: 10nF and 100nF.
  - Integrators ON and OFF.

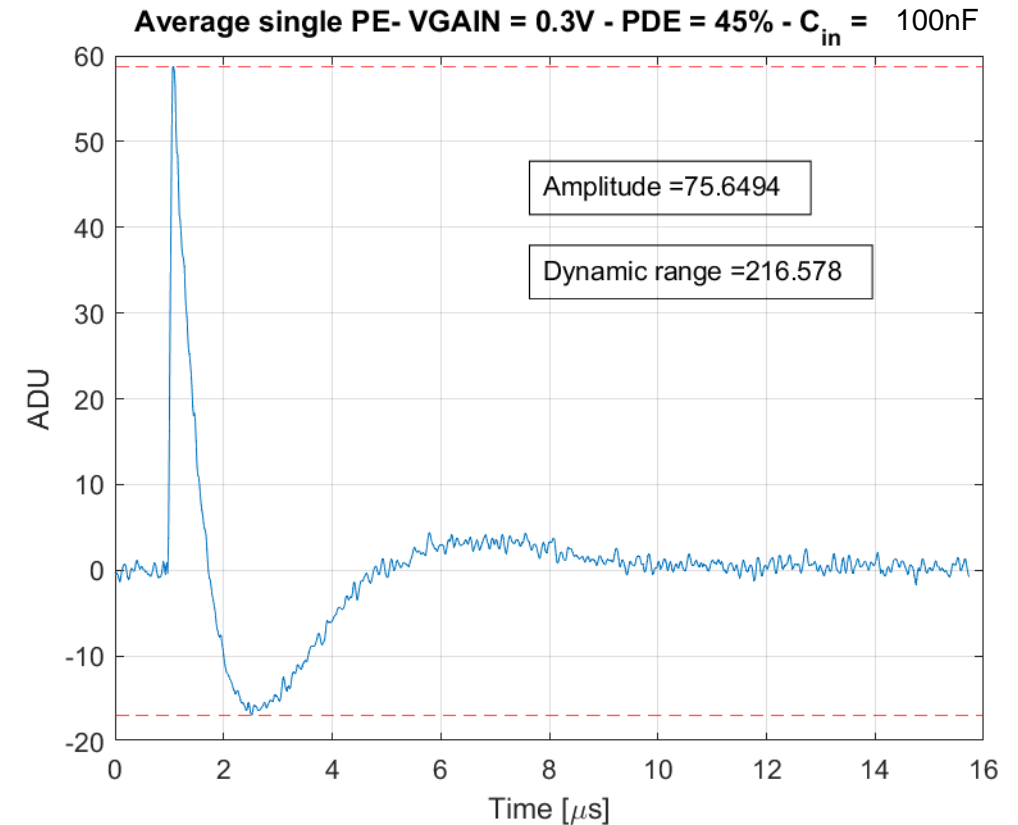
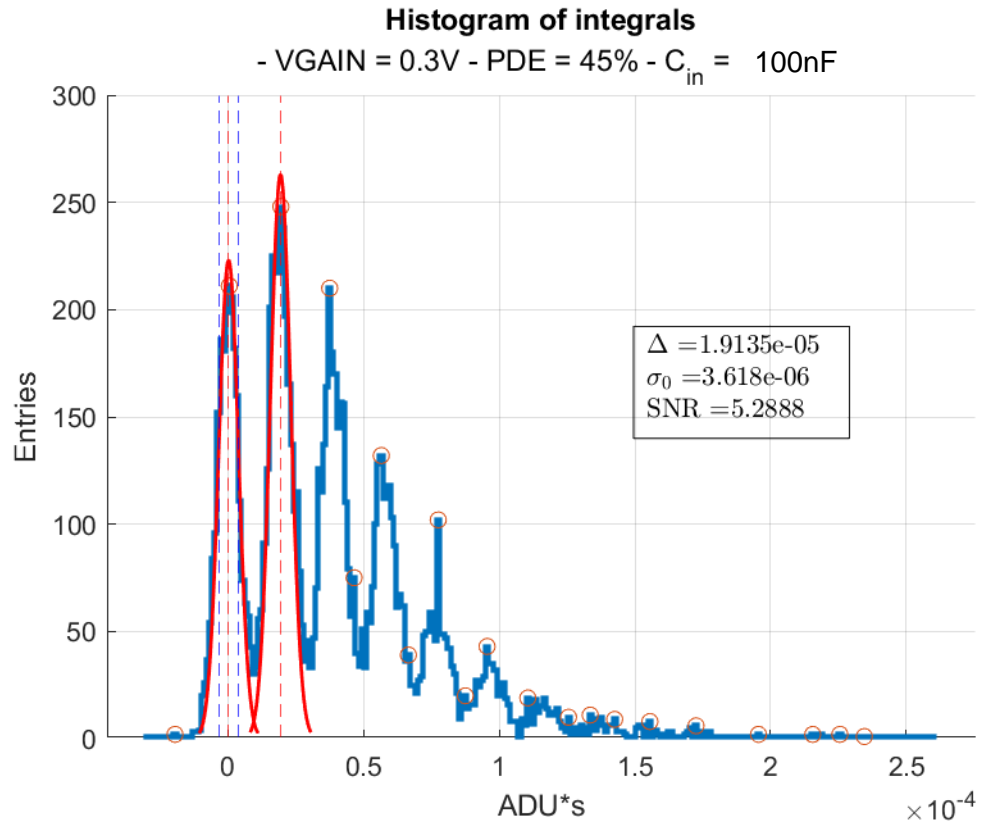
# Cold amplifier testing after applying the patches

PGA integrator ON



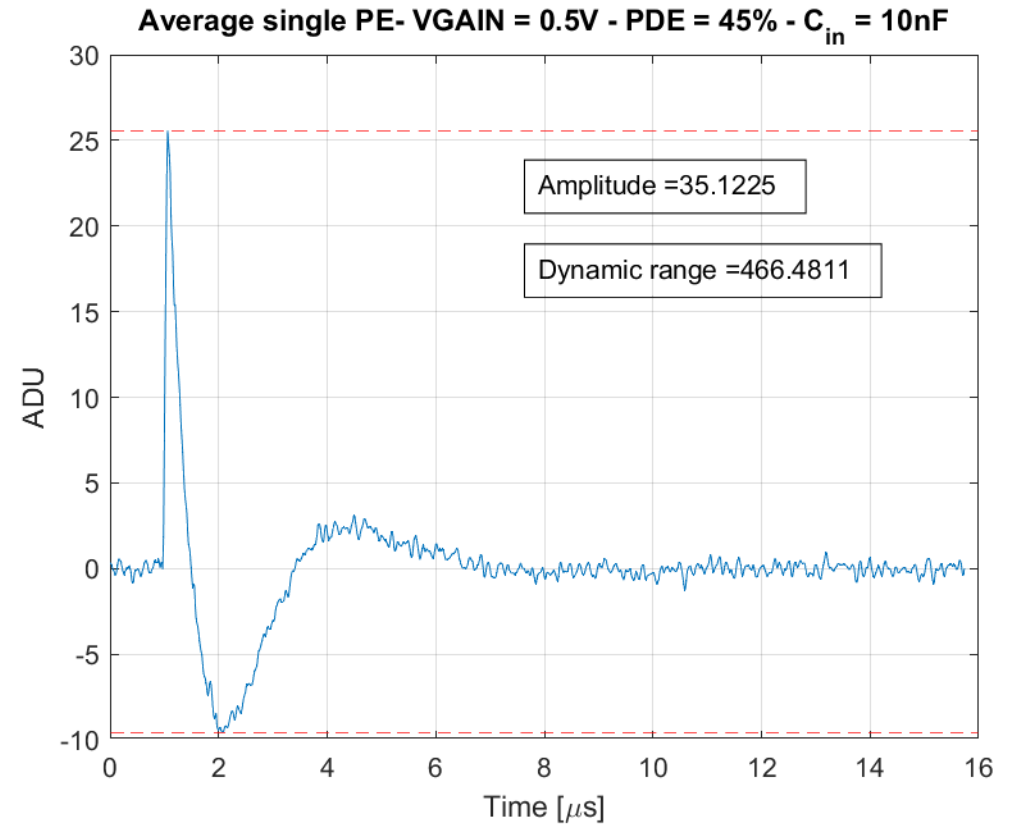
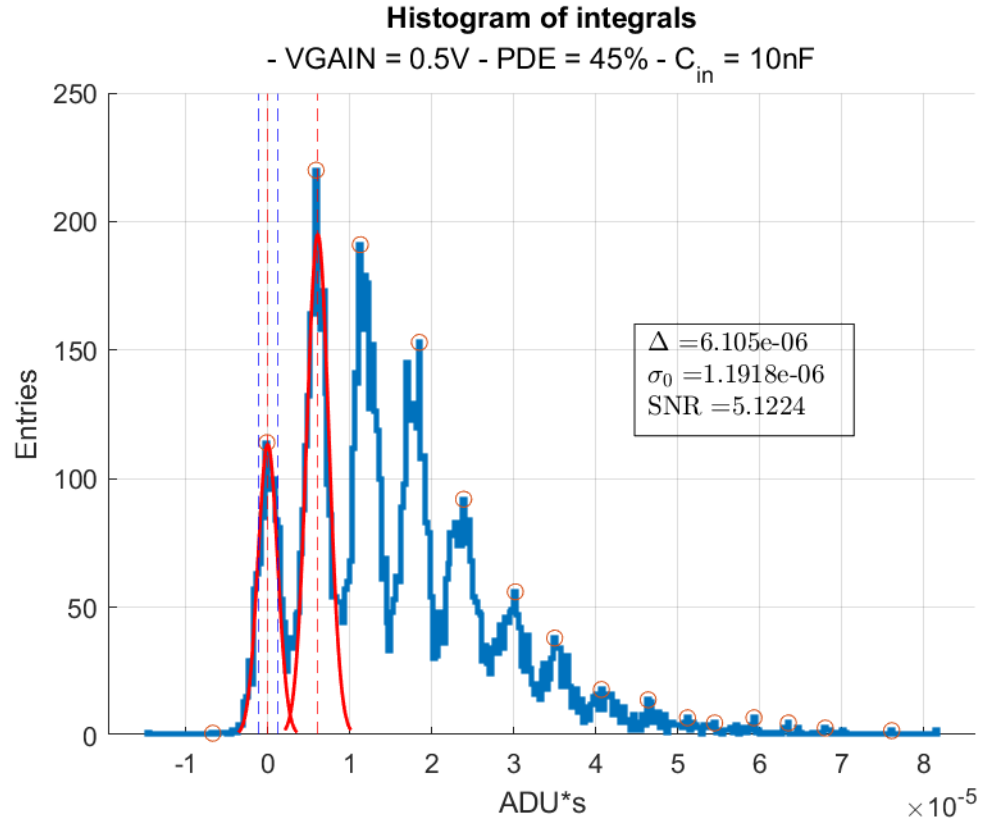
# Cold amplifier testing after applying the patches

PGA integrator ON



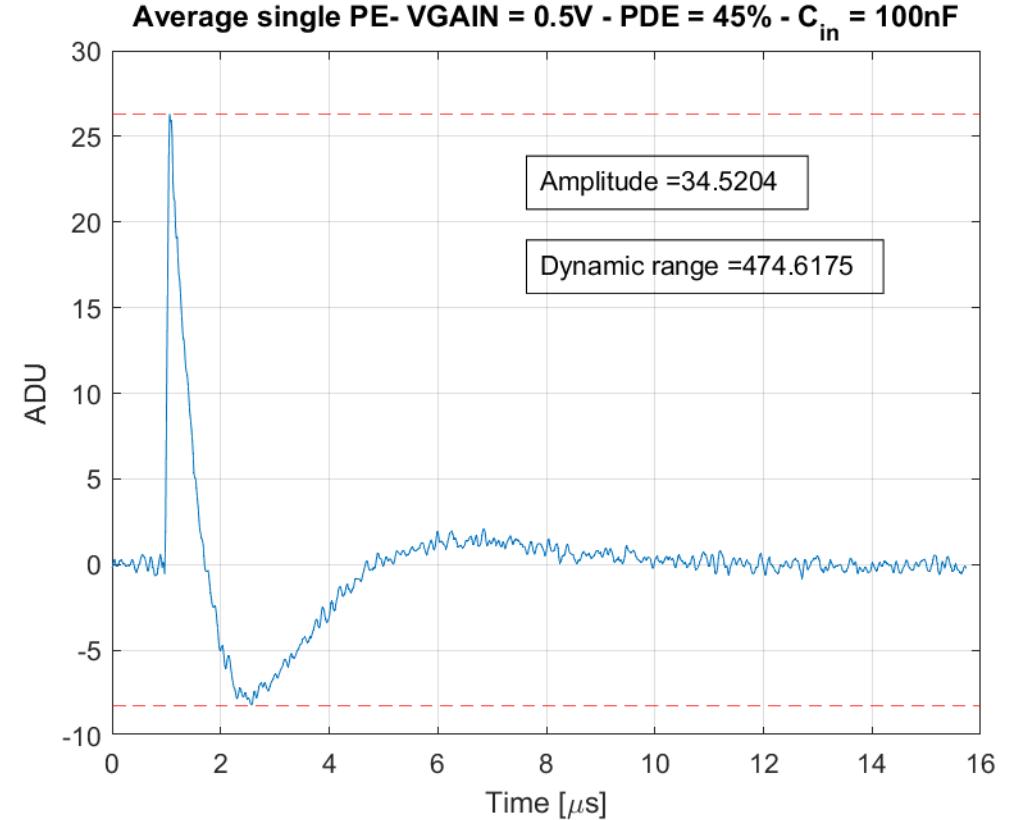
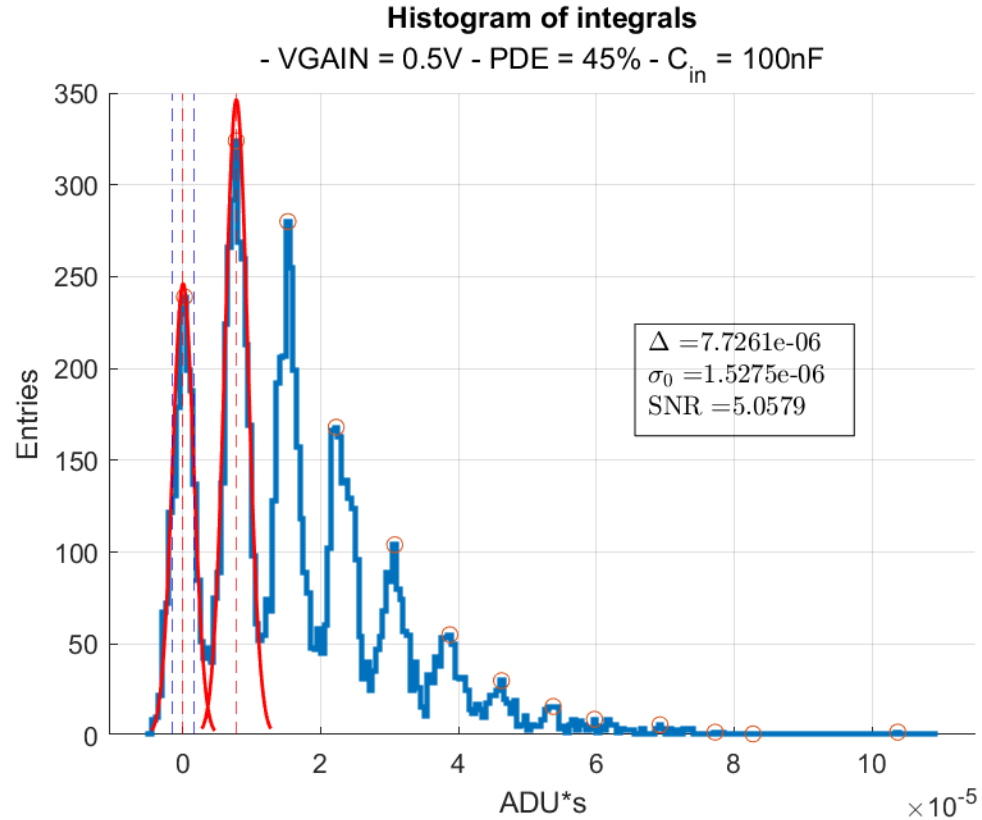
# Cold amplifier testing after applying the patches

PGA integrator ON



# Cold amplifier testing after applying the patches

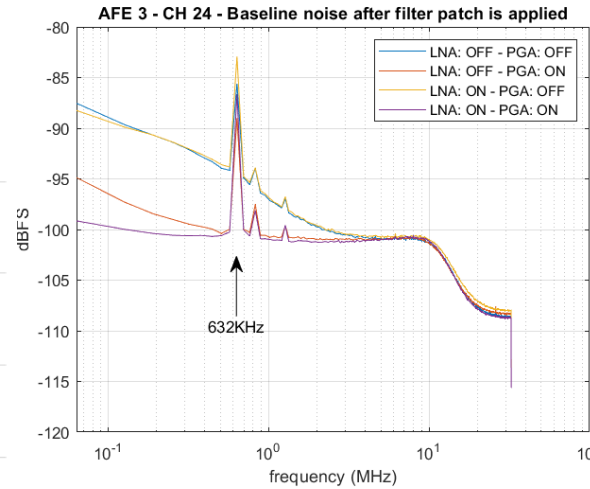
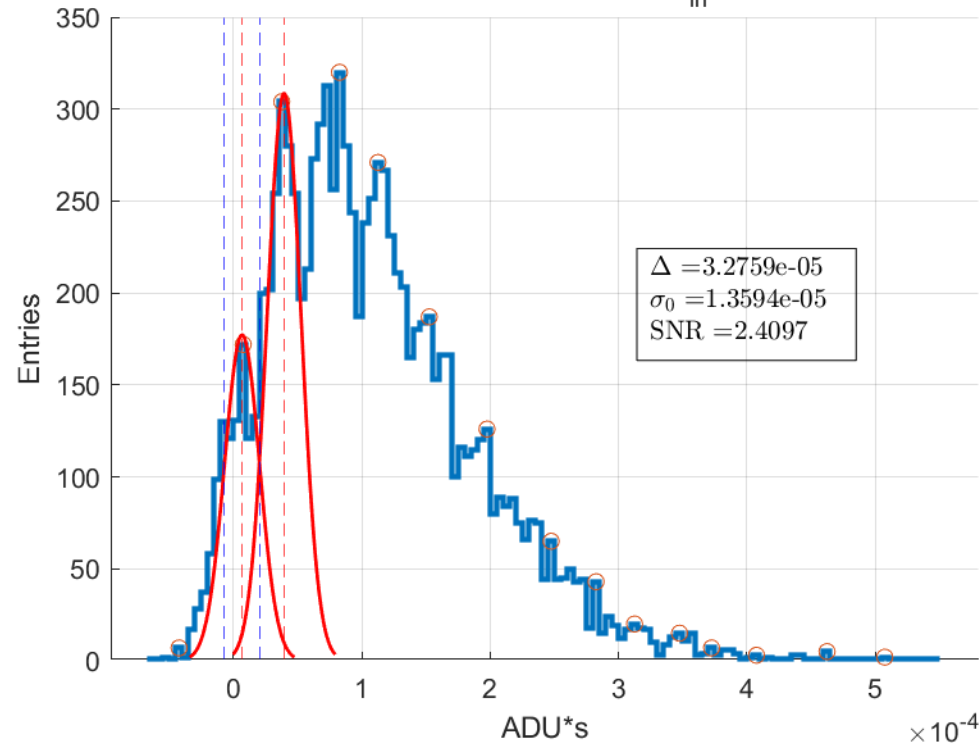
PGA integrator ON



# Cold amplifier testing after applying the patches – Integrators ON-OFF comparison

## PGA integrator OFF

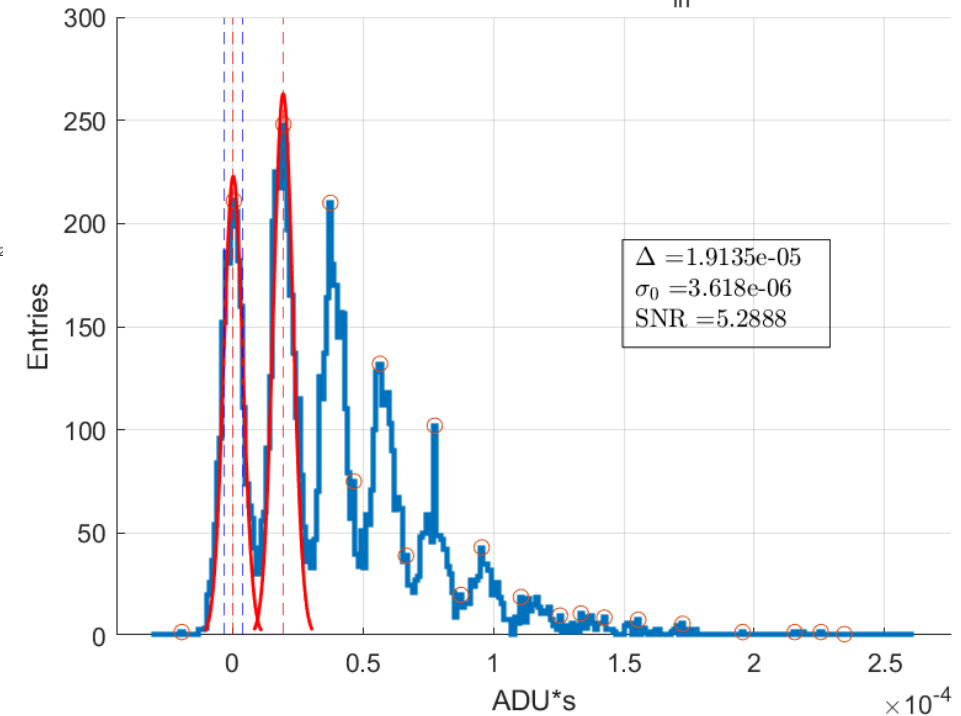
**Histogram of integrals**  
- VGAIN = 0.3V - PDE = 45% -  $C_{in} = 100\text{nF}$



- $\frac{1}{f}$  noise is present when the integrators are off. Possibly this noise originates after the LNA stage (?).
- This noise doesn't allow a stable baseline.

## PGA integrator ON

**Histogram of integrals**  
- VGAIN = 0.3V - PDE = 45% -  $C_{in} = 100\text{nF}$

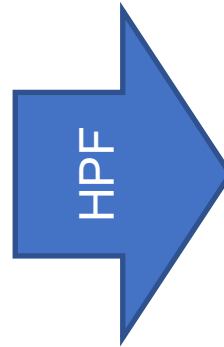
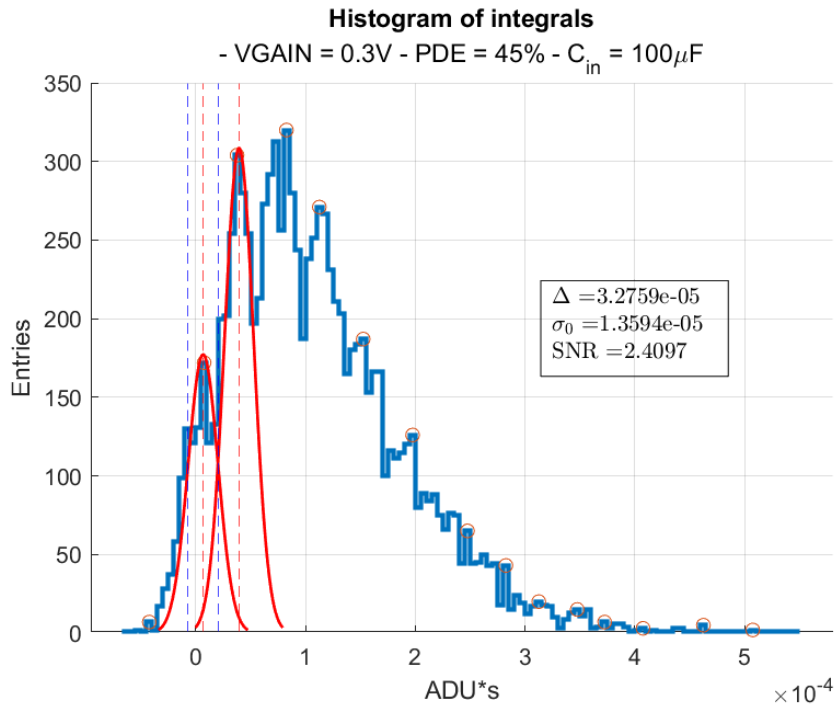




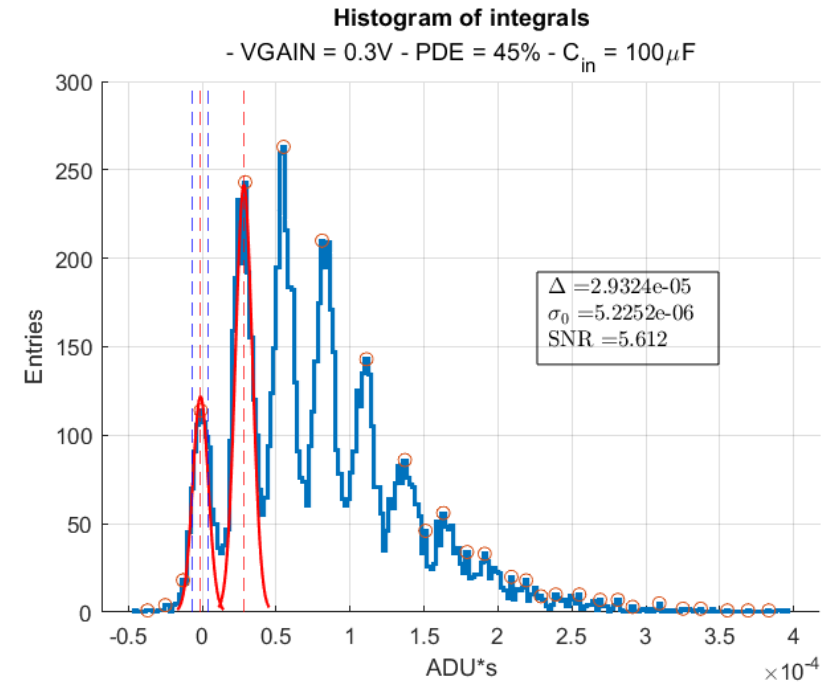
# Cold amplifier testing after applying the patches – Integrators ON-OFF comparison

## PGA integrator OFF

- Applying a first order 80kHz IIR digital Butterworth high pass filter to the data we can deal with the unstable pedestal.



- PGA integrator has a high pass response with cut-off at 80kHz. AFE5808 Datasheet page 42.



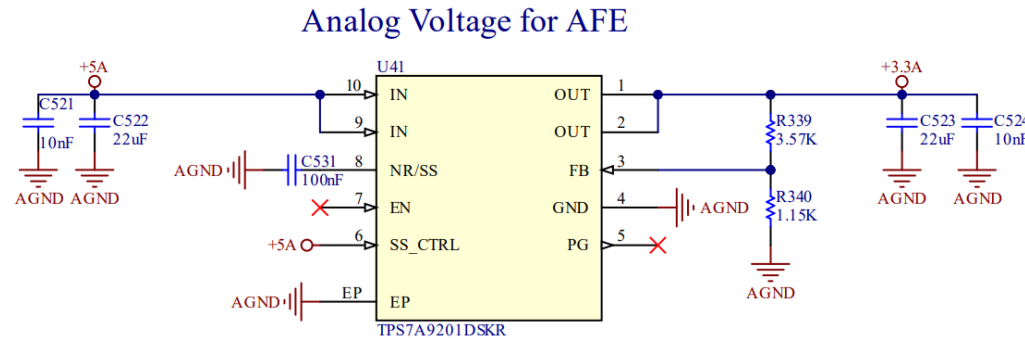
## Summary of tests

SNR		PDE		
VGAIN[V]	Ci [nF]	40 %	45 %	50%
0,3V	10	3,19	4,92	7,09
	100	3,60	5,29	8,67
0,5V	10	2,86	5,12	7,86
	100	4,10	5,06	8,07

## Dynamic Range

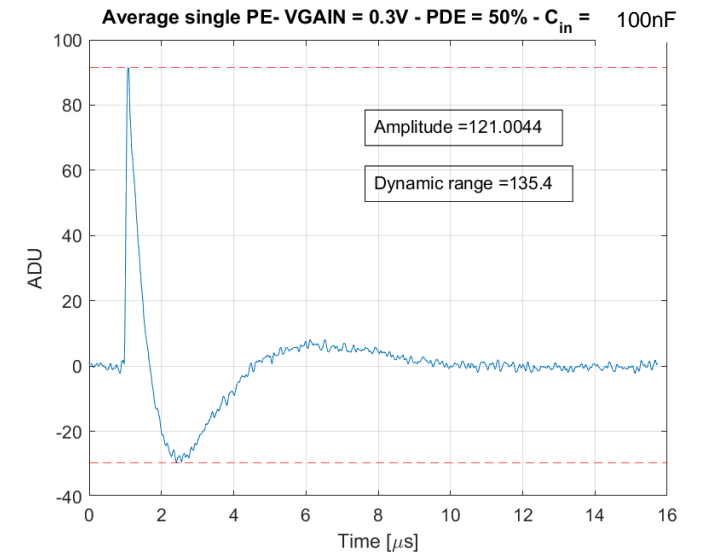
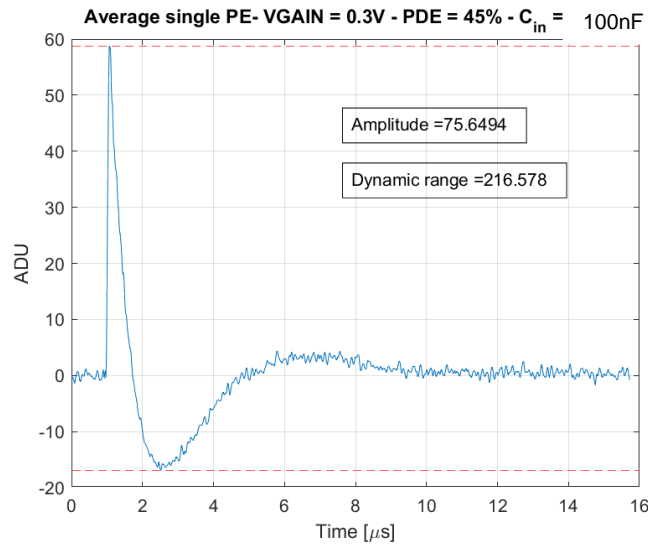
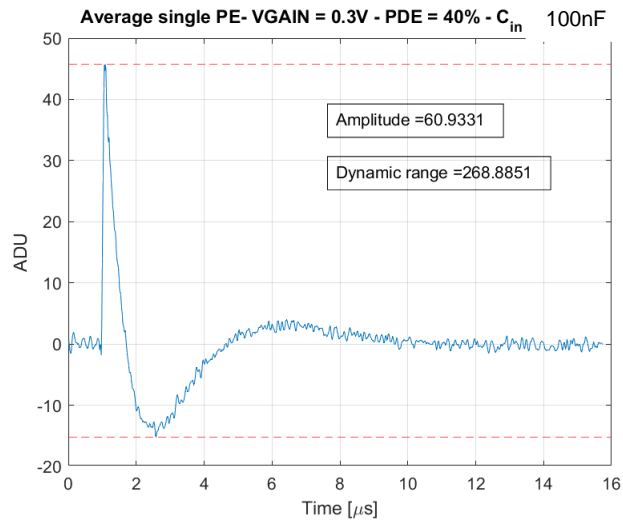
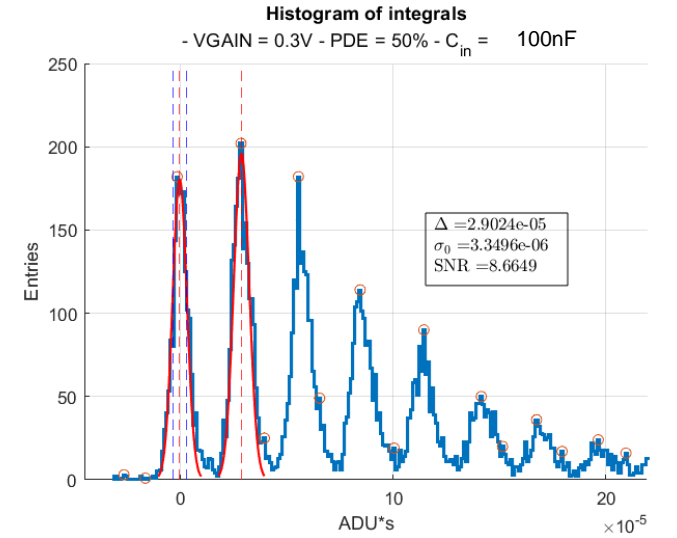
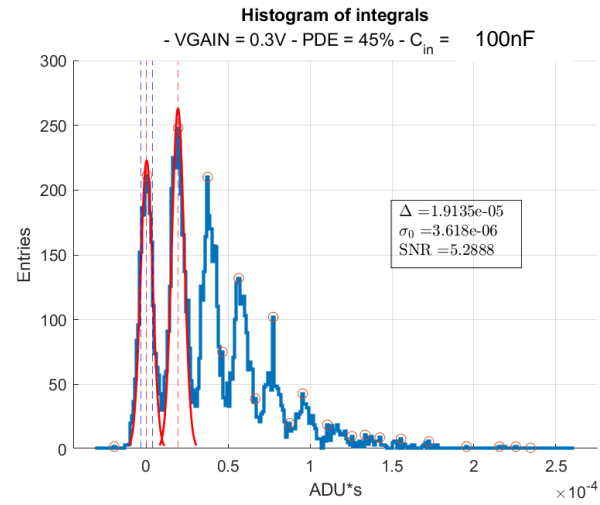
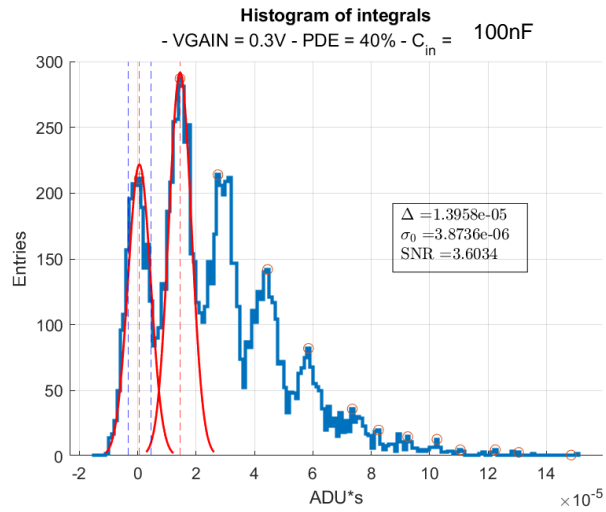
Dynamic Range		PDE		
VGAIN[V]	Ci[nF]	40 %	45 %	50%
0,3V	10	263	204	131
	100	268	216	135
0,5V	10	633	466	295
	100	613	474	313

# DAPHNE was damaged

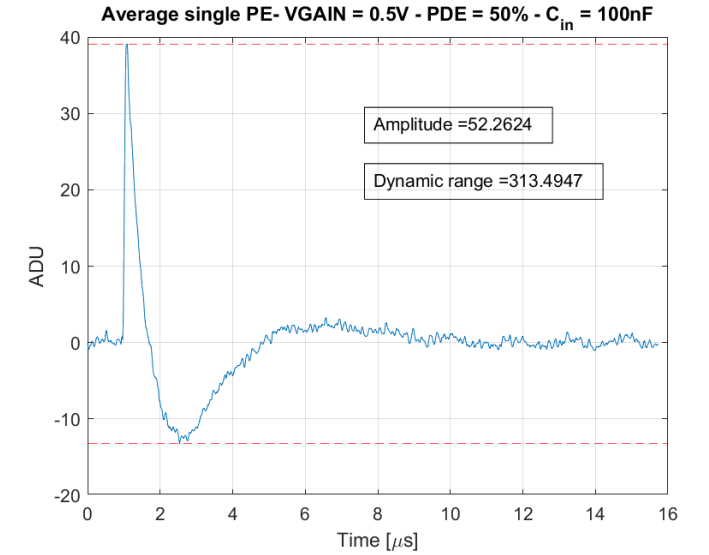
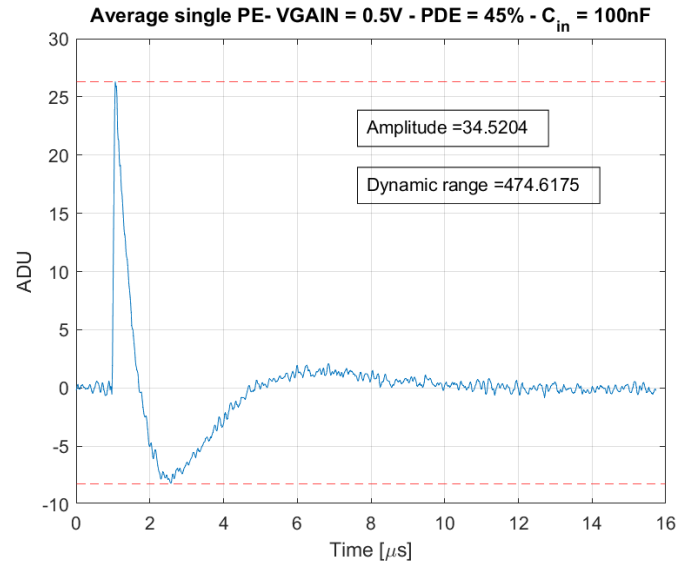
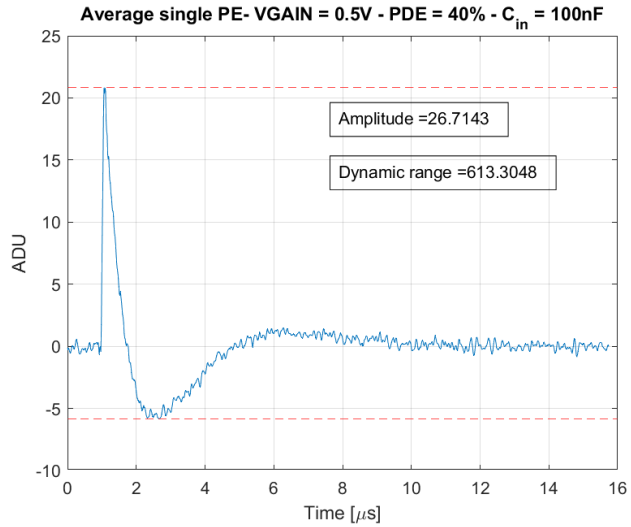
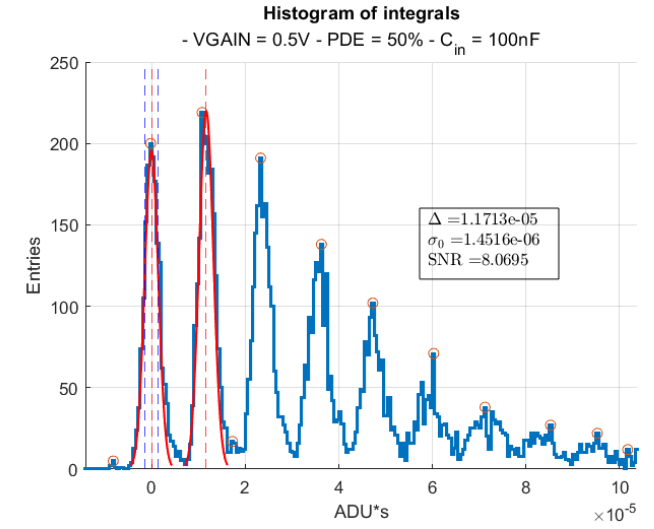
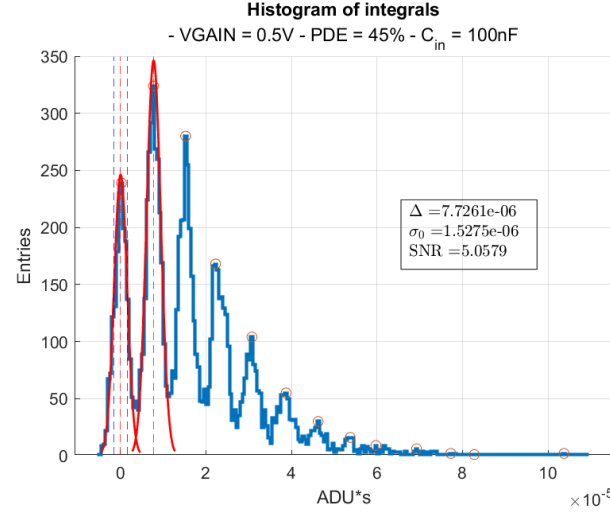
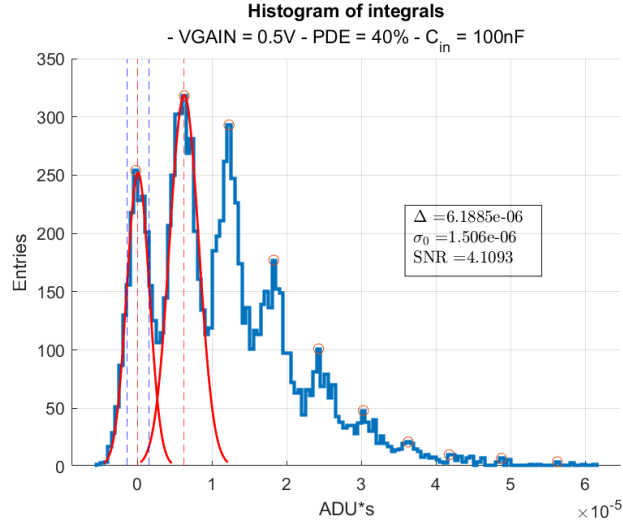


- During the test, I shorted the +5A causing a spike of current that damaged the analog voltage 3,3V regulator.
- The regulator still works, and our DAPHNE is still functional, but is limited. (e.g. disabling the integrators on all AFEs causes the regulator to enter in an unstable operation).
- Looking to buy a spare, we realized that the lead time for this component is 1-2 years.
- One supplier has it in stock, charging ~40US\$ per chip with a 80US\$ shipping rate.

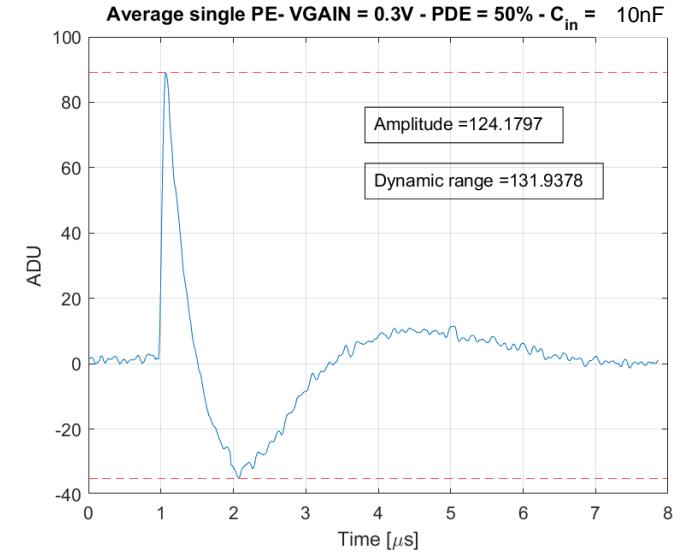
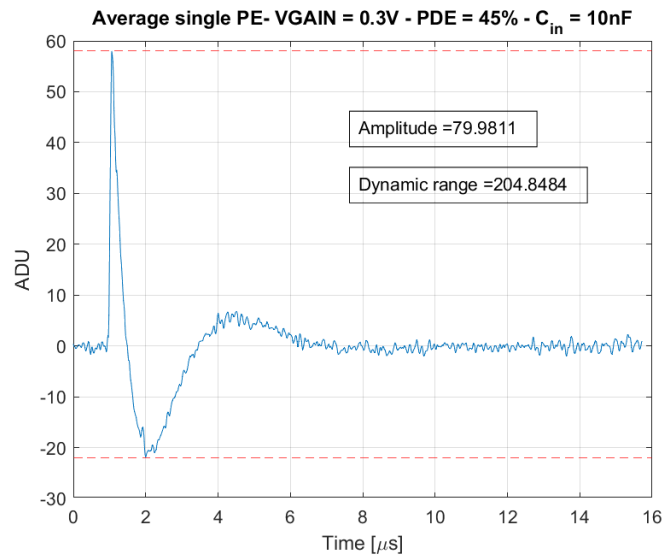
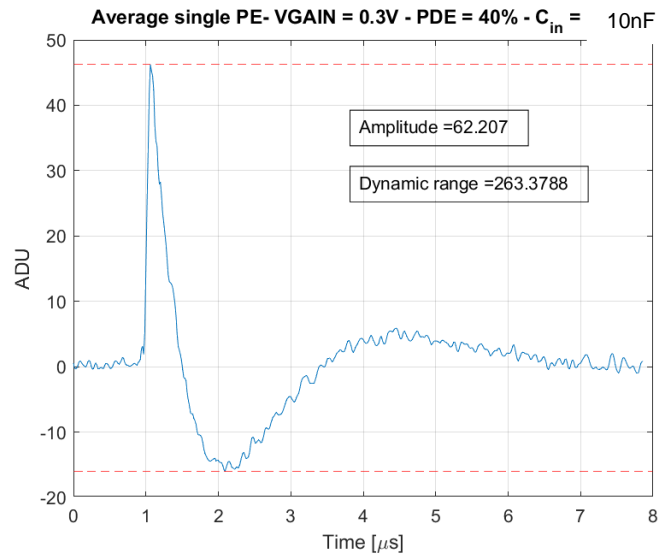
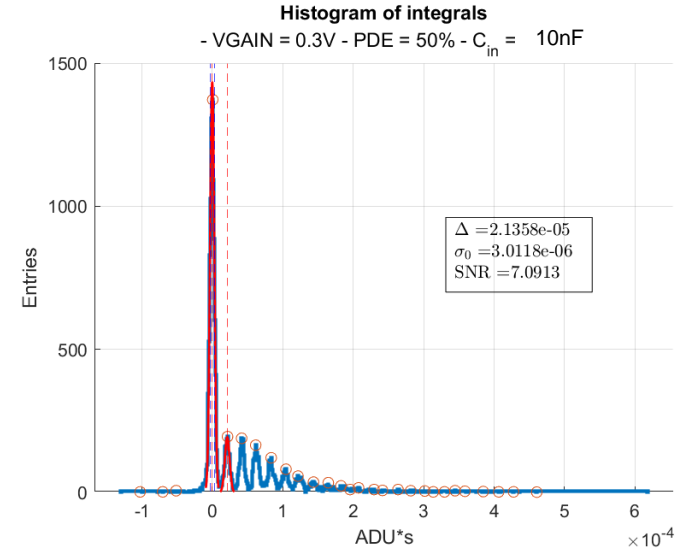
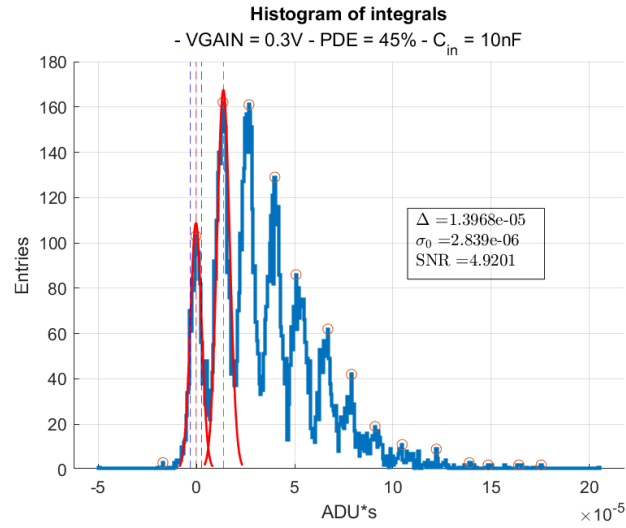
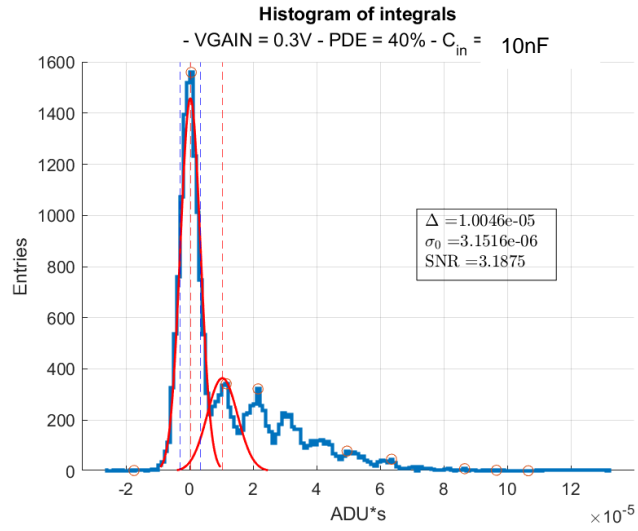
# Miscellaneous



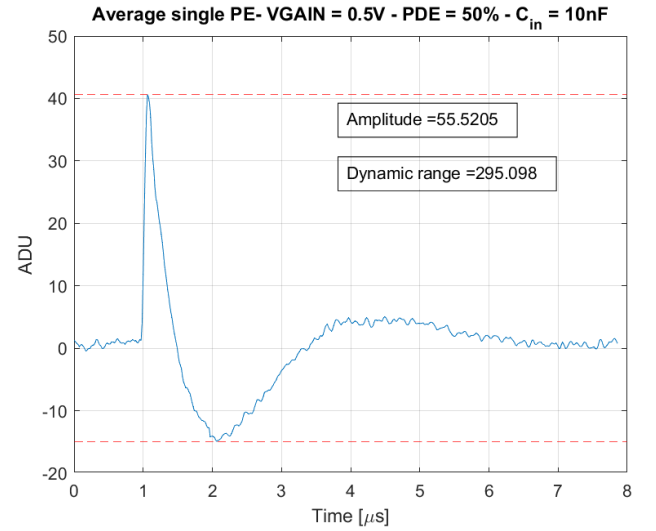
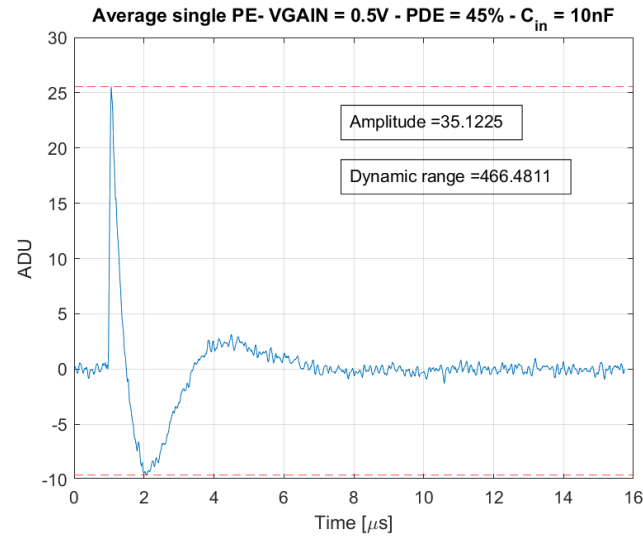
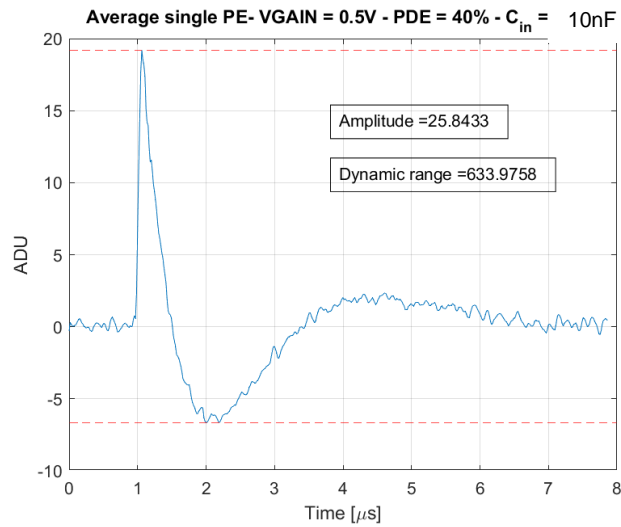
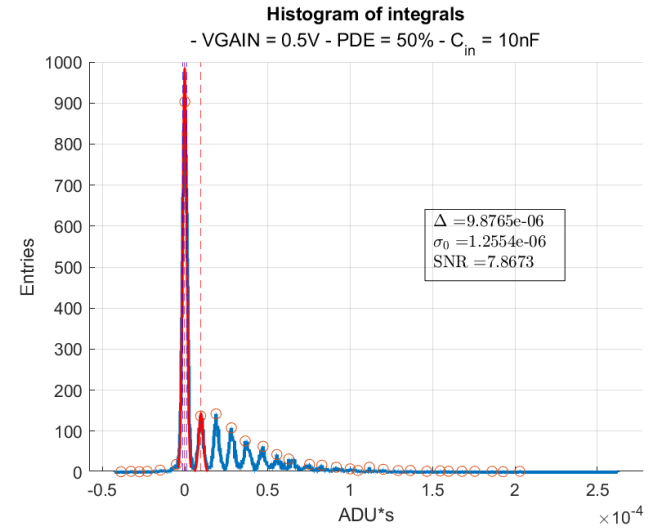
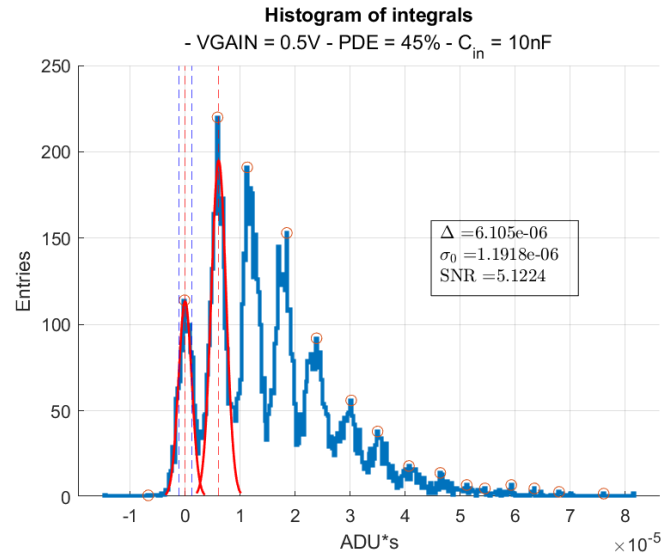
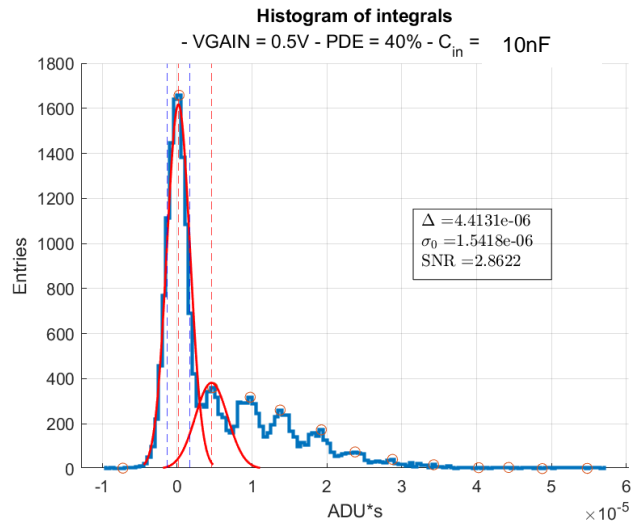
# Miscellaneous



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