DEEP UNDERGROUND NEUTRINO EXPERIMENT

DAPHNE Test at Milano-Bicocca

E. Cristaldo , M. Delgado , C. Gotti , F. Terranova

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UNIVERSITA' DEGLI STUDI DI MILANO BICOCCA

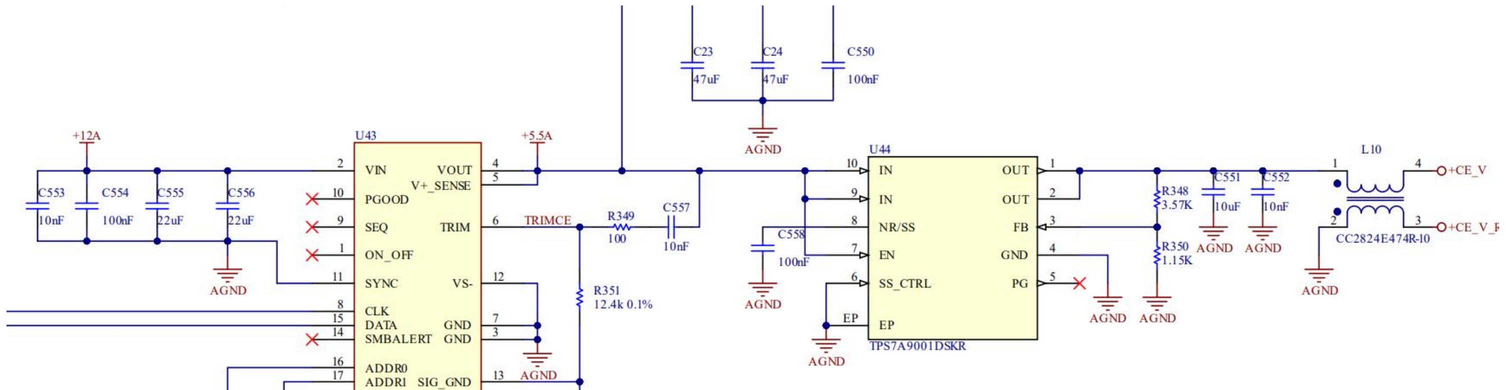
INFN Istituto Nazionale di Fisica Nucleare

DUNE

Introduction

- Quick summary of last presentation.
- VGAIN tests to obtain the best dynamic range.
- Cabling tests.
- Digital Filtering.

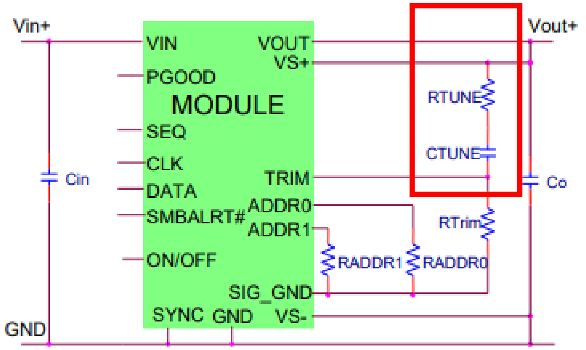
200KHz oscillation at +5,5V rail



Linear Regualtor for Cold Electornics, 500mA
Initially set for +3.3V output
Cold Electronics Adjustable Voltage (+CE_V)
Cold Electronics Adjustable Voltage Return (+CE_V_R)

Applied PATCH

- First, we lowered the output voltage to +5V changing R351 to 2,7KΩ.
- Looking into the datasheet, we found the recommended values for Rtune and Ctune(R349 and C557).
- Changing Rtune from 100Ω to 270 Ω and Ctune from 10nF to 2200pF mitigated the oscillation.



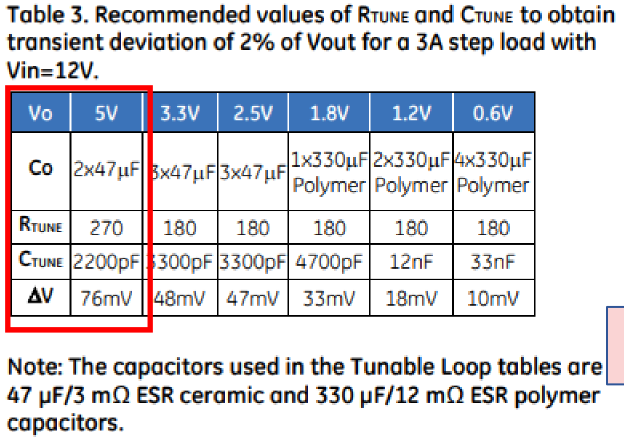
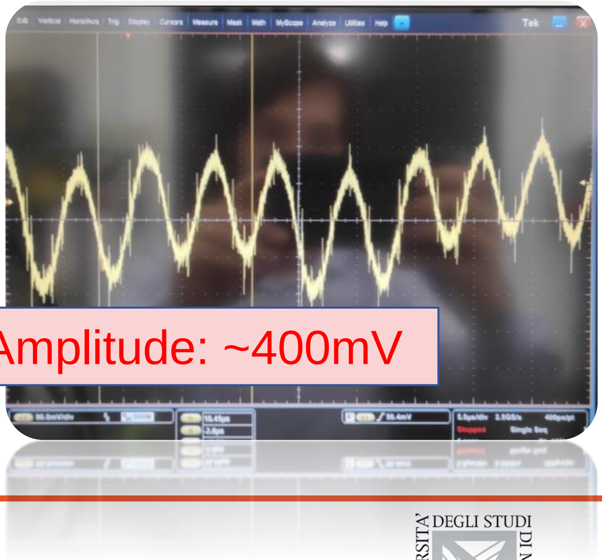


Table 3. Recommended values of RTUNE and CTUNE to obtain transient deviation of 2% of Vout for a 3A step load with Vin=12V.

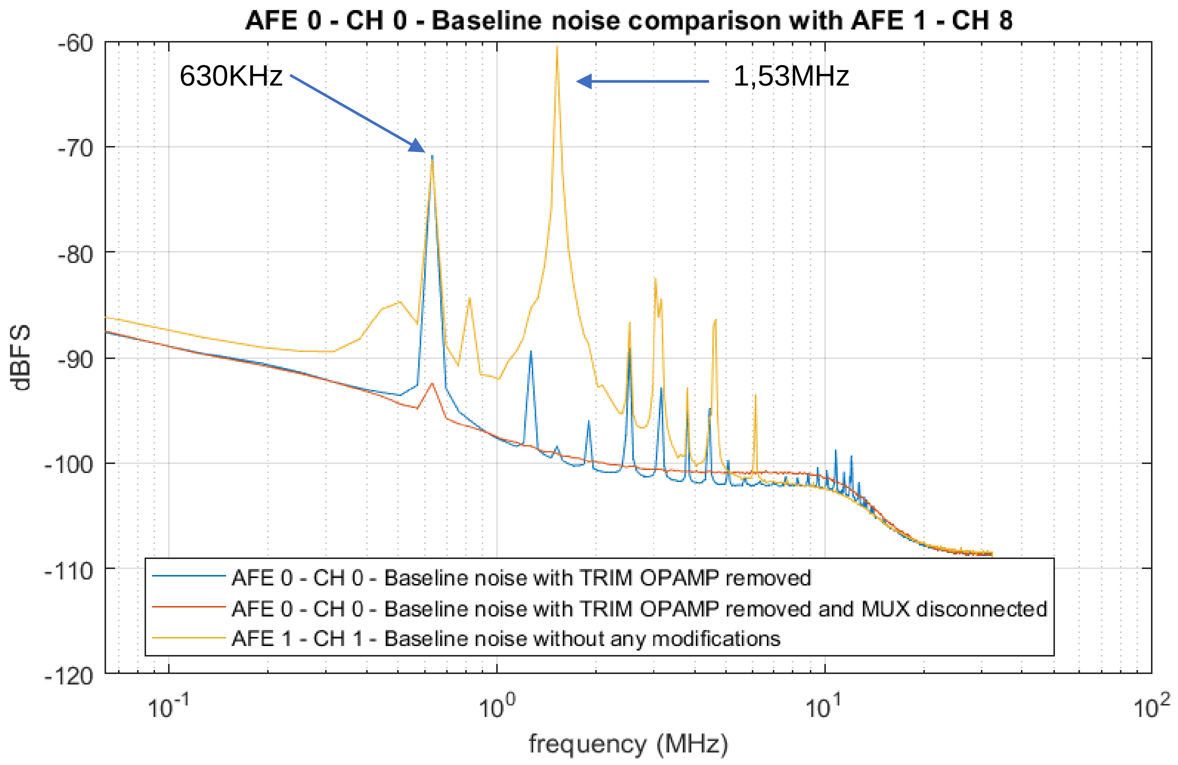
Vo	5V	3.3V	2.5V	1.8V	1.2V	0.6V
Co	2x47μF	3x47μF	3x47μF	1x330μF Polymer	2x330μF Polymer	4x330μF Polymer
RTUNE	270	180	180	180	180	180
CTUNE	2200pF	3300pF	3300pF	4700pF	12nF	33nF
ΔV	76mV	48mV	47mV	33mV	18mV	10mV

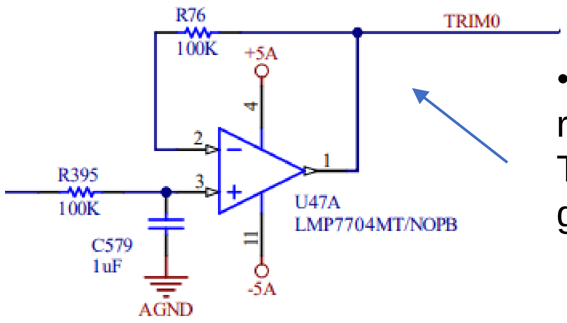
Note: The capacitors used in the Tunable Loop tables are 47 μF/3 mΩ ESR ceramic and 330 μF/12 mΩ ESR polymer capacitors.



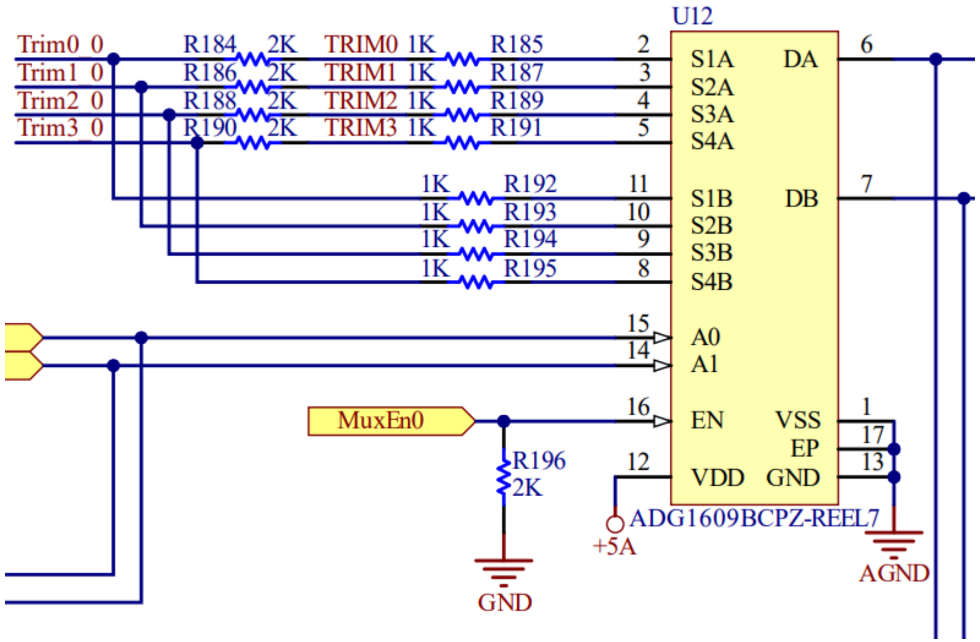
Amplitude: ~400mV

Noise at the AFE inputs





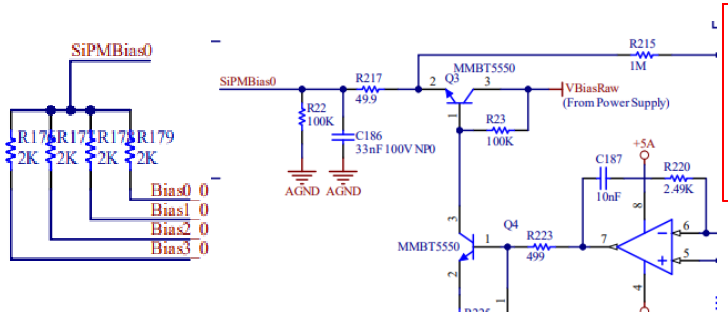
- LMP7704 was removed and TRIM node was grounded.

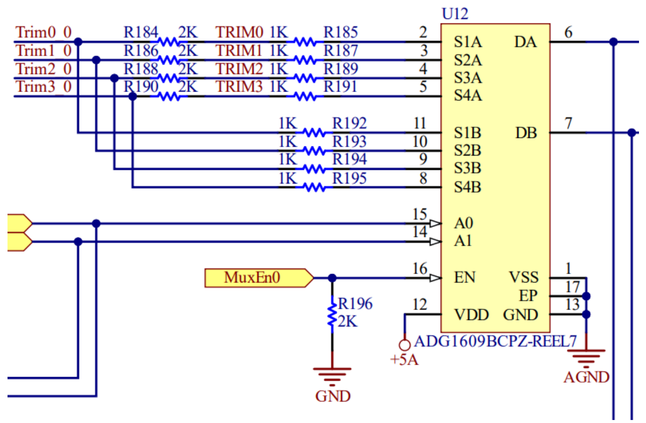


- The noise spectrum in yellow corresponds to the overall noise seen at the AFE input.
- Removing U47 and grounding the TRIM node immediately improves the noise levels, eliminating the 1,53MHz component originating at the -5V rail.
- Removing R192 from U12 eliminates the 630KHz component.

Patches applied to recover TRIM and Current Monitoring systems

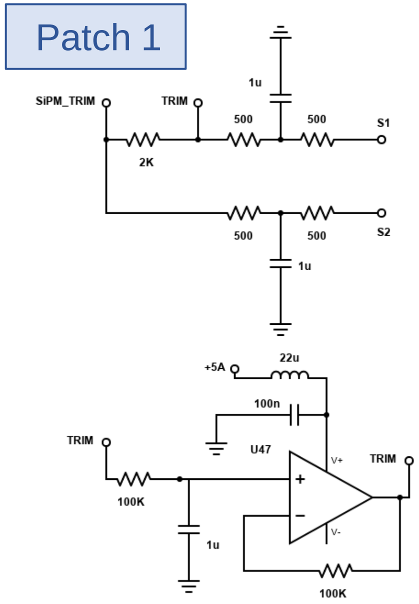
- Three different patch have been applied in successive ordering. Each one of them trying to to minimize the number of modifications and components needed.



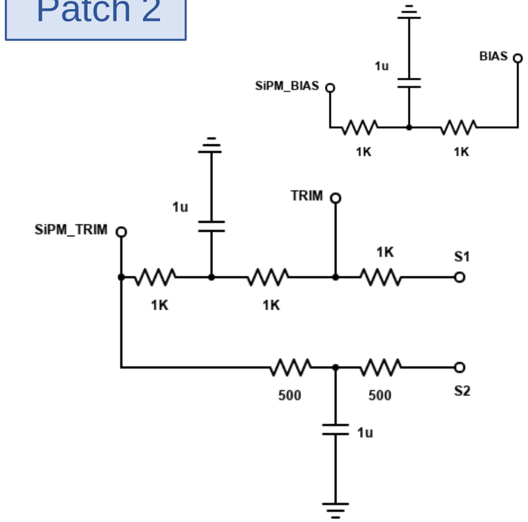


- To filter better the SiPM bias, R217 value was changed to 1K and C186 was changed to 1u.
- This bias patch is included in (1) and (3)
- Patch (2) splits the 2K resistor (R179) to form a filter with a 1u capacitor.

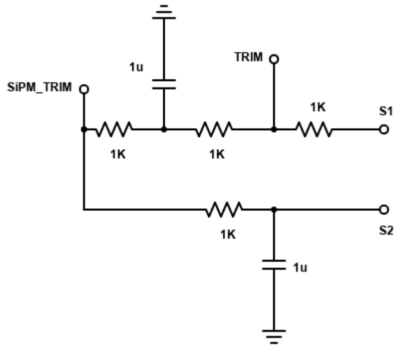
Patch 1



Patch 2

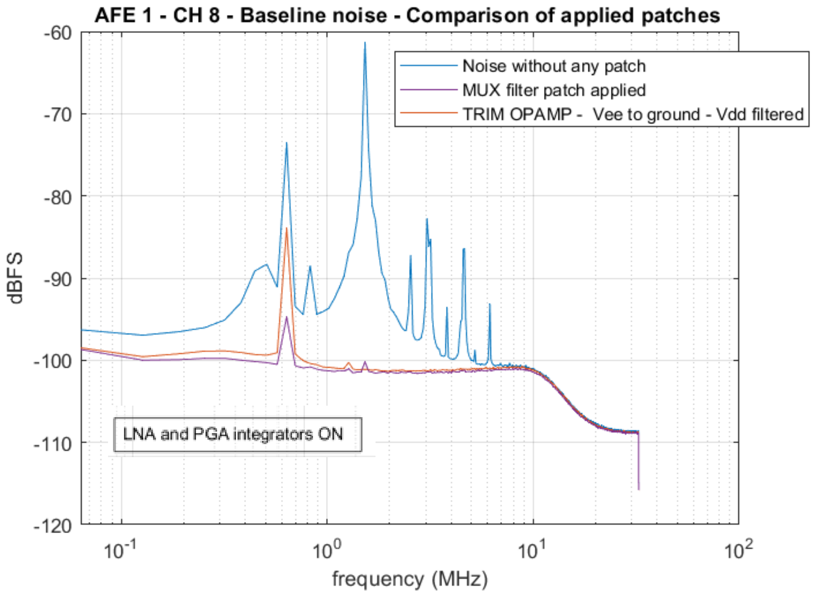


Patch 3

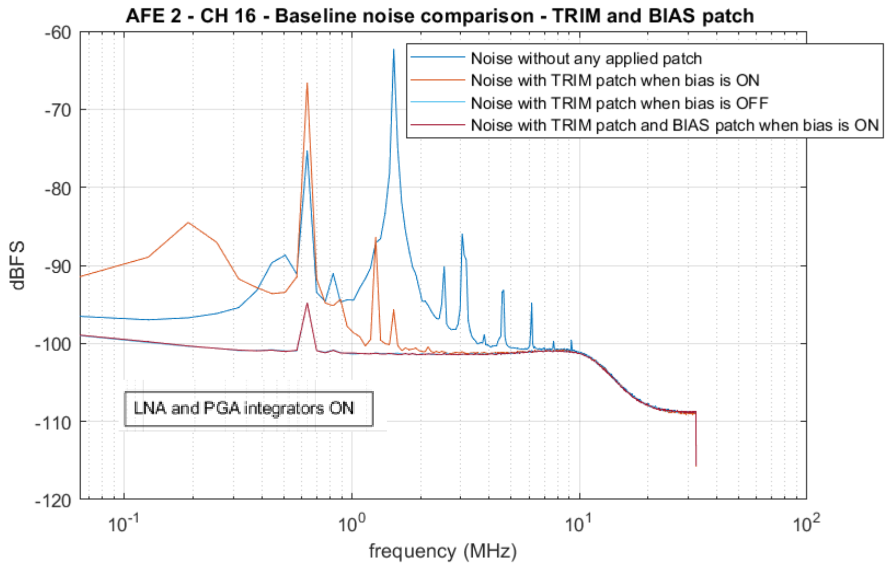


Patches applied to recover TRIM and Current Monitoring systems

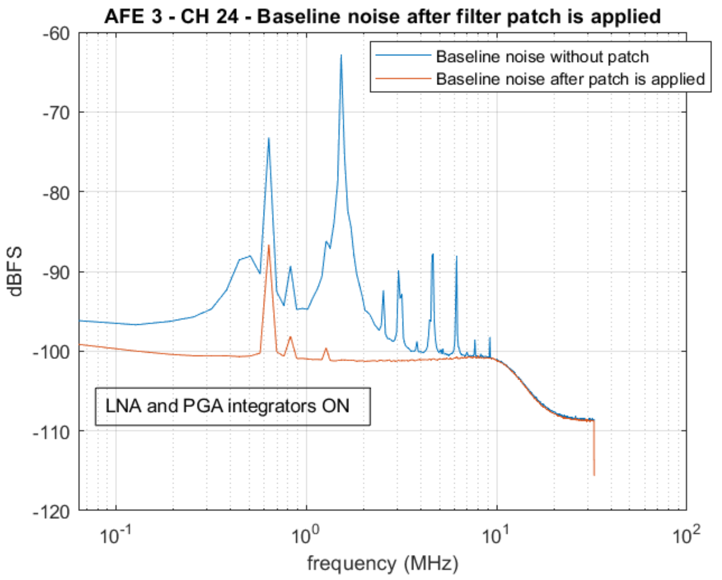
Patch 1



Patch 2

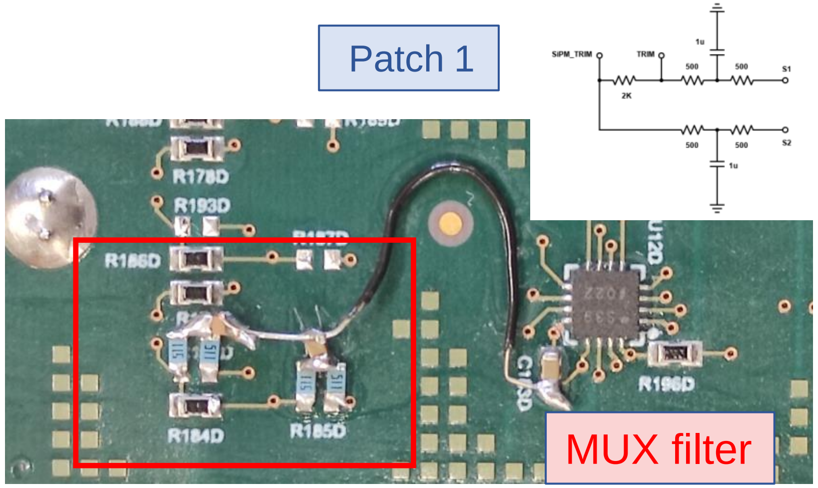


Patch 3

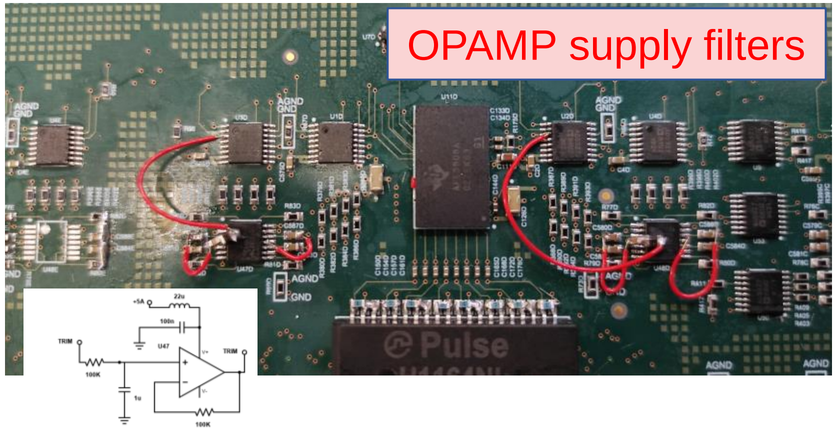


Patches applied to recover TRIM and Current Monitoring systems

Patch 1

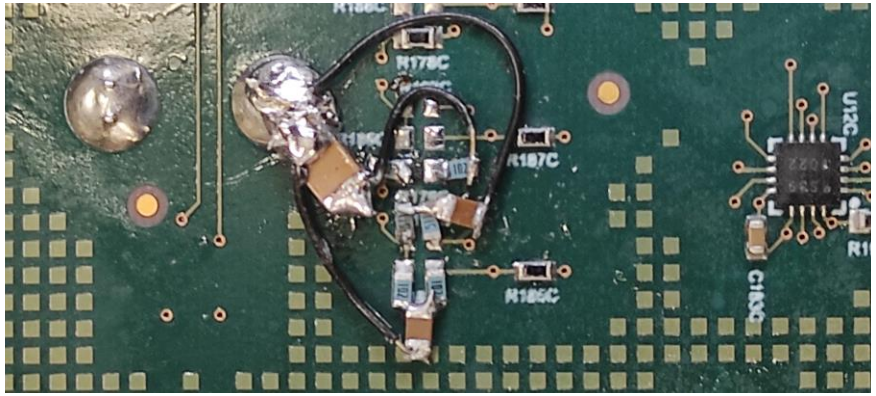


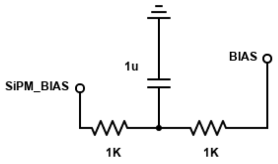
MUX filter

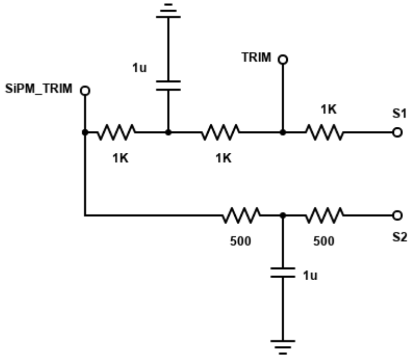


OPAMP supply filters

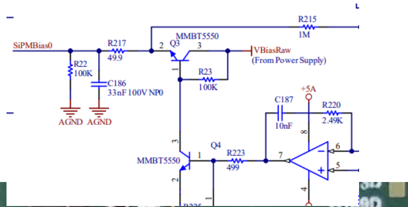
Patch 2

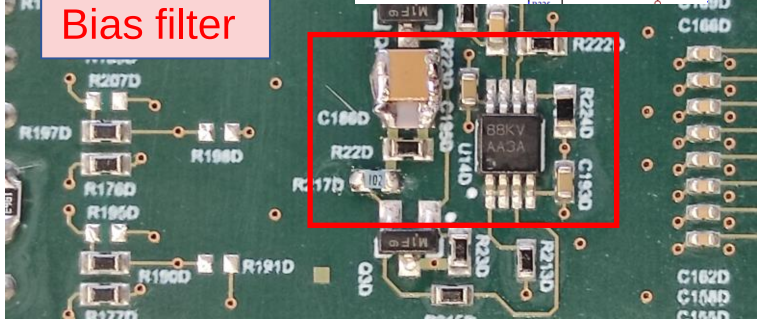




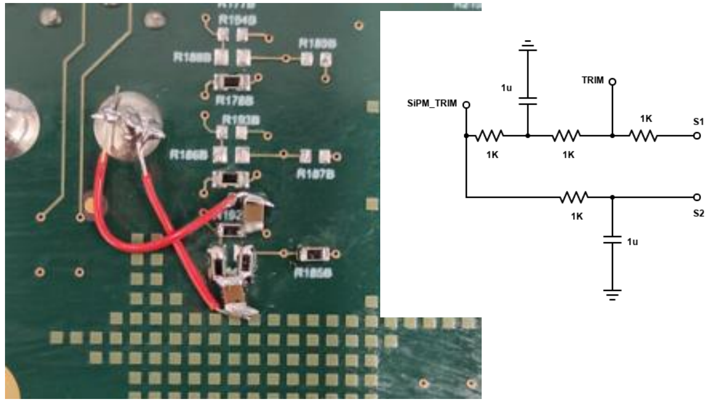


Patch 3

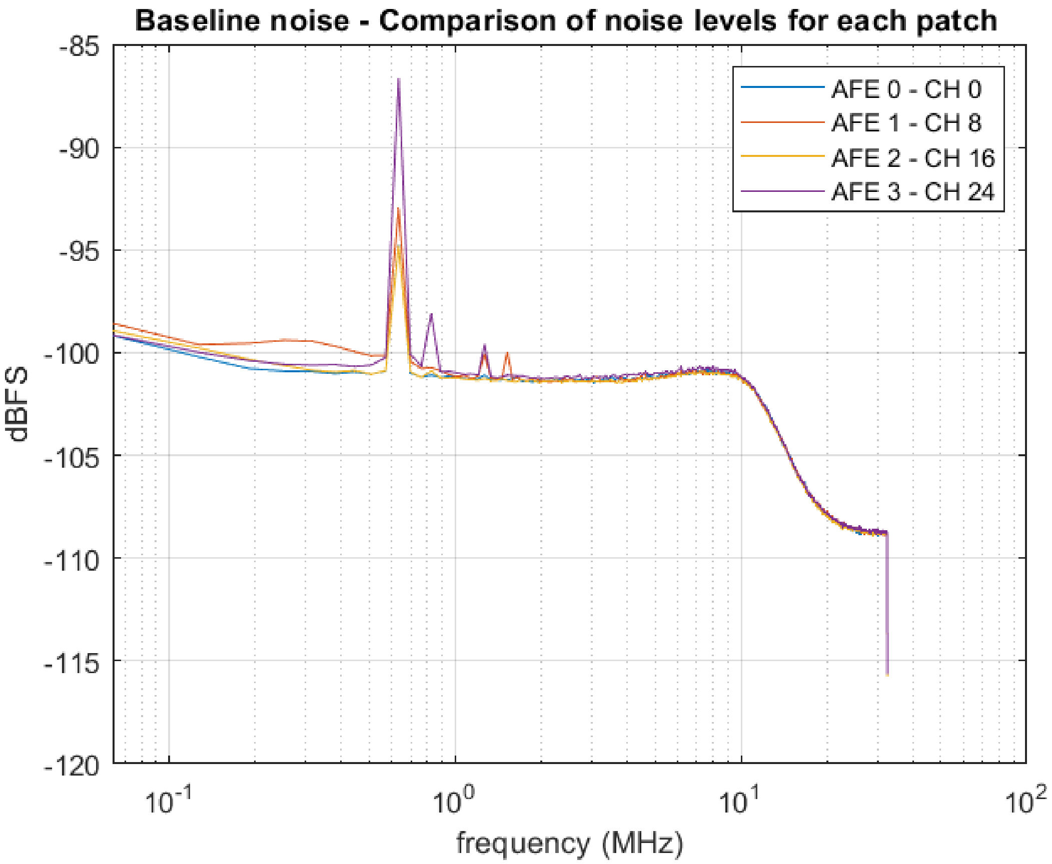


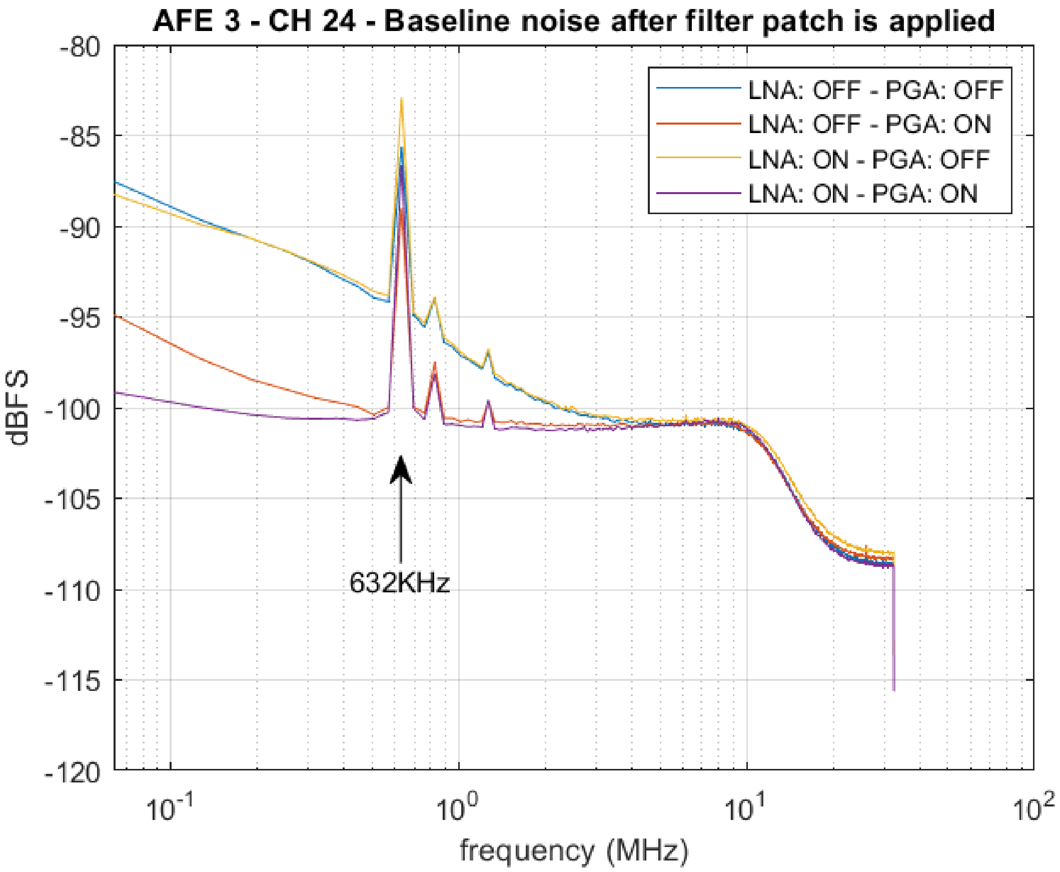


Bias filter



Result and comparison with integrators

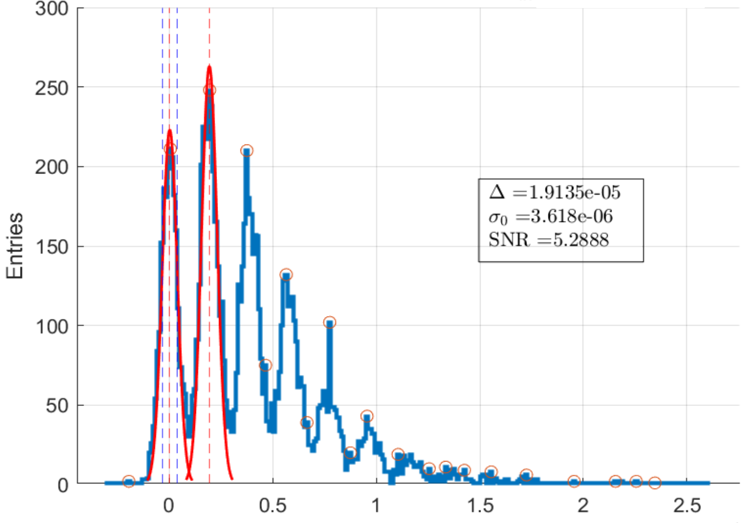

Baseline noise - Comparison of noise levels for each patch


AFE 3 - CH 24 - Baseline noise after filter patch is applied

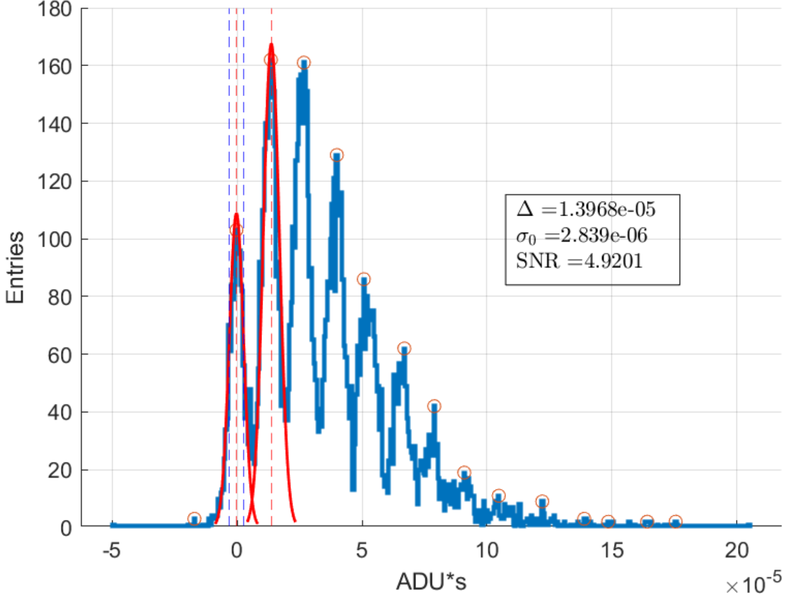
Cold amplifier testing after applying the patches

PGA integrator ON

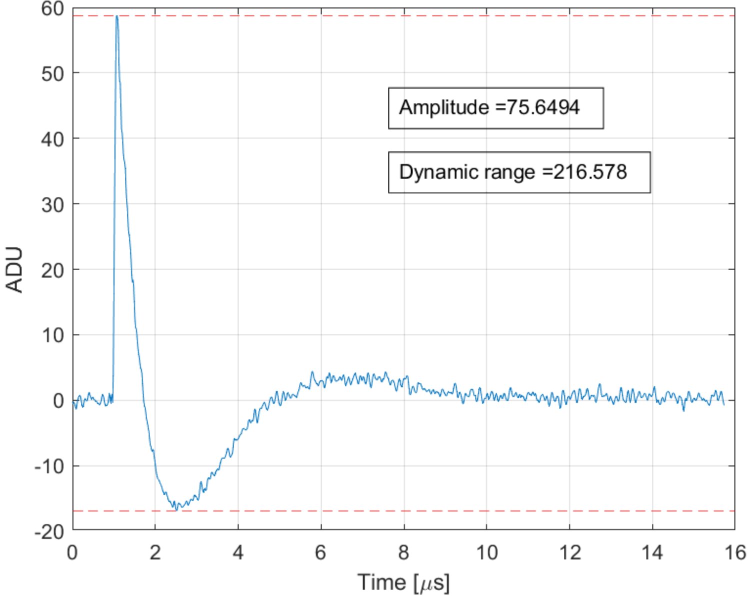
Histogram of integrals
- VGAIN = 0.3V - PDE = 45% - C_{in} 100nF



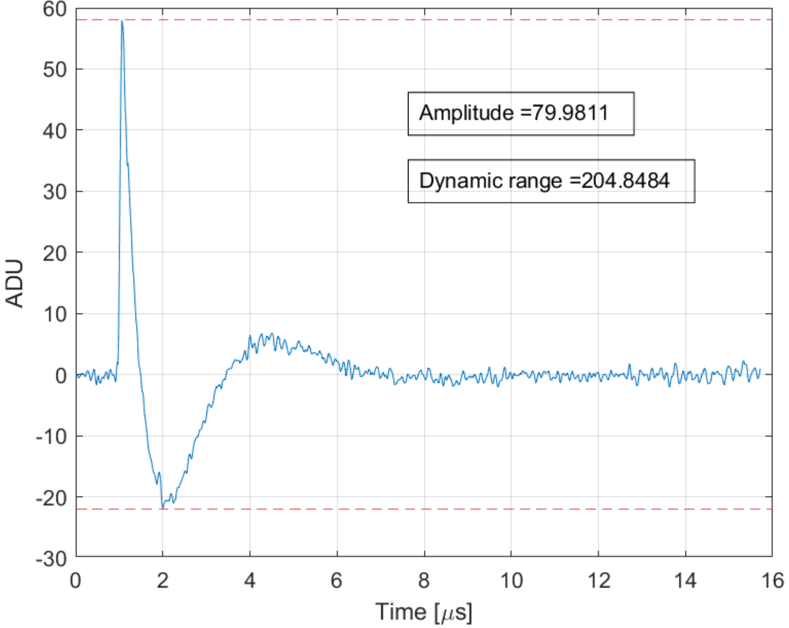
Histogram of integrals
- VGAIN = 0.3V - PDE = 45% - C_{in} = 10nF



Average single PE- VGAIN = 0.3V - PDE = 45% - C_{in} = 100nF



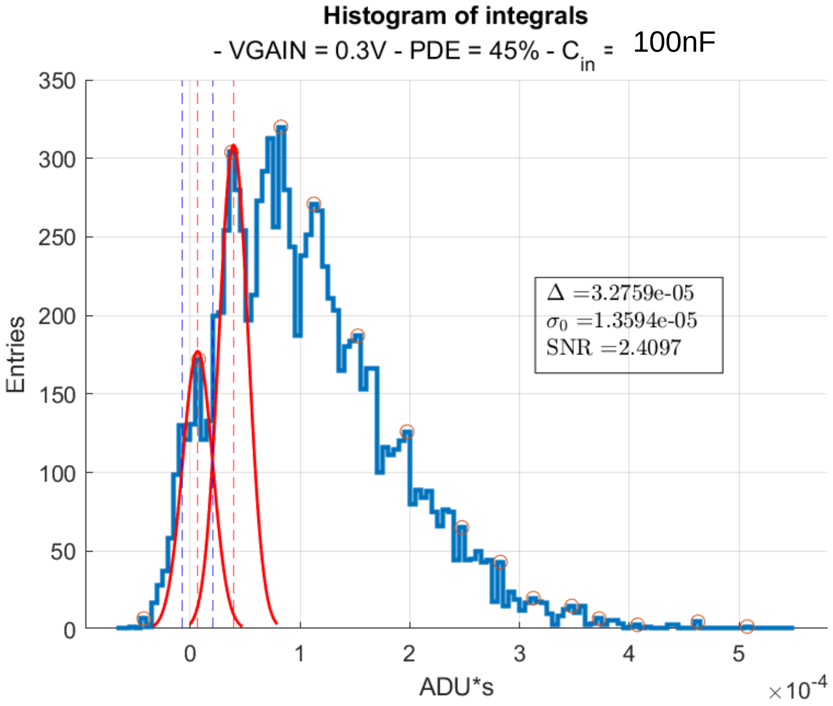
Average single PE- VGAIN = 0.3V - PDE = 45% - C_{in} = 10nF

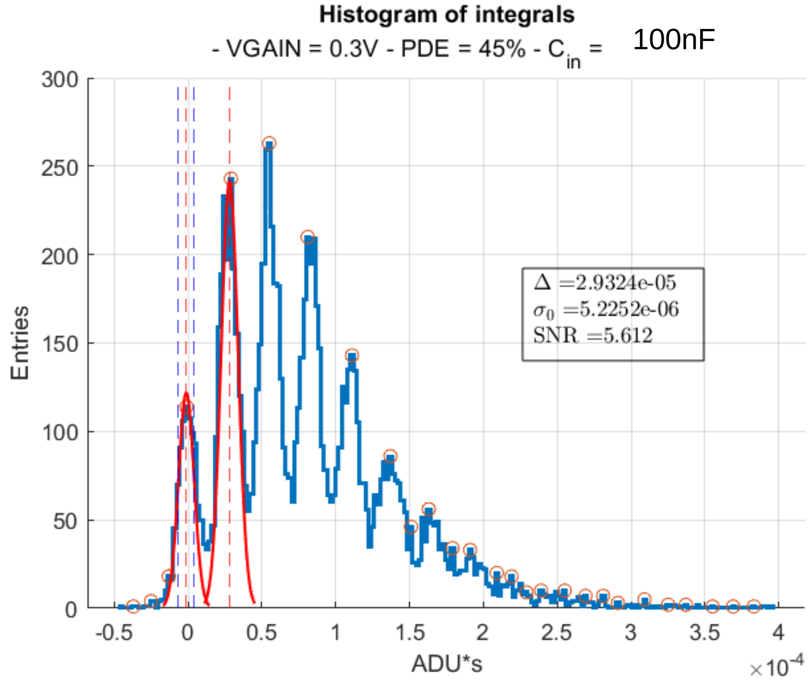


Cold amplifier testing after applying the patches – Integrators ON-OFF comparison

PGA integrator OFF

- Applying a first order 80kHz IIR digital Butterworth high pass filter to the data we can deal with the unstable pedestal.





- PGA integrator has a high pass response with cut-off at 80kHz. AFE5808 Datasheet page 42.

Summary of tests

SNR

		PDE		
VGAIN[V]	**Ci [nF]**	**40 %**	**45 %**	**50%**
0,3V	10	3,19	4,92	7,09
	100	3,60	5,29	8,67
0,5V	10	2,86	5,12	7,86
	100	4,10	5,06	8,07

Dynamic Range

		PDE		
VGAIN[V]	**Ci[nF]**	**40 %**	**45 %**	**50%**
0,3V	10	263	204	131
	100	268	216	135
0,5V	10	633	466	295
	100	613	474	313

End of Summary

VGAIN to obtain the required dynamic range

- To obtain the required VGAIN (Cin = 100nF) to achieve a dynamic range of 2000 P.E., we proceeded as follows:
  1. For a PDE configuration, in this case 45%, we took the measured value at a high VGAIN configuration (0,3V). From the previous slide this value is 216.
  2. With this value, we find that the average single P.E. is

$$A_{1P.E.(0,3V)} = \frac{2^{14}}{216} \approx 76\ ADU$$

     For VGAIN = 0,3V (27,39dB)(23,4).

  3. Then, the target amplitude for a single P.E. to obtain 2000 P.E. dynamic range is

$$A_{2000P.E.DR} = \frac{2^{14}}{2000} \approx 8\ ADU$$

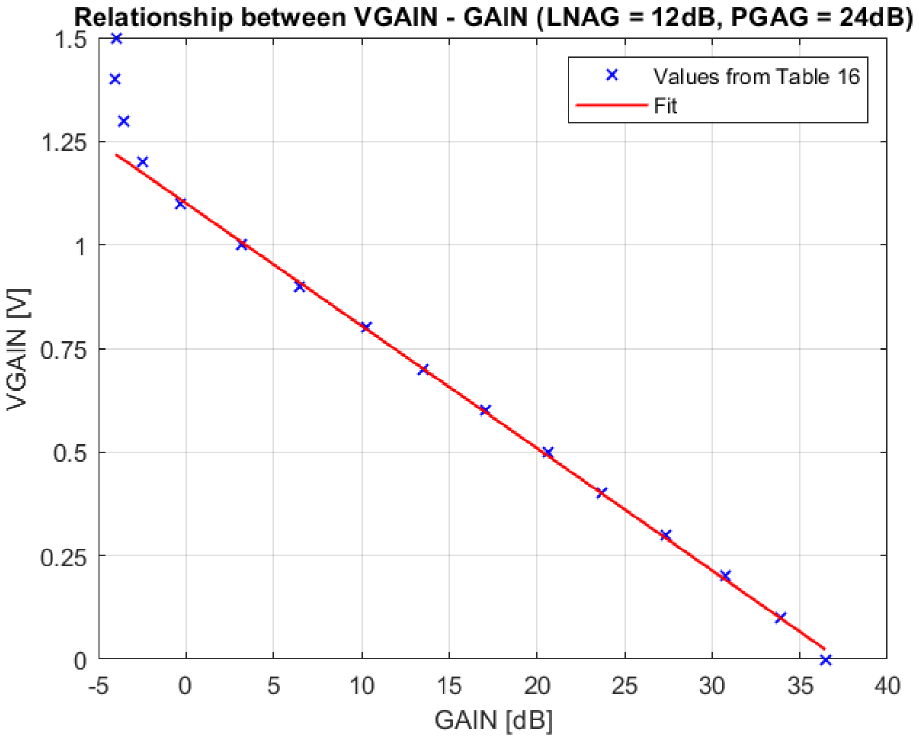
  4. Then, the desired GAIN to obtain a single P.E. of amplitude 8 ADU is

$$G_{1P.E.\,(8ADU)} = \frac{A_{2000P.E.DR} * G_{0,3V}}{A_{1P.E.(0,3V)}} \approx \frac{8 * 23{,}6}{76} \approx 2{,}48(7{,}89\text{dB})$$

- These GAIN values are referenced to table 16 (AFE5808 datasheet page 57), for the specific configuration (LNAG = 12dB, PGAG = 24dB).

VGAIN to obtain the required dynamic range

- Taking the values of GAIN of table 16 at the given configuration, we made a fit to extract the VGAIN value for the desired GAIN = 7,89dB, calculated previously.

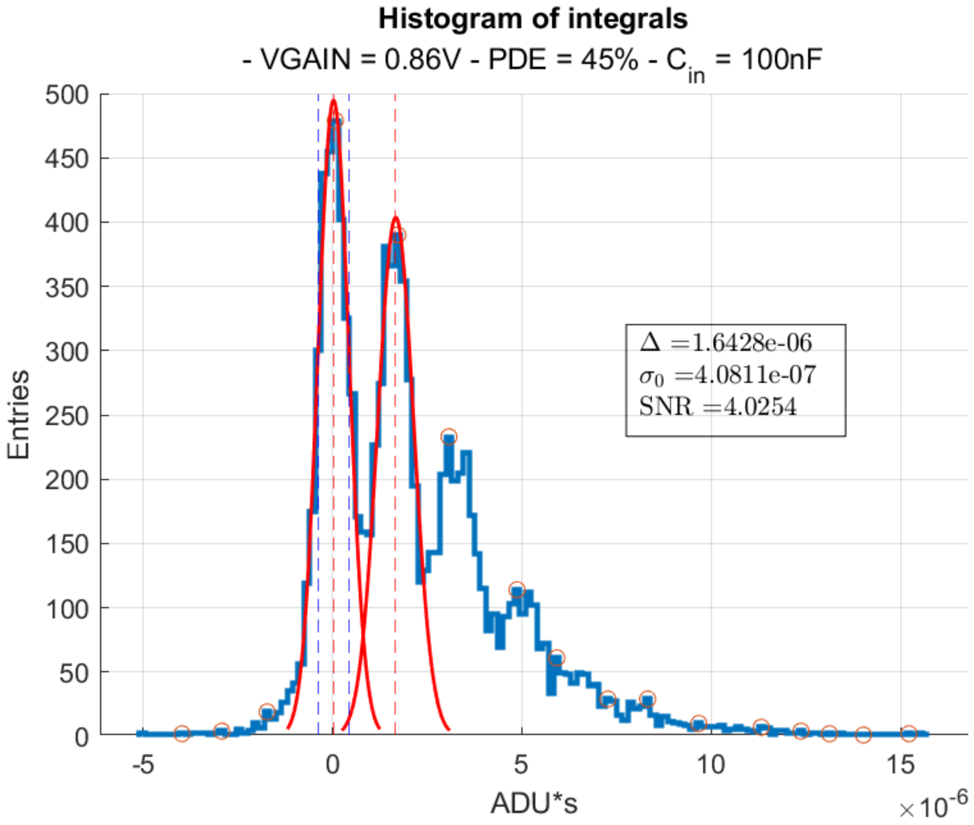


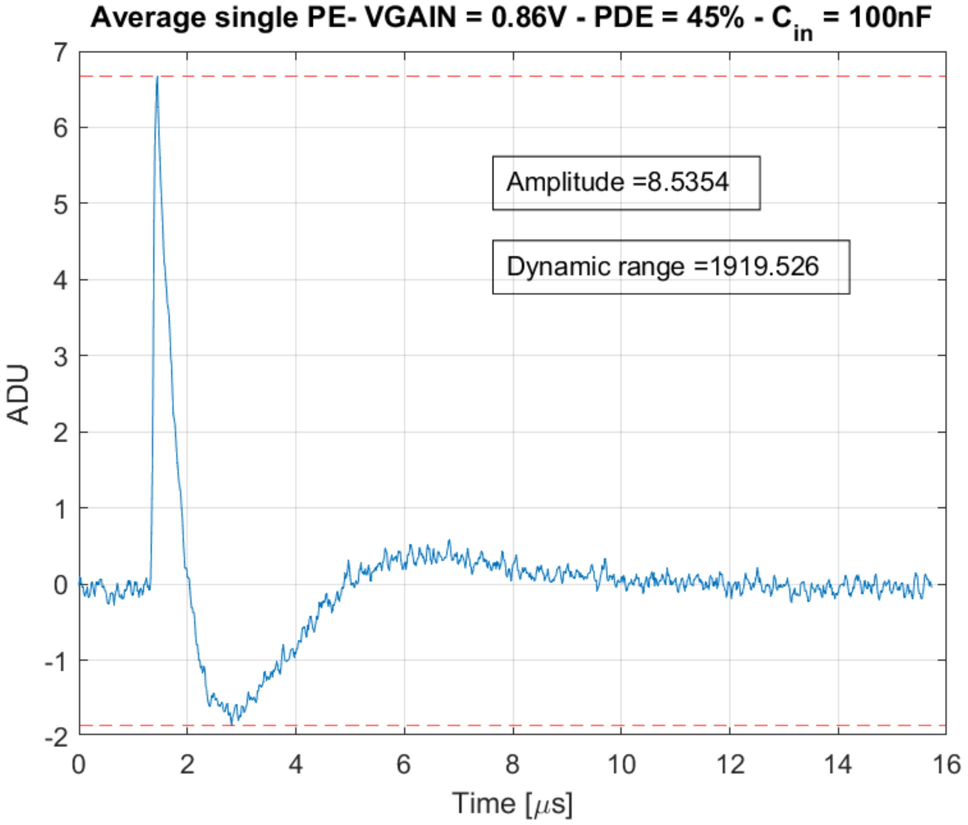
$$VGAIN_{1P.E.(8ADU)} = Fit(7{,}89dB) \approx 0{,}86V$$

VGAIN to obtain the required dynamic range

VGAIN = 0,86V

integrators ON*



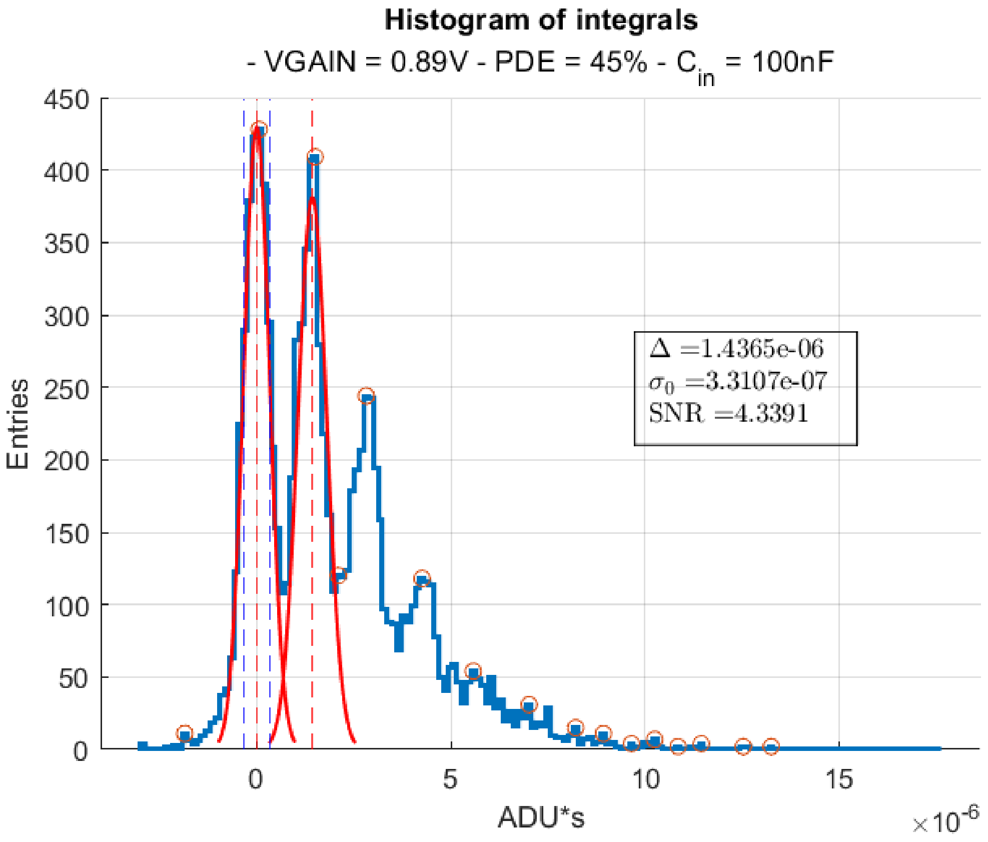


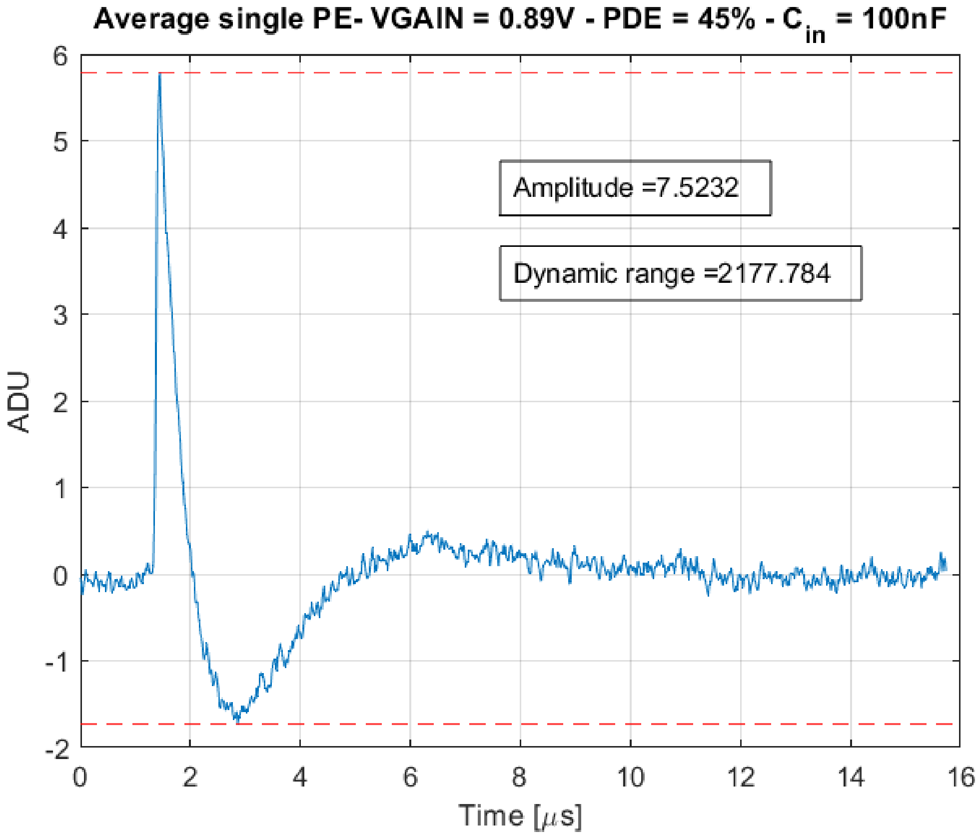
* Only half of the dynamic range specified is usable with the integrators ON.

VGAIN to obtain the required dynamic range

integrators ON*

VGAIN = 0,89V



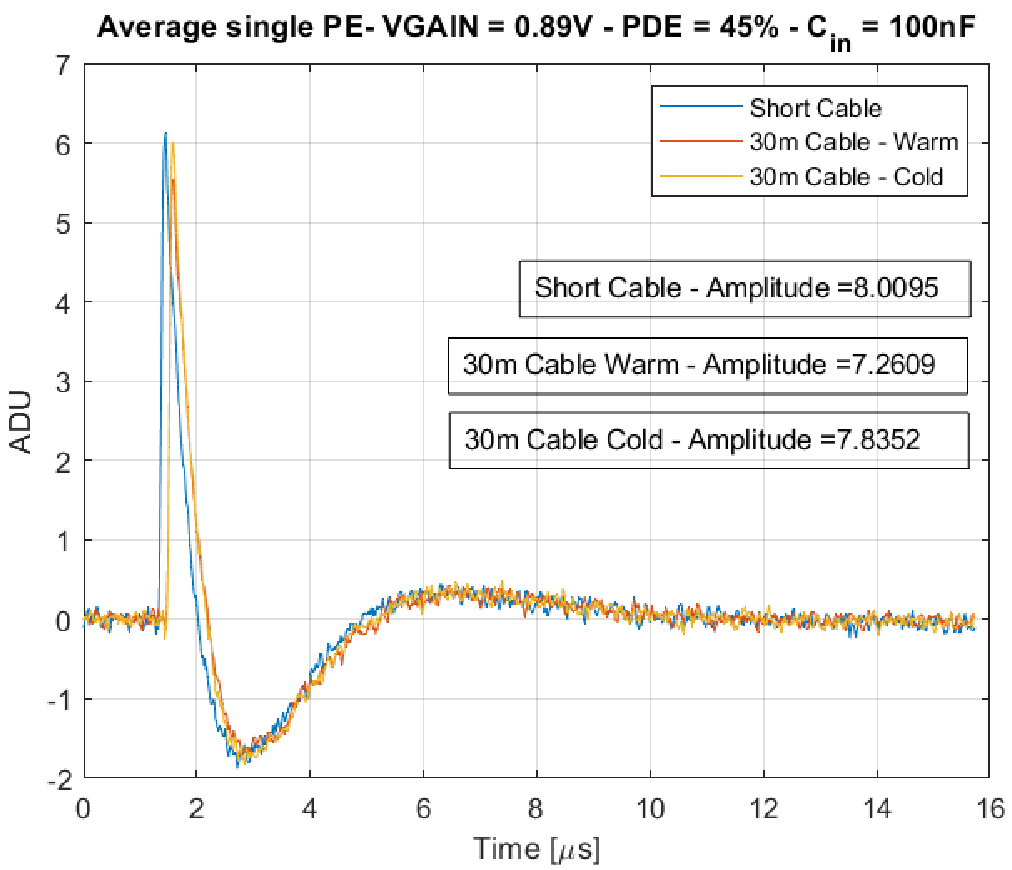


* Only half of the dynamic range specified is usable with the integrators ON.

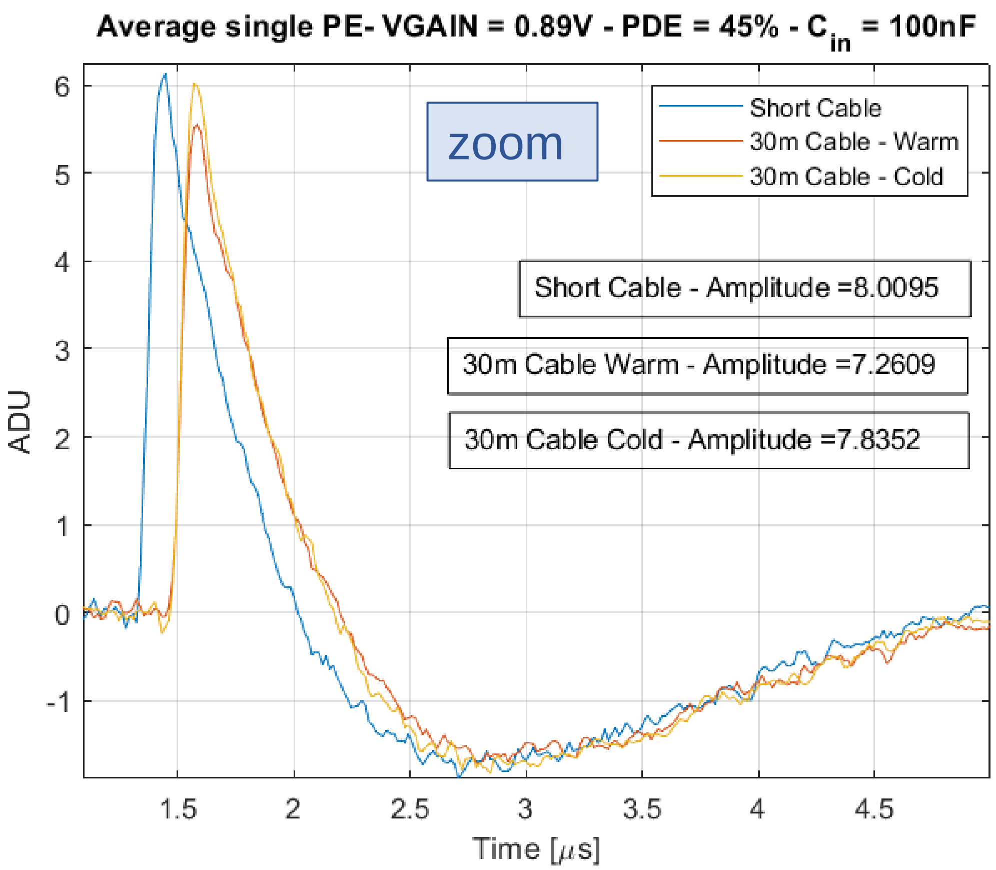
Cabling test

- We performed tests using ~30m of cabling to connect DAPHNE with the cold electronics. The cable is then connected to the flange board and terminated to DAPHNE with a flex cable DB15 adapter.
- The aim of the test is to check if the length of the cable has a negative effect, deteriorating the signal fidelity, especially after the modifications (patches) that were applied.
- The cables were tested at a warm temperature and submerged in liquid nitrogen.

Cabling test



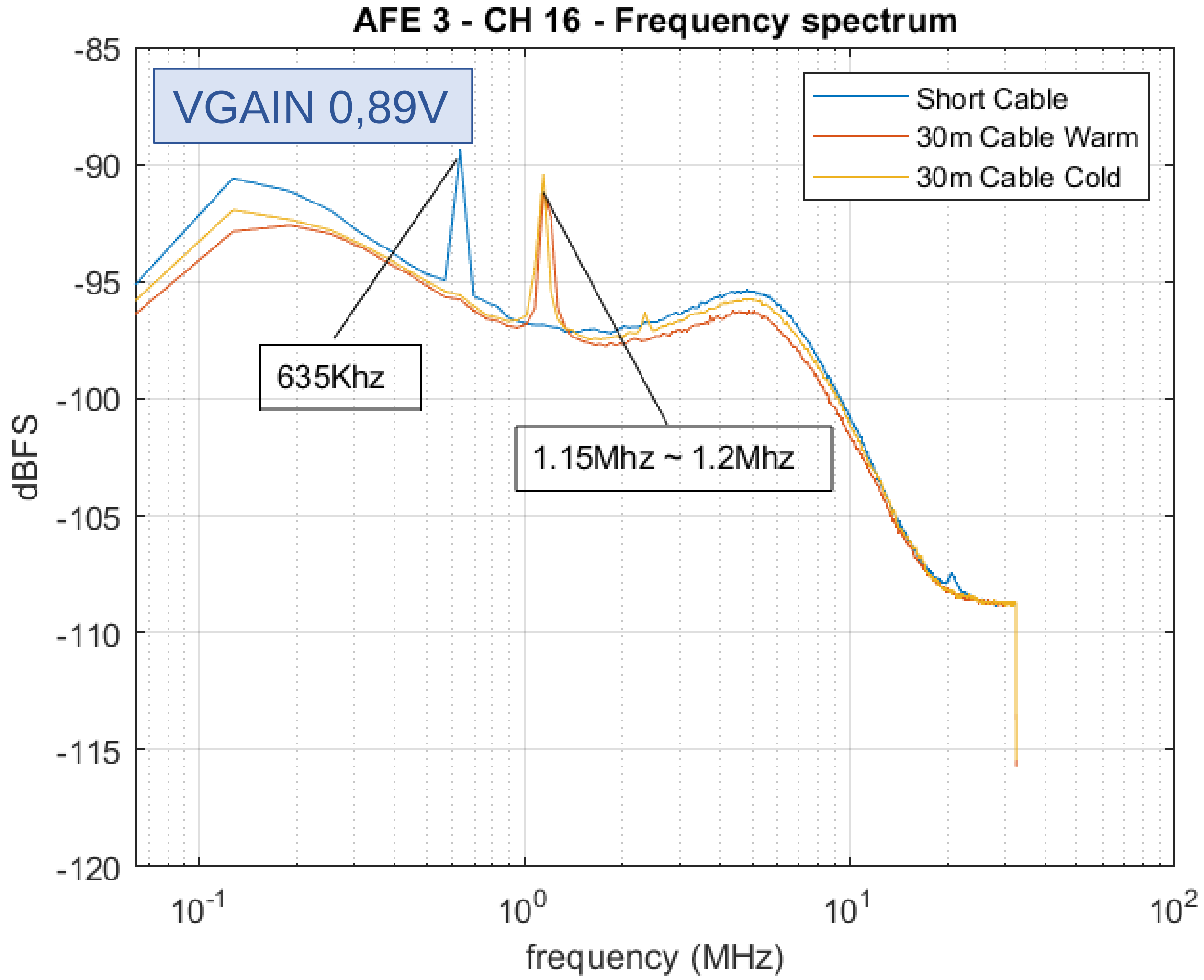
Average single PE- VGAIN = 0.89V - PDE = 45% - C_{in} = 100nF



Average single PE- VGAIN = 0.89V - PDE = 45% - C_{in} = 100nF

- The figures on top show the acquired average single P.E. waveforms for the short cable, 30m cable cold and warm.
- Visually inspecting these waveforms we can conclude that there is not any significant degradation in the signal fidelity caused by reflections or any other effects.
- We observed that the signal is delayed about 10 time ticks (~160ns).
- Closely inspecting, we see a 9,25% attenuation with the 30m cable at warm compared to the short cable. With the 30m cold cable, the attenuation gets reduced to 2,12% compared to the short cable. This behavior is expected due to the drop in the cable resistivity at cold temperatures.

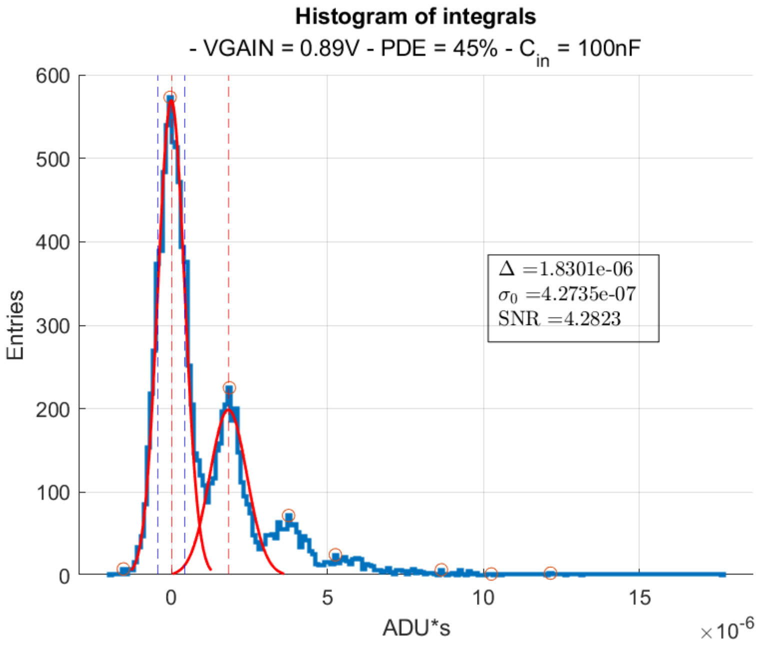
Cabling test



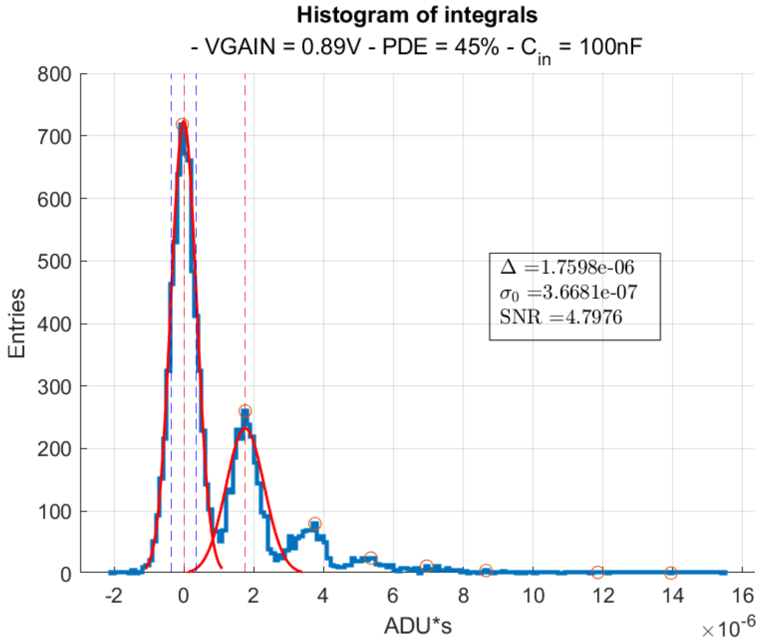
- Looking at the signal spectrum, we can see the attenuation factor for the frequency components in the waveforms.
- Here we see a behavior that was not expected, the infamous ~635KHz (that is most probably the switching frequency of the regulators) was attenuated and a new component appears at almost double the frequency.
- For us, it is not yet clear what is origin this effect but is clear that the 30m cable gives a clue.

Cabling test

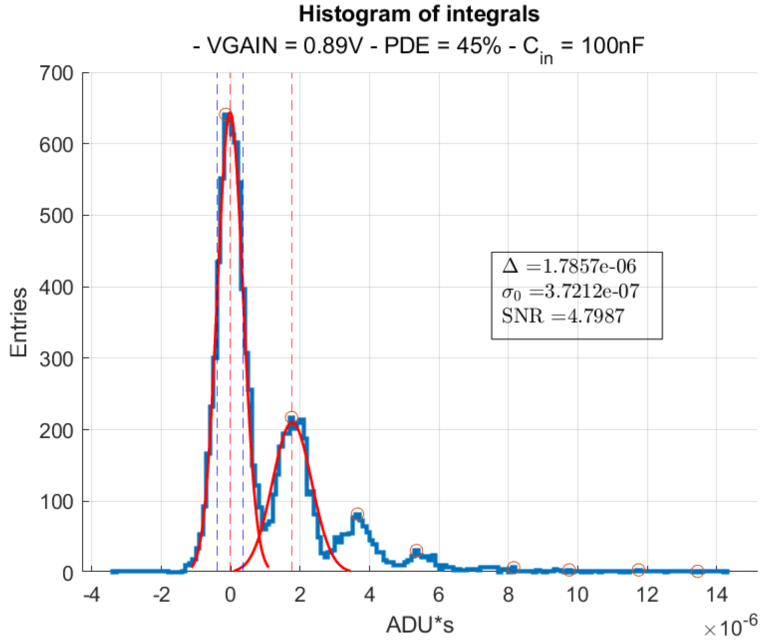
Short Cable



30m Cable Warm



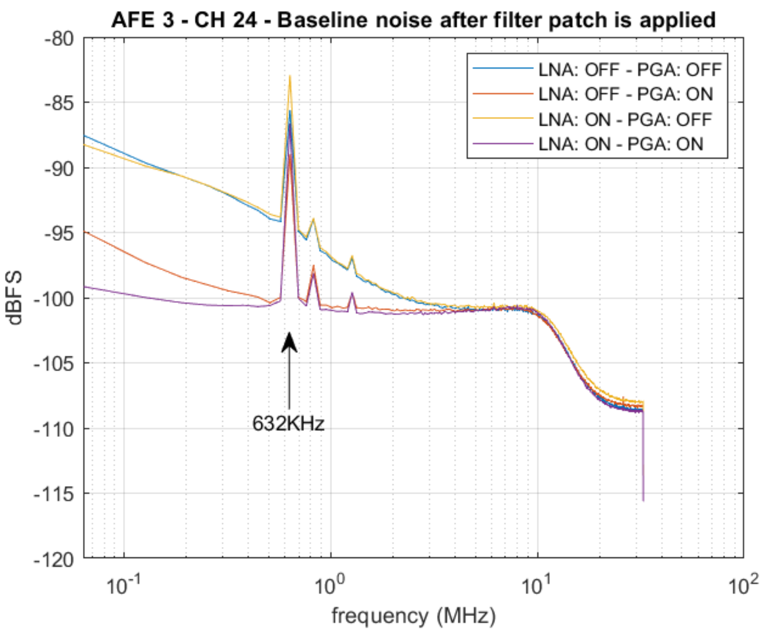
30m Cable Cold

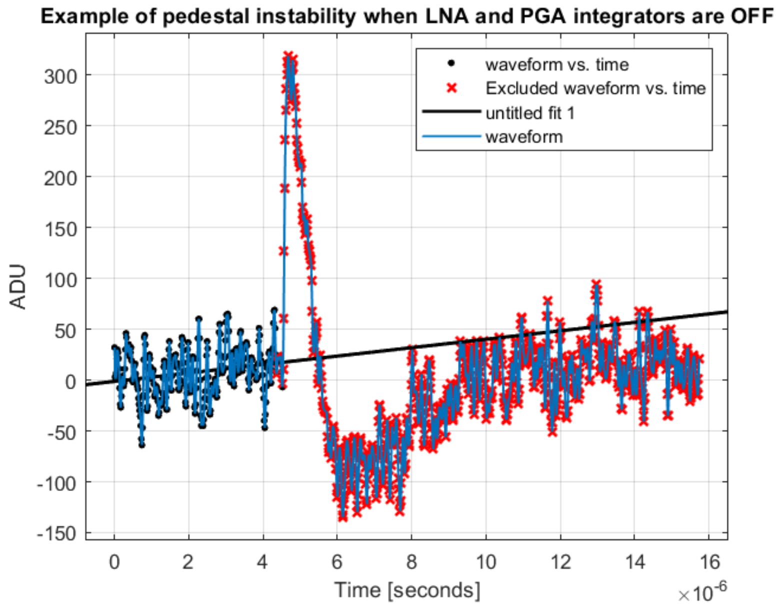


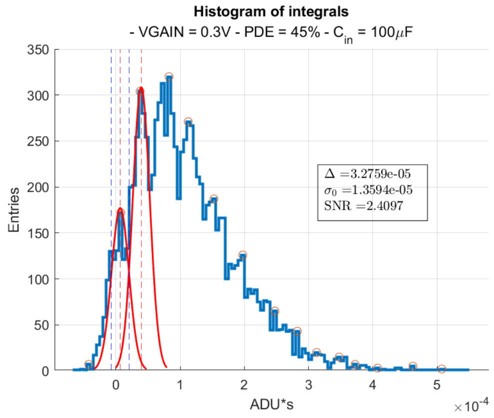
- These histograms show the SNR for the 3 different setups.
- We see an increase in the signal to noise ratio from ~4,28 to ~4,8 with both 30m warm and cold configuration compared to the short cable.
- This slight increase in SNR can be explained by the decrease in σ_0, probably caused by the frequency component shift of the noise from ~600Khz to ~1,2MHz, which is a frequency that has less impact in the SNR calculation.
- Also, the slight decrease in Δ can be explained by the attenuation factor caused by 30m the cable.

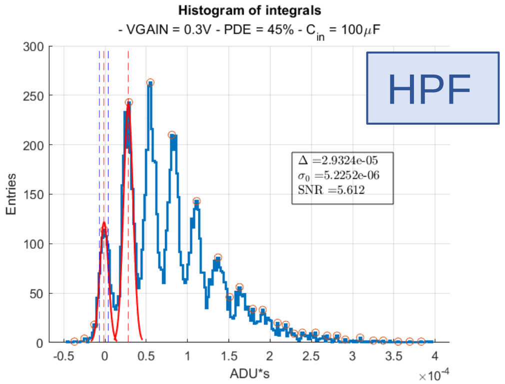
Digital Filtering

- We have noticed that with integrators OFF, we have a 1/f noise component that causes a pedestal instability due to the presence of low noise components.
- Just by applying an 80KHz digital high pass filter is enough to improve drastically the histogram.









Digital Filtering

- The AFE5808 has a digital HPF functionality described in page 48.
- We tested the digital filter with positive results, but the main drawback is that at the end it centers the signal at the middle scale just as turning on the LNA and PGA integrators, which limits the dynamic range.
- A solution is to implement this filter in the FPGA after the AFE Final Digital Output, adding the capability to restores the pedestal.

- Comment about the pedestal recovery: Removing the pedestal with a HPF is ideal for the data analysis and the triggering mechanism. Pedestal recovery is needed to correctly calibrate each channel to obtain the best dynamic range.

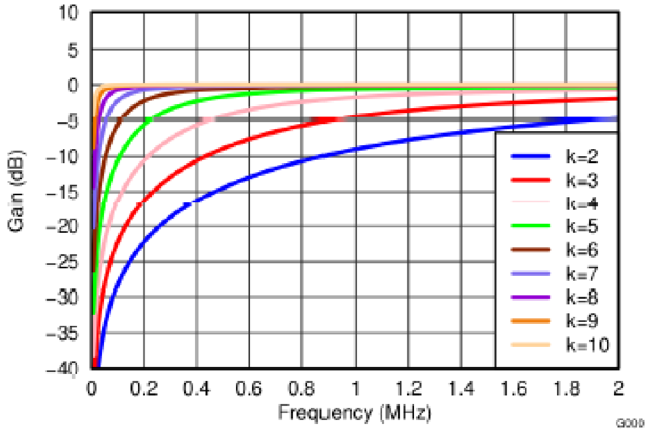


Figure 58. Digital High-Pass Filter Response

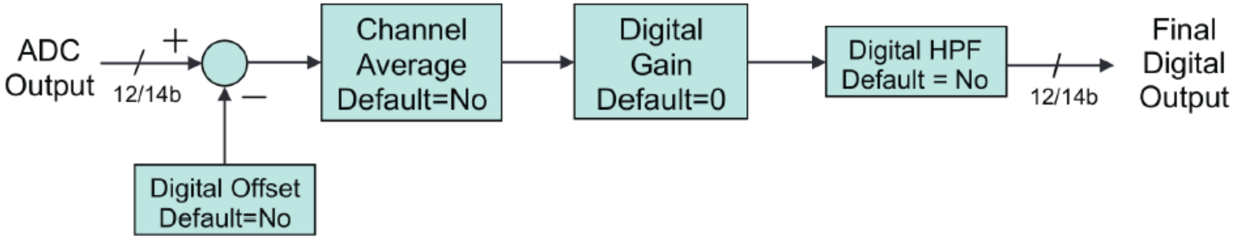
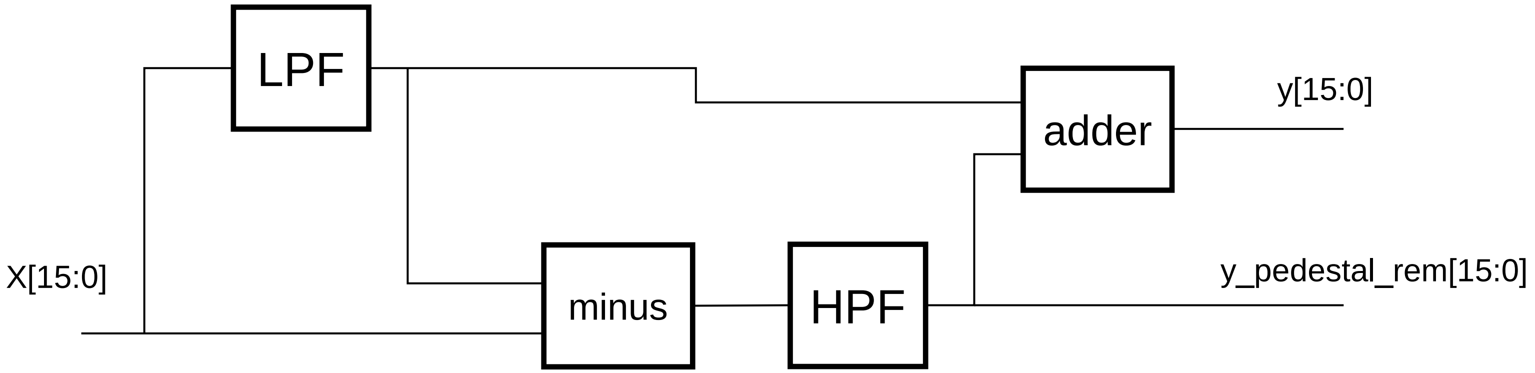


Figure 79. ADC Digital Block Diagram

$$y(n) = \frac{2^k}{2^k + 1}\left[x(n) - x(n-1) + y(n-1)\right]$$

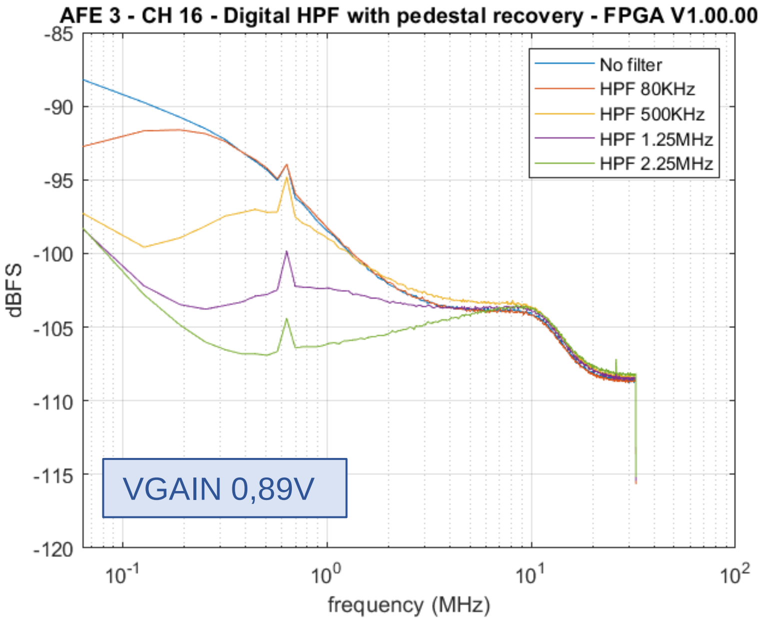
Digital Filtering

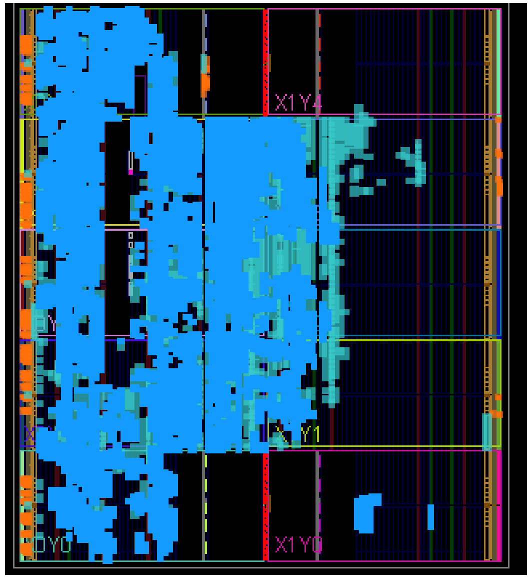
- We have implemented a very rudimentary proof of concept HPF with pedestal recovery for DAPHNE 40 channels.
- We have inserted it in Jamieson’s firmware, specifically working in a fork of commit e448dfc13fa5a73cb7bd0bad0c785dc7f6af6892, between the AFE frontend module and the SPY buffers.



Digital Filtering

- The digital filters seems to be working as expected as can be seen from the spectrum of the digitalized waveforms, and the ability to move the pedestal is maintained.
- The waveforms are with the cold amplifier disconnected.
- We have run behavioral and post-synthesis simulations with expected results.
- The next step is to test with the cold amplifier to see whether it improves the response.
- Right now, the design is very inefficient with the FPGA resources, using more than half of the DSP units. This can and will be improved after the concept test.





Resources used by filter